CA-22

Analog Input Output

Interface Operation Manual

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May 1980

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Aurora, Ohio 44202

Attn: Warranty Information

WARRANTY INFORMATION

Name_____ Phone ( )_____

Street_____

City_____ State_____ Zip_____

Purchased from_____ Date of purchase_____

Model Number_____ Serial Number_____
(see nameplate on back)

Please complete the following additional information so that we may be better able to meet your requirements in the future.

Age_____

Education ( ) high school
( ) college
( ) graduate

Occupation_____

Use of computer ( ) home
( ) business
( ) school

Software purchased? ( ) yes
( ) no

Peripherals purchased ( ) terminal
( ) printer
( ) other_____

Where you learned of OSI
( ) friend
( ) magazine_____
( ) trade show
( ) dealer
( ) other_____

Plans to expand system ( ) yes
( ) no

Type of software_____

_____

Additional software desired but not available_____

_____

Was dealer helpful? ( ) yes
( ) no

Does he carry full line of accessories? ( ) yes
( ) no

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AN INTRODUCTION TO THE OHIO SCIENTIFIC SIXTEEN PIN I/O BUS

Ohio Scientific is pleased to introduce a unique new product line - The 16 Pin I/O BUS. With this system, it is possible to add up to eight special function boards while occupying only the backplane slot.

This is made possible by a novel BUS extension method which allows decoding, timing and eight bits of data to be carried on standard, inexpensive 16 pin ribbon cables.

Up to eight inexpensive 16 pin cables with standard DIP connectors may be attached to a single CA-20 board which in turn occupies one slot of the standard Challenger backplane. Alternately, one 16 pin I/O BUS cable may be attached to the CA-15 board at the rear of all C4P and C8P products. Note, in the case of the C4P-MF this allows system expansion beyond the normal four slot backplane.

Currently five HEAD END CARDS are available for interconnection to the system via the CA-20 or CA-15 boards.

Computer Interface to Sixteen Pin I/O BUS

The 16 pin I/O BUS may be attached to your computer via two different boards - the CA-15 or the CA-20. The descriptions of these boards are as follows:

CA-15 Board

The CA-15 board is a standard accessory interface installed on the following Ohio Scientific systems: C4P-MF, C4P-DMF, and C8P-DF.

The CA-15 is mounted at the rear of the computer and contains the following interface connections:

Joystick and numeric keypad
Modem and serial printer
Sixteen PIA lines (normally used for the Home Security system - AC-17P)
Sixteen Pin I/O BUS

The interconnect for the Sixteen Pin I/O BUS is simply a 16 pin DIP socket. To use the BUS, all that you have to do is attach one end of the 16 pin ribbon cable to the CA-15 board and the other end of the cable to one of the HEAD END CARDS.

Please note that some of the HEAD END CARDS require more power than may be practically carried via the ribbon cable alone. Therefore, some of the cards require auxiliary power supplies.

CA-20 Board

The CA-20 board contains all the necessary logic to decode eight distinct HEAD END CARD interfaces. The actual interconnect, as with the CA-15, is via simple 16 pin DIP sockets and standard 16 pin ribbon cables.

The CA-20 board also requires one slot of your computer's backplane. But remember, from this one slot you gain access to a maximum of eight accessory boards.

The CA-20 is recommended for use in the Ohio Scientific C2 series and C3 series computers. It can also be installed in C4P and C8P series systems with some modification to the CA-15 interface.

Since the logic required for the I/O BUS interface is simple, an additional feature was added to the CA-20 board - a crystal controlled "time-of-day" clock (hardware) subsystem. The operation of the clock, excepting reading time and setting time, is totally independent of the host computer. As a matter of fact, with the included on-board, auto-recharging, battery back-up, your computer may actually be turned off for several months without losing time.

The features of the clock subsystem are as follows:

Hours, minutes, seconds and 1/10 seconds
Day of week
Day of month
Month of year
Four Year calendar

If you happen to own (or use) a C2 series or C3 series computer, the CA-20 board can actually control the power cycling of the entire computer when equipped with an optional power sequencer package. This means you can preset a time (month, day, hour, etc.) within the clock subsystem and when that preset time agrees with the actual time, A.C. power is applied to the entire computer system through the power sequencer. At a later time, the system's A.C. power may also be removed and the system shut down under software/clock subsystem control.

For applications where the clock subsystem is not required, the CA-20A will perform all the Sixteen Pin I/O BUS functions associated with full-feature CA-20.

HEAD END CARDS

HEAD END CARDS is a general name used to describe any or all of the special function boards which attach to the Ohio Scientific Sixteen Pin I/O BUS. There are currently five such boards and, with the exception of the CA-22, they will only interface with the computer via the Sixteen Pin I/O BUS.

Please note, as detailed earlier, you must use a CA-15 or a CA-20 board at the "computer end" of the Sixteen Pin I/O BUS to complete the interface.

In the following pages a brief product and application description of the currently available HEAD END CARDS will be presented.

Bit Switching and Sensing —— The CA-21

The CA-21 is a 48 line parallel I/O board featuring three 6821 PIAs (peripheral interface adapters) and prototyping/interconnect areas.

The use of PIAs in the design allows for maximum interface versatility as you may configure any one of the 48 I/O lines as either an input or an output. As outputs, each line is capable of driving a minimum of one standard TTL load.

Additional versatility is added because 24 of the lines, when configured as outputs, may simultaneously function as inputs. This feature, although somewhat confusing, is extremely useful for applications such as switch matrix decoding.

Each of the 48 lines is brought out to two foil pads (suitable for wire wrap stakes) as well as a location on one of four 12 pin Molex-type female edge connectors. There are also eight 16 pin DIP socket locations which are intended for use as prototyping areas. Additionally, the 12 PIA "hand-shaking" lines are brought to 12 single foil pads.

The CA-21, with proper buffering, may be used for virtually any computer controlled bit switching or bit sensing application that you can imagine. With a full complement of eight CA-21s interfaced via the CA-20, a total of 384 individually controllable I/O lines are possible!

An interesting application using one CA-21 board would be a complete, if somewhat slow, emulation of the standard Ohio Scientific BUS.

A more standard application might be augmenting the standard Home Security System (AC-17P) with "hard-wired" sensors.

One type of sensor you could easily add is a standard window "perimeter detector". This could be done with commercially available adhesive foil tape. You could then detect a break-in (through a broken window) by sensing a break in the foil tape.

Another useful application you could set up in concert with the AC-12P wireless A.C. Remote Control, might be sensing when a room is entered. You could accomplish this with pressure-switch door mats or door switches. When room entry is detected, the lights could be turned on or, turned off on exit.

If you are designing any sort of dedicated control system, the CA-21 is an ideal choice. You can easily sense many types of input (pressure transducers, flow sensors, switches, etc.) while controlling outputs from a simple single LED display to a network of solid state relays controlling A.C. power.

EPROM Programmer —— The CA-23

The CA-23 is an EPROM programmer designed for use with the growing families of 5 volt only EPROMS. With the CA-23 you can program and verify all 1K through 8K byte EPROMS of this type. Note these parts are often identified as 8K - 64K bit EPROMS.

The CA-23 can program (or verify) data in two basic modes - EPROM to/from EPROM or EPROM to/from computer RAM memory.

Additionally, EPROM data may be read directly into the computer's RAM memory.

There are four LED indicators on the CA-23. The first is "SOCKET UNSAFE". This means that a programming voltage is present at the socket and if you insert or remove an EPROM it is likely to be damaged.

The second indicator is "PROGRAMMING". This means that your EPROM is currently being programmed.

The third indicator is "ERROR". This means that somewhere along the line your programming attempt was unsuccessful.

The final indicator is "PROGRAM COMPLETE". This means that your program and verification was successful.

The most intriguing application for this product is the creation of "custom" parts for your computer or peripherals. This could range from a new system monitor to a new high level language. It could even include a new character generator for your CRT or printer. Note, however, tinkering around with the internals of computers and peripherals requires a fairly high degree of technical expertise. Also, most manufacturer's warranties are voided by these types of modifications.

Several OEM (original equipment manufacture) and Research/ Development applications will be immediately obvious to those of you involved in that work.

The CA-23, as previously mentioned, is designed for use with 1K through 8K byte EPROMS. These parts come in various package styles and have various product names. For example, Intel's 2K x 8 part is the 2716, Texas Instruments' part is known as the 2516.

The CA-23 has both 24 pin and 28 pin zero insertion force sockets for reading, programming and verifying the EPROMS.

Prototyping ——— The CA-24

The CA-24 is a solderless bread-board designed for prototyping, experimental and educational applications.

The bread-boarding is made up of seven solderless plug-strips of the type manufactured by AP Products. Two of the plug-strips contain a connection matrix of 5 by 54 connections and are used as signal distribution points. Another pair of 96 location plug-strips are for powering the bread-board area. The actual experimenter area is comprised of three plug-strips, each with a 10 by 64 location connection matrix. Additionally, sixteen LED indicators and sixteen DIP switch positions are provided for signal observation and control functions.

Board I/O is via TTL latches and bi-directional PIA ports as well as direct (buffered) data, signal and control lines from the computer BUS. This method allows you to directly interconnect devices such as 6850 ACIAs in addition to doing more "isolated" and/or independent circuits.

The CA-24 also contains a "clock" generator which is continuously variable from approximately 25,000 Hz. through 70,000 Hz. You may also connect the clock to an on-board 16 stage divider chain. This allows division of the fundamental frequency by as little as 2^1 (2) to as much as 2^{16} (65,536).

The applications for the CA-24 are primarily prototyping and experimenting. Parts may be inserted and removed from the

terminal strip blocks over and over. Interconnection of parts is accomplished simply with solid, narrow gauge wire jumpers. Errors in design or connection are extremely easy to correct.

The CA-24 lends itself very well to structured experiments that are common in the educational environment. It is an ideal tool to aid in the teaching of computer and computer interface fundamentals.

Accessory Interface —— The CA-25

The CA-25 is designed to implement some of the functions normally associated with the CA-15 interface board.

It allows you to directly connect the Home Security System (AC-17P) and/or the Wireless A.C. Remote Control System (AC-12P) to C2 and C3 series computers. Additionally, if you own an older Ohio Scientific computer, you can now easily connect these systems to it.

An extremely useful application of the CA-25 is associated with small business systems. Using the CA-25 with the Home Security System, and perhaps a CA-15V (Universal Telephone Interface with speech synthesizer output), the computer could do payroll, inventory, etc. by day and "guard" the shop by night.

Analog I/O —— The CA-22

The CA-22 is a high speed analog I/O module. Although the CA-22 is classified as a HEAD END CARD, it differs from the rest of the family in that it may also be plugged directly into the computer's standard internal BUS. This allows for maximum flexibility in the use of the CA-22.

The analog input section of the CA-22 consists of a 16 channel amalog multiplexer. This means that you may connect up to 16 separate signals directly to the CA-22. Also included is a sample and hold circuit followed by the analog to digital converter circuitry.

The A to D converter is capable of either 8 bit or 12 bit operation. You may select these options under software control.

The accuracy of the converter is plus or minus one in the least significant bit. The stability of the circuit is rated at one millivolt drift per degree Centigrade.

The A to D conversion is extremely fast. It is capable of digitizing up to 66,000 samples per second in the 8 bit conversion mode and 28,000 samples per second in the 12 bit mode. Shannon Sampling Theory states that signals should be sampled at twice the highest frequency present. Therefore, it is possible for you to convert signals with a frequency greater than 30K Hz. Clearly, high fidelity audio is well within the spectrum of the CA-22.

The multiplexer has very high impedance inputs and is capable of accepting inputs in the range of -10 volts through +10 volts. The input is jumper selectable for other settings including a single sided range of 0 through +10 volts.

Due to the indeterminable nature of the actual inputs that you may actually apply to the CA-22, only the multiplexer inputs are brought out. However, a quad op-amp is laid out in foil which you may populate in several different modes to handle some of the more "common" input configurations.

The analog output section of the CA-22 consists of two identical high speed digital to analog converters. Each DAC can convert either 8 bits or 12 bits of data. Data input to the DACs is latched in such a manner that, when in the 8 bit conversion mode, the other four (of the total of twelve) bits are continuously output at a predefined value. You may, of course, define that value under software control.

The output of each DAC is buffered with a high speed op-amp capable of changing output voltage at the rate of 20 volts per microsecond. The standard configuration of each output is bi-polar with a voltage swing of -10 volts through +10 volts. This is jumper selectable to allow a uni-polar output of 0 through +10 volts.

Some additional I/O capacity is provided on the CA-22. There are three TTL level inputs and six open collector logic outputs. These are strappable to be either standard TTL level outputs or high-voltage outputs.

You can use the CA-22 for a multitude of analog sensing and/or analog controlling applications.

Using the proper transducers and the 16 input channels, you can monitor the temperature in several zones of a home or office. By extending this system with a CA-21, you could maintain precise temperatures by switching the proper controls on and off.

Another interesting, if somewhat obvious application, is in audio processing. Reverberation, phase shifting and echoing are just a few of the uses you could implement.

If you used blocks of RAM for data storage, other applications such as frequency doubling, etc., could be experimented with.

If you apply more sophisticated software techniques, such as a fast Fourier transform, on stored input data, very elaborate signal processing becomes realizable. Projects such as audio spectrum analyzers and speech recognition experiments are certainly practical. Note, in these types of applications you are likely to find some signal pre-processing in hardware is certainly beneficial - if not totally necessary.

If you employ both DAC outputs and the on-board unblanking circuit, X-Y oscilloscope plotting is an interesting application. By using these techniques and one or more of the analog inputs, you can construct a digital storage scope. Note, both of these applications require that you have access to an oscilloscope capable of X-Y input as well as blanking.

Summary

With the introduction of the 16 pin I/O BUS, Ohio Scientific has opened a new world of interfacing capabilities for both the large and the small computer user.

Systems ranging from totally automated sampling and control stations to complete R/D setups to educational lab stations are now available to you via standard building blocks and standard computer systems.

For pricing and availability, contact your nearest Ohio Scientific dealer.

CA-22

Overview

The analog I/O (input/output) board is a high performance analog to digital (A/D) and digital to analog converter (DAC) interface board with the following features:
16 channel (multiplexed) 12 or 8 bit A/D (analog to digital converter) with S/H (sample and hold) and very high impedance inputs. The CA-22 Analog I/O (input/output) provides the capability of converting up to 16 channels of continuous signals into discrete digital values which can be processed on your OSI computer. The user's program can scan one channel (PORT) continuously or all sixteen, or any combination, with each individual port selectively converted at 8 or 12 bit resolution, depending on the requirements of the application. High sampling rates with high resolution are available. A resolution of 12 bits (Ø.Ø25% of full scale reading) or 8 bits (Ø.4% of full scale reading) may be selected. The software to control data acquisition is very simple and straightforward. Since the conversion is performed completely by the successive approximation type converter, no software conversion routines are required. The user's program need only instruct the CA-22 which port and at what resolution. This allows the processor complete freedom during the hardware conversion process to perform other tasks if required. This also allows the use of high level languages such as BASIC as well as machine code routines. The 16 port A/D is strappable to several unipolar (positive excursions from the ground reference) or bipolar (positive or negative excursions) to take full advantage

of the resolution of the converter. The maximum FSR (full scale range) is +10V to -10V (20V peak/peak) at 4.8 millivolt resolution per bit for 12 bit resolution (see chart, Figure 1, in another section of this manual for possible FSR ranges); 8 bit resolution of +/- 10 volts corresponds to 78 millivolt resolution.

Data and control are handled by use of dedicated addresses (device registers) which are treated as memory addresses. Additionally, three logical input lines and six logical output lines are provided on the J4 connector on the CA-22 board. These logical lines permit convenient interconnection to external circuits. The logic line data is also available in registers for normal programming.

The resolution of the CA-22 board is consistent with many process control and laboratory instrumentation demands; high fidelity audio processing can be easily accommodated with these capabilities.

Two 12 Bit D/A channels (digital to analog converters). Each D/A channel is identical and operates independently of the other. They may be operated directly in either the 8 bit or 12 bit mode at the discretion of the user depending on the resolution required. Each D/A may be independently strapped to several FSR ranges from 5V peak/peak to 20V peak/peak. The FSR range capability is identical to that of the A/D converter as is the bit resolution. Each D/A incorporates a current driven buffer for protection of the A/D and to provide very fast slew rates (voltage change vs time). Each D/A is capable of FSR

voltage swings (-10V to +10V) in less than two millionths of a second (2 microseconds) including switching, slewing and settling time.

Logic Control Inputs/Outputs

Some applications may require logic control of the device the CA-22 is interfaced to, such as servo-drive direction and master enables, tape recorder control, or remote sensor enables. Six logic outputs and three logic inputs have been provided for this reason. The six outputs are latched, negative is true, buffered open collector drivers. These are configured as TTL compatible as shipped from the factory but can be strapped for higher voltage operation (up to 30V) by the user. The three inputs are TTL compatible with termination capability in artwork (user populated resistors).

X-Y Scope Plotting

The CA-22 is provided with circuits to enable X-Y scope plotting by the user. The user must have access to an oscilloscope with X-Y inputs and an intensity or blanking input (usually found on the back of the scope). The two D/A converters provide the X-Y outputs and an output from the CA-22 (unblank) provides the blanking control. Many applications are possible using this technique including a digital or analog storage scope.

HEAD END CARD or Motherboard Installation

The CA-22 is unique compared to other 'HEAD END CARDS' because it can be installed inside the computers card cage connected to the standard bus or outside of it on the OSI accessory bus for "hands on" use. See the installation section for more information.

Artwork Conveniences

In some applications the user may wish to pre-process the incoming analog information (filters, preamplifiers, summing amplifier, etc.) to lighten the load of the processor in "Real Time" or to decrease the complexity of the software required in advanced applications or experiments such as voice recognition, audio processing, etc. An area in artwork is included that provides the interconnections required to construct most of the typical op-amp circuits discussed. Also provided is a prototyping grid for digital or analog circuits the user may deem necessary for the application intended. Parts for these circuits are supplied by the user. Refer to other sections of this manual for more detail.

Summation

The CA-22 is a very accurate, fast analog interface module that can be used in a vast amount of different applications or experiments. The software to control the data acquisition is very simple and in some cases such as continuous (8) bit conversions of only one channel, the software need only read a location to obtain valid and continuously updated A/D information.

The A/D conversion rates 68,000 (8) bit or 28,000 (12) bit conversions per second and the accuracy (+/- 1LS) and the D/A conversion rate of full scale resolution swing in under two microseconds and an error of only (+/- 1LS) certainly would suggest many possible applications to the user. Some of these may be high fidelity audio processing, speech input/output lab, process control or home/business environmental control.

The conversion rates mentioned above are for single port conversion. The conversion rate of each channel when polling the ports will be slightly slower than the conversion rate divided by the number of ports polled. The above rates (68,000 - 8 bit or 28,000 - 12 bit) are a conservative figure. In actual practice the rates should be closer to 30,000 (12) bit and 70,000 (8) bit conversions per second, although these are not guaranteed.

CA-22 I/O ASSIGNMENTS

R/W	HEX	DECIMAL	REGISTER	7	6	5	4	3	2	1	Ø
R	C7Ø8	5Ø952	DATA	AD11	AD1Ø	AD9	AD8	AD7	AD6	AD5	AD4
R	C7Ø9	5Ø953	STATUS/DATA	1=RDY	I/OIN6	I/OIN5	I/OIN4	AD3	AD2	AD1	ADØ
W	C7ØA	5Ø954	CONTROL	1=12 BIT Ø=8 BIT	1= EN-INT	Ø=FLAG ENABLE	X	MD	MC	MB	MA
W	C7ØB	5Ø955	LOGIC OUT	X	X	$\overline{\text{OUT5}}$	$\overline{\text{OUT4}}$	$\overline{\text{OUT3}}$	$\overline{\text{OUT2}}$	$\overline{\text{OUT1}}$	$\overline{\text{OUTØ}}$
W	C7ØC	5Ø956	DAC1-HIGH	D11	D1Ø	D9	D8	D7	D6	D5	D4
W	C7ØD	5Ø957	DAC1-LOW	X	X	X	X	D3	D2	D1	DØ
W	C7ØE	5Ø958	DAC2-HIGH	D11	D1Ø	D9	D8	D7	D6	D5	D4
W	C7ØF	5Ø959	DAC2-LOW	X	X	X	X	D3	D2	D1	DØ

R/W = READ ONLY (R) OR WRITE ONLY (W)

$\overline{\text{SIG NAME}}$ = LOGIC OUTPUTS ARE LOW TRUE (Ø=1)

Software

The analog to digital converter hardware is configured such that several different modes of data acquisition are available. A flag is provided that is used to inform the user that a new conversion is complete and updated data is available. This flag must always be used in the 12 bit mode and may or may not be used in the 8 bit mode at the discretion of the user.

The flag is necessary in 12 bit operation since a 12 bit word is being processed by an 8 bit machine. If the status register is read and the flag is valid the hardware sets an internal status register which prevents the data buffer from being modified until after the computer has read the second byte. Therefore, there are no timing considerations that must be observed in this operation other than the order of data acquisition which is the 4LSB's first and the 8 MSB second. The only other consideration in the flag mode is if one or all of the three TTL inputs (which are returned in the status register) are to be used, they must not be independently accessed. That is, the three inputs should be scanned only when reading the status register while looking for a data valid flag; when a valid data flag is returned the digital data can be masked from the analog data and immediately processed or stored. Repeatedly reading the status register, when the data conversion is complete, will result in the most significant bits of data being held constant, i.e. not being updated. For this reason, the sample program #1 is the preferred way to program.

If it is not required by the application, the flag circuitry may be turned off in the 8 bit mode. Reading the A/D information is then done simply by reading a location ($C7Ø8).

Analog input port selection is done by writing to $C7ØA. When scanning ports the flag mode should be used to insure an updated conversion of the selected port is complete. Bits MA to MD=Ø would select port Ø and bits MA to MD=15 would select port 15. If port 2 is to be read using the flag mode, the correct data to store at $C7ØA would be $Ø2 for 8 bit operating and $82 for 12 bit operation. This value should be stored twice in immediate succession to force a new conversion of the new port. $C7Ø9 would then be read checking D7 for a 1 or valid data flag. When the flag is received, the lower 4 bits of a 12 bit conversion are returned in DØ-D3 and in 8 bit conversions these 4 bits are simply ignored. Also during this time, the three TTL inputs are returned in D4-D6 of $C7Ø9. The most significant (MS) 8 bits of a 12 bit conversion and the 8 bits of an 8 bit conversion are then simply reading $C7Ø8. $C7Ø8 will not be modified by the hardware until it has been read.

EX.1. 12 Bit Mode

> Initialize the control register ($C7ØA) to 12 bit, enable flag and select port (1XØXXXXX). When valid data is available, D7 of $C7Ø9 will be a one. On the cycle that a valid data flag is received the least significant 4 bits of the conversion are returned in D3-DØ, and the most significant 8 bits are available at $C7Ø8, which are latched and will not be updated again until after $C7Ø8 has been read.

EX.2. 8 Bit Mode With Flag

Initialize control register ($C70A) to 8 bit, enable flag and select port (ØXØXXXXX). When valid data is available, D7 of $C709 will be a one. After the valid data flag is read, the 8 bit conversion data is available at $C708 and will not be updated until after it is read.

EX.3. 8 Bit Mode No Flag

Initialize control register ($C70A) to 8 bit, disable flag and select port (ØX1X-XXXX). After initializing or any write to $C70A to change ports a period of at least 20us must be allowed before valid data is available at $C708. Thereafter, the data will always be valid and updating.

Control of the two 12 bit D/A converters is handled by simply storing data in two buffers for each A/D.

The least significant four bits are stored in a hardware buffer and are not presented to the D/A until the MS eight bits are written. A 12 bit word would be written to DAC1 by writing the LS four bits to $C70D then the MS eight bits to $C70C. If 8 bit operation is desired, the LS four bits should be initialized once at the beginning of the program and, thereafter, only the MS eight bits would be written to $C70C. DAC2 operation is identical, with the LS four bit buffer at $C70F and the MS eight bit buffer at $C70E. The DAC order of magnitude is D7=MSB (most significant bit) and DØ=LSB (least significant bit).

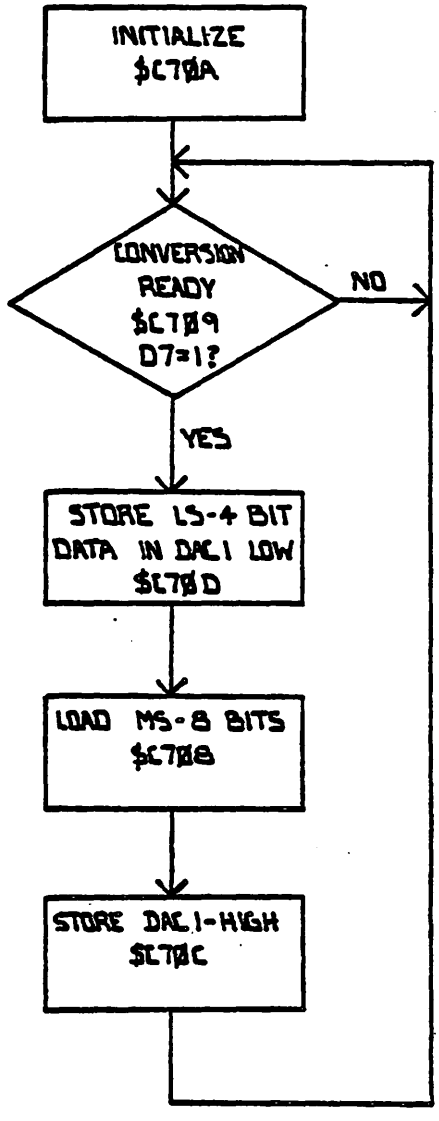
Audio Demonstration

An interesting experiment or demonstration of the audio processing capability of the CA-22 would be to connect the output of the preamplifier from a radio, tape player, etc., to an input of the CA-22 then one of the D/A outputs to the input of an audio amplifier. A simple program could then be used to simply 'pass' the converted audio data from input to output of the analog board. If good quality audio equipment is used in this experiment the high fidelity capability of the CA-22 will be realized. Connect the preamplifier output to Port #Ø at J2 Pin 1 and the ground to J2 Pin 2 (use shielded cable). Connect the audio amplifier to DAC1 at J2 Pin 12 and the ground to J2 Pin 11 (use shielded cable). The program found in this manual (PROG. 1) should then be executed and the audio adjusted to a suitable level. Prog. 1 instructs the A/D to do 12-bit conversions of the audio signal then transfers the digital encoded audio data to DAC1 for conversion back to audio. This program could be easily modified to perform 8 bit conversions. Change the #$8Ø in line 2ØØ to #Ø and delete line 28Ø. Both of the above programs use the flag mode. In 8-bit audio processing the flag is not usually required. To convert Prog. 1 to 8-bit mode using no flag change the #$8Ø in line 2ØØ to #$2Ø, delete lines 22Ø, 26Ø, 27Ø, and 28Ø. The label "LOOP" should be inserted in line 29Ø. The FSR (full scale range) of the A/D and D/A may have to be lowered for this experiment.

I think it should be J2, Feb 26, 1981 WF. Pin 3 ?

```
 10                ;   **********************************
 20                ;   **          PROG. 1             **
 30                ;   **********************************
 40                ;   ** A/D D/A SAMPLE PROGRAM  **
 50                ;   ** READ ANALOG INPUT PORT 0**
 60                ;   ** AND OUTPUT TO DAC 1  12 **
 70                ;   ** BIT RESOLUTION. REPEAT  **
 80                ;   **********************************
 90                ;
100 C708=           ADHIGH=$C708      A/D MS(8) BITS (D7)=MSB
110 C709=           ADLOW =$C709      A/D LS(4) BITS & FLAG (D0)=LSB
120 C70A=           CONTRL=$C70A      CONTROL REGISTER WRI/ONLY
130 C70C=           DAC1H =$C70C      D/A(1) MS(8) BITS & WORD STRB
140 C70D=           DAC1L =$C70D      D/A(1) LS(4) BIT BUFFER
150                 ;
160 4000                    *=$4000   OBJECT CODE DESTINATION
170                 ;
180                 ;       **** INITIALIZE ****
190                 ;
200 4000 A930       START   LDA #$30        12 BIT, FLAG ENABLE, PORT(0)
210 4002 8D0AC7             STA CONTRL      INITIALIZE PARAMETERS
220 4005 8D0AC7             STA CONTRL      FORCE NEW CONVERSION
230                 ;
240                 ;       **** MAIN BODY  ****
250                 ;
260 4008 AD09C7     LOOP    LDA ADLOW       GET CONVERSION STATUS
270 400B 10FB               BPL LOOP        IF (D7)=0 NOT READY
280 400D 8D0DC7             STA DAC1L       STORE VALID DATA DAC BUFFER
290 4010 AD08C7             LDA ADHIGH      GET MS(8) BITS
300 4013 8D0CC7             STA DAC1H       AND STROBE DAC W/12 BIT DATA
310 4016 4C0840             JMP LOOP        GO DO IT AGAIN
```

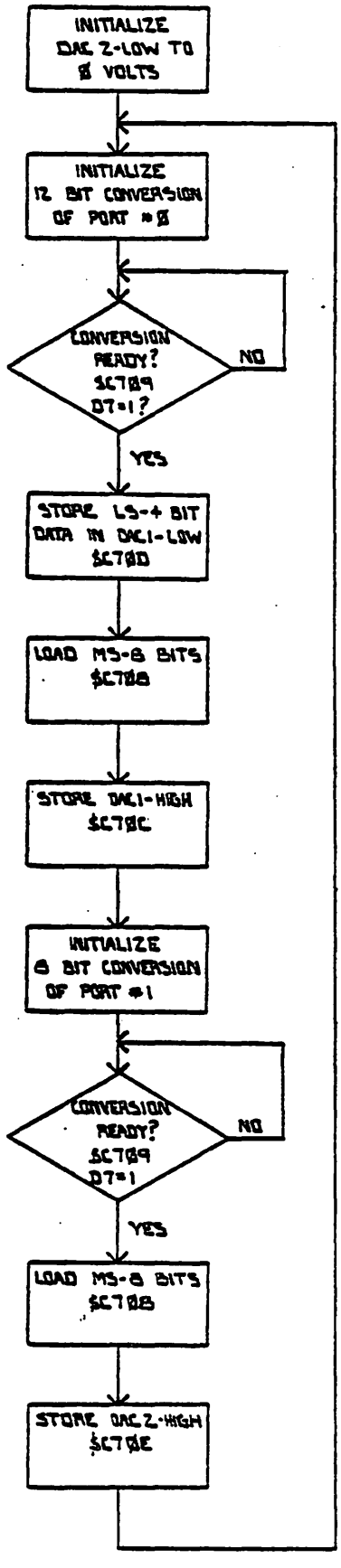
PROGRAM 1



WHEN STATUS REGISTER ($C709) IS READ AND D7=1 (READY) THE LEAST SIGNIFICANT 4 BITS OF A 12 BIT CONVERSION ARE VALID AND RETURNED IN THE SAME READ CYCLE

```
 10                 ;       **********************************
 20                 ;       **          PROG. 2             **
 30                 ;       **********************************
 40                 ;       ** A/D D/A SAMPLE PROG.  **
 50                 ;       ** READ ANALOG INPUT     **
 60                 ;       ** PORT(0) AND OUTPUT TO**
 70                 ;       ** DAC(1) 12 BIT RESOLU-**
 80                 ;       ** TION, READ INPUT PORT1:**
 90                 ;       ** AND OUTPUT TO DAC(2) **
100                 ;       ** 8 BIT RESOLUTION.     **
110                 ;       ** REPEAT ENDLESS LOOP   **
120                 ;       **********************************
130                 ;
140 C708=           ADHIGH=$C708          A/D MS(8) BITS (D7)=MSB
150 C709=           ADLOW =$C709          A/D LS(4) BITS & FLAG (D0)=LSB
160 C70A=           CONTRL=$C70A          CONTROL REGISTER WRI/ONLY
170 C70B=           IOUT  =$C70B          6 BIT DIGITAL OUT
180 C70C=           DAC1H =$C70C          D/A(1) MS(8) BITS & WORD STRB
190 C70D=           DAC1L =$C70D          D/A(1) LS(4) BIT BUFFER
200 C70E=           DAC2H =$C70E          D/A(2) MS(8) BITS & WORD STRB
210 C70F=           DAC2L =$C70F          D/A(2) LS(4) BIT BUFFER
220                 ;
230 4000                  *=$4000         OBJECT CODE DESTINATION
240                 ;
250                 ;       **** INITIALIZE ****
260 4000 A90F       INIT    LDA #15           INITIALIZE DAC2 LS(4) BITS
270 4002 8D0FC7             STA DAC2L         TO (0V)
280                 ;
290                 ;       **** MAIN BODY  ****
300                 ;
310 4005 A980       START   LDA #$80          12 BIT, FLAG ENABLE, PORT(0)
320 4007 202140             JSR RDY           SET PORT AND GET RDY FLAG
330 400A 8D0DC7             STA DAC1L         STORE LS(4) BITS DAC(1)
340 400D AD08C7             LDA ADHIGH        GET MS(8) BITS PORT(0)
350 4010 8D0CC7             STA DAC1H         & STROBE 12 BIT DATA
360 4013 A901               LDA #1            8 BIT, FLAG ENABLE, PORT(1)
370 4015 202140             JSR RDY           SET PORT AND GET RDY FLAG
380 4018 AD08C7             LDA ADHIGH        GET MS(8) BITS PORT(1)
390 401B 8D0EC7             STA DAC2H         & STROBE 12 BIT DATA
400 401E 4C0540             JMP START         & GO DO IT AGAIN
410 4021 8D0AC7     RDY     STA CONTRL        SET PARAMETERS AND PORT #
420 4024 8D0AC7             STA CONTRL        FORCE NEW CONVERSION
430 4027 AD09C7     LOOP    LDA ADLOW         CHECK CONVERSION STATUS
440 402A 10FB               BPL LOOP          IF D7=0 NOT READY
450 402C 60                 RTS               WE HAVE VALID DATA!-RETURN
```

PROGRAM 2


INITIALIZE DAC 2-LOW TO Ø VOLTS
INITIALIZE 12 BIT CONVERSION OF PORT #Ø
CONVERSION READY? $C7Ø9 D7=1?
NO
YES
STORE LS-4 BIT DATA IN DAC1-LOW $C7ØD
LOAD MS-8 BITS $C7ØB
STORE DAC1-HIGH $C7ØC
INITIALIZE 8 BIT CONVERSION OF PORT #1
CONVERSION READY? $C7Ø9 D7=1
NO
YES
LOAD MS-8 BITS $C7ØB
STORE DAC2-HIGH $C7ØE

```
1 GOTO 10
2 :
3 :                  PROG. 3
5 :       D. C.    D. V. M PROGRAM USING 574
7 :       CAN ALSO BE USED TO ADJUST GAIN
8 :       AND OFFSET USING 4 1/2 DIGIT D. V. M.
9 :
10 A=50952:REM ADDRESS OF A/D
15 R=20/4096:REM RESOLUTION=20 VOLTS SCALE / 12 BIT(2↑N)
20 POKEA+2,128:REM SET UP PORT AND BITS AND ENABLE
23 :
25 FOR LOOP=1TO20:REM TAKE AVERAGE OF READING TO PREVENT JITTER
30 H=PEEK(A+1):I=H:REM CHECK FOR CONVERSION READY
40 H=HAND128:IFH<>128 GOTO 30:REM IF D7=0 NOT READY
60 J=IAND15:  REM GET LS(4) BITS
70 V=PEEK(A):REM GET MS(8) BITS
80 V=V*16+J:V=V*R:REM MULTIPLY BINARY EQUIV.  X RESOLUTION=VOLTS(ABS)
90 X=10-V:VX=VX+X:NEXT LOOP:X=VX/20:REM AVERAGE
95 X=X*1E3:X=INT(X):X=X/1E3:REM WE ONLY WANT 3 DIGIT FRACTION
100 PRINTCHR$(13);TAB(5);X;TAB(13);"VOLTS";:REM DISPLAY VOLTAGE
110 VX=0:GOTO25:REM CLEANUP AND RESTART
```

574 I/O Assignment

WO-$C70F - DAC2 LOW 4 BITS

WO-$C70E - DAC2 HIGH 8 BITS + WORD STROBE

WO-$C70D - DAC1 LOW 4 BITS

WO-$C70C - DAC1 HIGH 8 BITS + INTENSITY OUTPUT + WORD STROBE

WO-$C70B - 6 BIT I/O OUT

WO-$C70A - CONTROL REGISTER (MUX., INT., BITS)

RO-$C709 - ADLOW - 4 BITS + FLAG = $3T^2L$ INPUTS

RO-$C708 - ADHIGH - 8 BITS + (RESET UPDATE CONTROL)

	7	6	5	4	3	2	1	Ø	
$C709	1=VALID A/D DATA	IO1N6	IO1N5	IO1N4	AD3	AD2	AD1	ADØ	STATUS/DATA REGISTER
$C708	AD11	AD1Ø	AD9	AD8	AD7	AD6	AD5	AD4	DATA REGISTER
$C70A	Ø=8 BIT 1= 12 BIT CONVERSION	1 ENINT	Ø=FLAG ENABLE	X X	MD MD	MC MC	MB MB	MA MA	CONTROL REGISTER

$C708 = 5Ø952

$C709 = 5Ø953

$C70A = 5Ø954

$C70B = 5Ø955

$C70C = 5Ø956

$C70D = 5Ø957

$C70E = 5Ø958

$C70F = 5Ø959

Applications Information

D/A Converters

The Digital to Analog converters are high speed devices capable of FSR swing in under one usecond settling to .Ø1% FSR in two useconds. This includes switching, slewing, and settling time. In most cases, the D/A converter speed will be limited only by the processing speed of the host computer. The loading of the output op-amps should be kept above 15ØØ ohms during normal operation. The output may be shorted to either supply rail or ground indefinitely without damage to the device.

A/D Converter

The A/D converter is a high speed, highly accurate successive approximation device.

As shipped from the factory the A/D will do approximately 66,ØØØ 8-bit and 28,ØØØ 12-bit conversions per second. If the application does not require exacting accuracy, the conversion rates may be increased several different ways. The following paragraphs may be used by the technically oriented user to customize the error vs conversion rate for his particular application if so desired.

The A/D converter is comprised of a 16-channel multiplexer, a sample and hold amplifier and the converter itself. The major factors in this sequence of analog acquisition are multiplexer switching time of 1.5 usec (if a new port has just been selected), the sample time of the S/H amp (8 usec @ .Ø1% error) and the actual A/D conversion rate. It can be seen that if any of these factors can be decreased the conversion rate will increase accordingly.

The most obvious way to increase throughput would be to delete the S/H amp entirely and decrease the timing components R85 and C25 to about 1 usec. This would also require a jumper from the sample and hold Pins 8 to 5 after removing the component.

Since the 12-bit conversion takes approximately 25 usec and the 8-bit approximately 5 usec, it can be seen that a dramatic conversion rate increase will be obtained, particularly in the 8-bit mode where the sample time is actually longer than the conversion time. Unfortunately, in most applications, the S/H will be required to prevent the converter from converting one voltage on the MSB's and an unrelated voltage on the LSB's, the error depending on the slew rate of the input vs the conversion rate of the A/D. This type of error can be quite large and is not a recommended tactic in most applications.

Another way to increase the conversion speed slightly less than the previous example but with good accuracy results would be to decrease the sample time allowed the S/H amp. As shipped, the S/H amp is adjusted to an 8 usec window which translates to .01% sample error. If a larger error can be tolerated, this can be adjusted to 6 usec for .1% error or 4 usec for 1% error. Four usec is about the minimum sample window that should be allowed as the percentage of error will increase dramatically with any further increase, unless the hold capacitor is reduced in size accordingly. Consult manufacturer's specifications for these values.

The previous methods are valid in the 8-bit and 12-bit mode. In the 8-bit mode the actual conversion time of the A/D itself may be adjusted. This would be accomplished by substituting the

crystal (X1) with another value. As shipped from the factory, this frequency is 3579545 Hz resulting in an 8-bit conversion time of 5 usec. The maximum recommended substitution would be 4.5 MHz resulting in 4 usec conversion time and an increase in error rate of approximately +/-½LSB.

The convert command one shot (U4H) 8ØØ nsec pulse is used to insure that the sample to hold transient of the sample/hold amp has settled and in no case should this be adjusted below 8ØØ nsec. In applications where the ambient temperature approaches or exceeds 5Ø°C, it may be beneficial to increase this time to 1.2 usec.

As can be seen from the previous discussion, trade offs can be made to increase the speed of data acquisition if slightly more error can be tolerated. Conversely, if greater accuracy is desired, conversion rates can be sacrificed to decrease the error. Although in most applications the 574 is already optimized as shipped from the factory. The sample "window" could be increased with about 1Ø usec giving the highest degree of accuracy and a 2 MHz crystal substitution for (X1) would increase converter accuracy to its highest capabilities, but resulting in conversion times of 9 usec + 1Ø usec + 8ØØ ns = 19.8 usec. The resulting accuracy improvement in most applications would not be required.

Scaling

The ADC8Ø input and DAC8Ø outputs should be scaled as close to the maximum signal range as possible in order to utilize the maximum signal resolution of the converters.

It is recommended that output voltage ranges -1Ø to +1ØV and Ø to +1ØV not be used if the supply voltages are ever less than the recommended ±12V. The output amplifier may saturate if Vsupply -Vout > 2.ØV. Refer to Figure 1 for possible scaling ranges and procedures. The 574 is factory configured for (CØB) code +/-1ØV.

Digital Input Codes

Three binary codes are available on the 574 analog interface. They are complementary (logic "Ø" is true), straight binary (CSB) for unipolar input signal ranges, and complementary two's complement (CTC) and complementary offset binary (COB) for bipolar input signal ranges.

Binary		Voltage Range and LSB Values				
Voltage Range	Defined As	+/-1ØV	+5V	+/-2.5V	Ø to 1ØV	Ø to +5V
Code		COB or CTC*	COB or CTC*	COB or CTC*	CSB**	CSB**
One Least Significant Bit	$FSR/2^N$	$2ØV/2^N$	$1ØV/2^N$	$5V/2^N$	$1ØV/2^N$	$5V/2^N$
	N=8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	N=12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values						
ØØØ...ØØØ***	+Full Scale	+1ØV-3/2LSB	+5V-3/2LSB	+2.5-3/2LSB	+1ØV-3/2LSB	+5V-3/2LSB
Ø11...111	Mid Scale	Ø	Ø	Ø	+5V	+2.5V
111...11Ø	-Full Scale	-1ØV+1/2LSB	-5V+1/2LSB	-2.5+1/2LSB	Ø+1/2LSB	Ø+1/2LSB

*COB = Complementary Offset Binary
**CSB = Complementary Straight Binary
*CTC - Complementary Two's Complement. Obtained by using the complement of the most significant bit.

***Voltages given are the nominal value for transition to the code specified.

Figure 1.

A/D Converter Ranges

Input Range	Code	W3Ø	W31	W27	W28	W29
+/-1ØV*	*COB or CTC	X			X	
+/-5V	COB or CTC		X		X	
+/-2.5V	COB or CTC		X	X	X	
Ø to +5V	CSB		X	X		X
Ø to +1ØV	CSB		X			X

X = Jumper: All others should be unconnected.
*As shipped from Factory.
Refer to Sheet 2 of Schematics.

Figure 2.

D/A Converter Ranges

Range	Code	Pin 6 Op Amp	Pin 17 D/A	Pin 19 D/A
+/-1ØV*	*COB or CTC	19 D/A	15 D/A	6 OP-AMP
+/-5V	COB or CTC	18 D/A	15 D/A	N.C.
+/-2.5V	COB or CTC	18 D/A	15 D/A	15 D/A
Ø to +1ØV	CSB	18 D/A	21 D/A	N.C.
Ø to +5V	CSB	18 D/A	21 D/A	15 D/A

*As shipped from Factory.
Refer to Sheet 3 of Schematics.

Figure 3.

Digital I/O

The CA-22 as delivered by the factory has a 6-bit digital output port and a 3-bit digital input port. Both are TTL compatible and may be used in applications requiring logical control or enabling of a device to which the CA-22 is interfaced. If more than three input lines are required or if the signal is not (TTL) compatible and all 16 multiplexed analog inputs are not required in the application, they may be used to 'read' those digital inputs. The absolute maximum input rating (+/-25V) of the multiplexer must be observed in this case.

The 6-bit output port is configured by the factory as TTL compatible. The user may reconfigure this to several different modes of interfacing. Ø.7V to +12V interfacing may be accomplished by cutting W-23 and jumpering W-24 or .7 to 3ØV open collector by cutting out R49-R54. The 74Ø6 open collector driver is capable of sinking 4Ø MA and will tolerate a high level output voltage up to +3ØV.

The 6-bit output port may be expanded to 8-bit by populating the prototyping area of the CA-22 if required.

Refer to the software section for Digital I/O techniques of these two ports.

Note that the 6-bit output port is inverted data. U1D may be substituted with a 74Ø7, 7417 or equivalent part if necessary to change to true data.

X-Y Oscilloscope Plotting

An oscilloscope with an X-Y plotting function and intensity input may be used for visual display of the X-Y outputs of the two DACs on the 574. U1C (Sheet 3) is used to control the intensity of the beam.

The interface should be used such that DAC'2 then DAC'1 are updated in that sequence. When DAC'1 is updated U1C Pin 12 one-shot is fired which will be the approximate settling time of DAC'1. After this period U1C Pin 13 is fired and is used to (unblank) the oscilloscope beam. This signal is factory configured for low true blank (positive logic). If your oscilloscope requires high true blank, cut W-39 and jumper W-40. R32 may be used to vary the "unblank" period but in some applications C15 and/or R34 may need optimization by the user for his application or scope persistence.

Adjustments

Although calibration with lower resolution equipment is possible, a 4½ digit D.V.M. should be used for the following procedures.

D/A Offset Adjustments

For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the offset potentiometer for zero output.

For bipolar (COB,CTC) configuration, apply the digital input code that should produce the maximum negative output voltage and adjust the offset potentiometer for that voltage.

D/A Gain Adjustments

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output for the range you have configured. Adjust the gain potentiometer for this positive full scale voltage. Since the gain and offset adjustments affect each other, this procedure may have to be repeated several times to get the best results.

A/D Offset Adjustment

Sweep the input through the end point transition voltage that should cause an output transition to all ones. Adjust the offset potentiometer R4 until the actual end point transition voltage occurs at E off/on. The ideal transition voltage values of the input are given in Figure 1.

A/D Gain Adjustment

Sweep the input through the end point transition voltage that should cause an output transition to all zeros. Adjust

the gain potentiometer R3 until the actual end point transition occurs at E on/off. Figure 1 details the transition voltage levels required.

R6Ø has been provided to facilitate sweeping the analog input voltage during these adjustments.

Since the gain and offset adjustments affect each other, this procedure may have to be repeated several times to get the best results.

Analog to Digital Data Acquisition

The ADC is a successive approximation type converter which requires no software overhead during the conversion process. Data acquisition is accomplished in the following manner. Port selection (1 of 16), conversion resolution (8 or 12-bit) and flag/no flag are selected by the user by a write to $C70A which is decoded as (/FORMAT). This 'word' is latched into U2C which controls the 'format' of the data acquisition. MA-MD select the proper port through the multiplexers U1A and U2A. R1 and R2 prevent excessive current flow through the multiplexer in an overvoltage situation. The absolute maximum input should be kept less than +/-25 volts. D1 and D2 prevent more than +/-.75V of the rails of the analog supply voltage grom being applied to the sample and hold (S/H) amplifier. R11 and R12 form the offset adjustment network. R5 controls the percentage of adjustment capability of the gain network R5, R6, R7 and R3. C11 prevents noise from being injected into the gain input. C31, C28, C30, C29, C13, C14, C4, C3, C29, C28, C10 and C8 are for power supply decoupling and high frequency filtering. C12 is the hold capacitor of the S/H.

A typical cycle involves the following. The one shot U4H causes the S/H to switch to the sample mode for 8 usec. At the end of this period the S/H is switched to HOLD and the one shot U4H Pin 5 is triggered. On the trailing edge of this delay (sample to hold transient settling time) the convert command is generated. At the end of the convert cycle (STATUS) generates

a new sample and the cycle continues. Until the next (CONV) command data is available at (AD11-ADØ) and on the first (Ø2) the data is latched into the 12-bit buffer U3B and U3A Sheet 1 by setting U4E Pin 5 (EOC) and U4F Pin 5 (VDF) high which are gated through U4G Sheet 1.

This 12-bit buffer will be updated at the completion of every converter cycle unless (FLAG) is high indicating the program has just read the LS(4) bits and flag at $C7Ø9 (/RL). Unable to update the 12-bit buffer at this time the converter will initiate a new cycle so that 'fresh' and updated information will be available after the program reads the MS(8) bits by reading $C7Ø8 (/RH) and reseting the flag register U4F.

When a new (FORMAT) is generated it must also be assumed that a new port has also been selected. When this occurs a new sample is forced by (/SAMPLE) U5F Pin 8 through U4G Pin 13. (/SAMPLE) also holds the valid data flag circuitry in the reset state so that when the present cycle is completed (VDF) will not be generated which would enable (FLAG). Since the S/H amp has been switched to sample the present conversion is invalid. At the end of this cycle U5F Pin 8 will be reset and at the end of the next cycle which will contain valid data (VDF) may be generated. If the cycle finishes after the sample time, the (CONV) command will be generated by the converter itself through U4F Pin 6 and the end of conversion latch U4E Pin 6. If the cycle finishes before the sample time the converter will stop and the (CONV) command will be generated by the end of the sample one shot period U4H Pin 4. This prevents wasting

up to 25 usec after a (/FORMAT) command before a sample could be taken.

The converter has an internal clock reference that is used in the 12-bit mode. In the 8-bit mode an external clock is provided by the crystal reference X1 and U5E and the internal clock must be switched off by (/8BIT) clock inhibit. U4E Pin 9 is used to sync the external clock to the convert command and divide the clock by two resulting in a 50% duty cycle. The conversion rate can be found by 1/((X1/2)/(BITS+1)). Where X1 is the crystal frequency in hertz, BITS equals number of bits of conversion (8). The 8-bit mode is accomplished by enabling the short cycle feature of the converter at Pin 21. Ten bit conversions could be done by connecting U4C Pin 9 to U2B Pin 28 instead of U2B Pin 30.

Digital to Analog Conversion

Refer to Sheet 3 of schematics. Since both DAC's are identical only DAC'1 will be discussed. A 12-bit word is written to the DAC in the following manner. The LS(4) bits are first written to U4B and strobed by (/DA1L) which was decoded by U5G Sheet 1 as a write cycle to $C70D. Notice that the 12-bit word latched in the 12-bit buffer U4A and U5C is not changed. Therefore, there is no change in the DAC output. To complete the 12-bit write the MS(8) bits are then written to $C70C which is decoded as (/DA1H). During this write cycle the MS(8) bits are presented by the CPU and the LS(4) bits are presented by U4B to the 12-bit buffer. At the end of

this write cycle the full 12-bit word is latched into the 12-bit buffer and presented to the DAC and the corresponding output change, if any, will be output. It can be seen from this discussion that a true 8-bit mode is inherently present and available. If U4B is first initialized to a predetermined offset or ØV, the MS(8) bits of the 12-bit buffer can then be changed at will with no change in the LS(4) bits as long as no writes are done to $C7ØD after software initialization.

R82 is required in applications using supplies under +/-15 volts to supply the necessary current for the internal reference of the DAC at Pins 24 and 16 of U5B. C31, C32, C4Ø, C39, C48 and C45 are for power supply decoupling and high frequency filtering. C55 and R93 form a compensation network in the op-amp circuit. R76 in the offset circuit is used to increase the resolution of the offset pot R65. R59 is not installed but may be used in conjunction with a resistor installed at W53 after cutting W53 to form a voltage scaling network. In most cases the output should be scaled using the information given in other sections of this manual. R8Ø controls the percentage of gain adjustability of the network R72, R71, and R80. Increasing R8Ø increases the percentage of adjustability. C47 prevents noise from being injected into the gain adjust input.

Accessory Bus C4P-MF, C8P-DF

Interfacing the CA-22 to the accessory bus on the back of your computer is accomplished by connecting a 16-pin ribbon cable from J5 of the CA-22 to J2 of the accessory bus "HEAD END CARD INTERFACE" on the back panel of the computer. If J2 is presently used to interface to another "HEAD END CARD", a CA-2Ø may be used to facilitate multiple accessory interfacing or the CA-22 could possibly be installed inside the computer's card cage and directly connected to the standard 48 line bus. If installed on the standard bus in a C8P-DF, the CA-22 must be readdressed to prevent bus contention with the present accessory bus on the 5Ø5B based computer. Refer to standard bus installation in this case. To configure the CA-22 for the accessory bus the following must be done:

Install	Delete/Remove
C17-C22	U1F
U2D	U2E
U3E	U5I
U3F	U6G
	U6F
	U6E

Refer to Block 'A' Sheet 1 of schematics and the CA-22 assembly diagram. C17-C22 must be installed if they have been removed in a previous configuration. Refer to the power supply requirements section for powering the CA-22 in this configuration.

The CA-22 as delivered from the factory is already set up in this configuration. Each of the above modifications should be

checked before installation anyway. Refer to Figure 4 or Figure 5 for the correct installation of the ribbon cable for accessory bus interfacing.

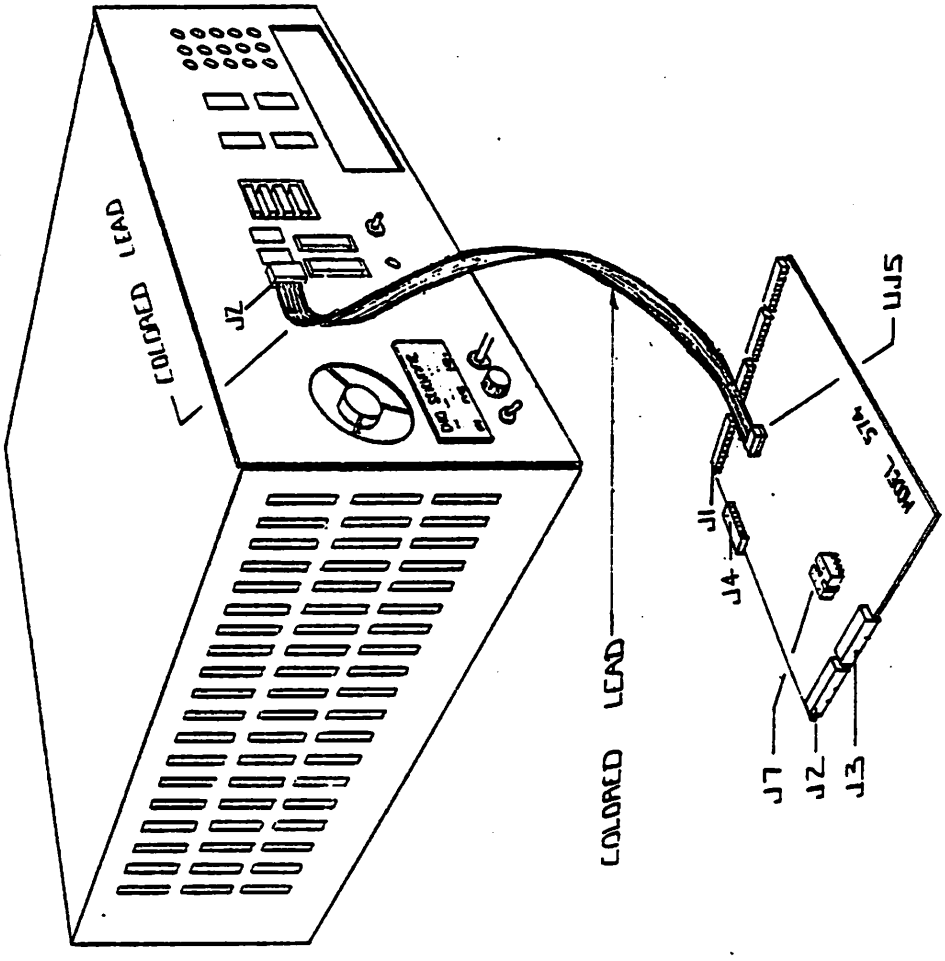


Figure 4.

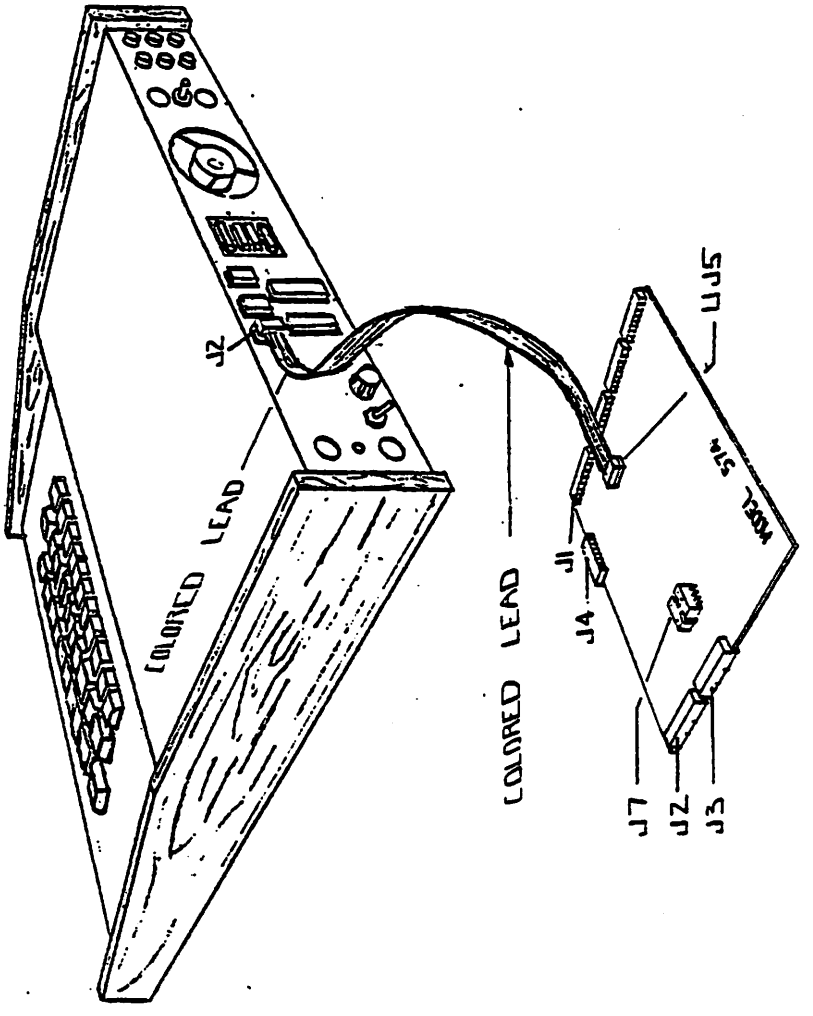


Figure 5.

48-Pin Motherboard Bus Installation Backplane

Interfacing to the 48-pin bus is accomplished by performing the following. Refer to Block 'B' Sheet 1 of schematics and the CA-22 assembly diagram.

Install	Delete/Remove
U1F	C17-C22
U2E	U2D
U5I	U3E
U6G	U3F
U6F	
U6E	

The three I.C. (integrated circuits) can be removed with a small screwdriver or similar instrument. Alternately pry up on each end (short end with no pins) of the package until it has been "rocked" out of the socket. Be sure that the screwdriver is placed between the package and the socket and not between the socket and the printed circuit board. You should find this to be a very simple operation. C17-C22 must be removed by desoldering or cutting them out with side cutters. The latter is recommended to prevent damage to the board. Installing the six I.C. packages is very simple. Each I.C. has an indentation on one end in a "U" shape. Refer to the CA-22 assembly diagram and install these packages as illustrated. When installing these I.C. packages be very certain that all pins are inserted into the socket. It is possible to bend a pin under the package and it is very difficult to see that this has happened.

Refer to power requirements section for powering the CA-22 in this installation.

CAUTION: Remove power from the computer before proceeding with the following steps. Remove the screws that fasten the cover to the computer, then carefully remove the cover and set aside. On some C2-C3 systems the Molex power connector to the muffin fan(s) must be disconnected before complete removal of the cover. Find a free slot in your card cage to install the CA-22. Install on the standard bus taking great care to align the pins of the CA-22 exactly as required and be certain that the component side of the CA-22 faces in the same direction as the other boards (toward the front). Installation of the CA-2Ø to the standard bus of the C4P-MF and C4P-DF (not recommended) or C8P-DF which are 5Ø5 Rev.B (CPU) based requires that the accessory bus interface on the 5Ø5 Rev.B. be disabled. This is very important since improper operation of the CA-2Ø and/or the accessory bus will be experienced if not done. Remove the 5Ø5 Rev.B from the card cage. Pay close attnetion (a quick sketch would be helpful) to any connectors that may have to be removed to get the 5Ø5 Rev.B in a suitable position for the following actions. Refer to the assembly drawing in the 5Ø5 Rev.B schematics and remove the two integrated circuit packages U4H and U3G. These two packages should be labeled (8T26 or 75136).

Alternately the accessory bus on the 5Ø5 Rev.B could be readdressed moving the enable line from U5J Pin 15 to U5J Pin 14 ($C6XX). This is not recommended since this is an OSI reserved address block and could possibly cause problems if any upgrades are ever added to your system. Also the type of modification should be left to an experienced technician with the proper tools and knowledge.

When this is completed re-install the 505 Rev.B in the computer taking care to replace any connectors previously removed in the exact locations noted before.

Installation in 510 (CPU) based systems is accomplished by simply connecting the CA-22 to the standard bus since there is no present accessory bus in these systems. The exception would be the case of a CA-20 already installed. In this case refer to the CA-20 manual for proper installation.

If the power supply requirements have already been met and the proper I/O connections to the CA-22 are installed then the cover of the computer should be re-installed at this time in the reverse order of removal making sure any ground straps or fans are reconnected. Refer to the power requirements section if not completed at this time.

WARNING: If a CA-12 (96 line interface) has been installed in your system either the CA-12 or the CA-22 must be readdressed to prevent bus contention problems. Alternatively the "HEAD END CARDS" could be connected to a CA-20 for multiple accessory bus interfaces.

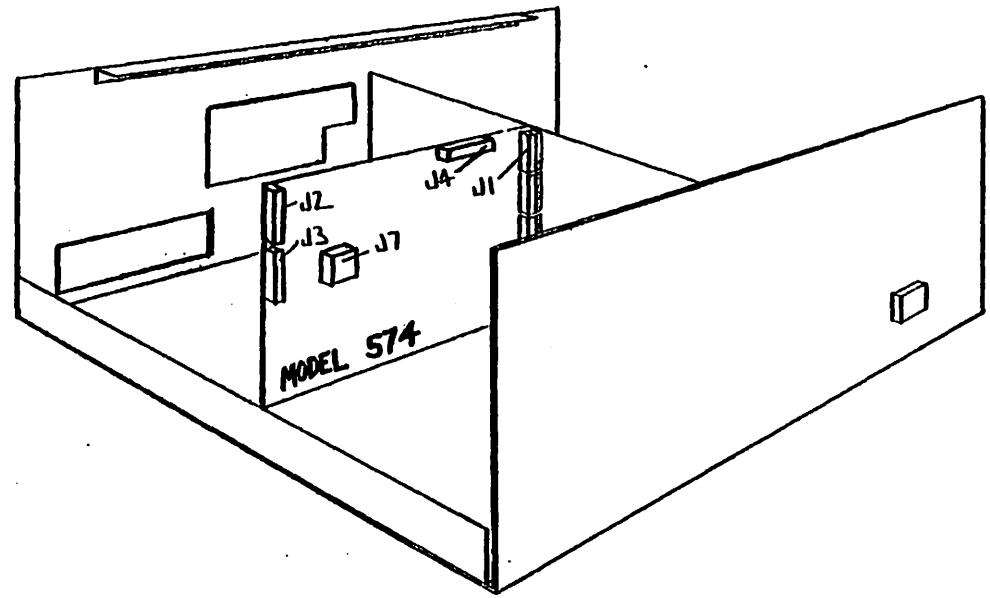


Figure 6.

Power Requirements

	+5V	± 5%	@ 750 MA
	+11.4V to +16V	± 1%	@ 100 MA
(1)	-11.4V to -16V	± 1%	@ 100 MA

(1) The negative voltage may be substituted with an unregulated negative D.C. voltage if connected as described in the power connections section.

Power Connections

The following section describes the power connections that must be wired to the CA-22. This type of operation is very critical to the board because faulty wiring or power supply connections could cause serious damage to the delicate electronics of the board. For this reason it is advised that only qualified personnel attempt the following actions. The warranty could possibly be voided if this is not done.

The CA-22 requires three voltages for proper operation (listed above). In most cases all three of these should be provided by the user via auxiliary power supplies. The exception is when the CA-22 is installed inside the computer's card cage and connected directly to the standard OSI 48 line bus. In this configuration the +5V and +12V are provided by the system power supplies and no further connections are required except for the -12V voltage. When the system power is used to supply the positive voltages, care should be taken to insure that the maximum capacity of the system supply is not exceeded. Connecting the minus supply is described later.

For installations where the CA-22 is installed as a "HEAD END CARD" the three supplies could be provided several ways. A connector on the CA-22 is provided to facilitate the connection

of these voltages. Any leads of this connector (J7) that are not used must be taped or cut off to prevent them from shorting.

+5V + 5% @ 750 MA

The +5V can be routed to an auxiliary supply or to the system supply. This connection should be from J7 Pin 1 or 2 to the positive 5 volts. Two connections are provided so that the user may 'daisy chain' the supply if multiple "HEAD END CARDS" are being installed. The extra lead should be taped or cut off if not used. A ground return must also be connected to the auxiliary supply or the system ground depending on your installation. The digital reference (ground) for this type of installation (accessory bus) is provided through the 16-pin ribbon cable. Refer to the CA-22 schematics (574) Sheet 4.

+11.4V to +16V + 1% @ 100 MA

Although the positive and negative voltage supplies of the CA-22 can be anywhere in the range of the above specifications, they should track. That is, if positive 12 volts is used then negative 12 volts should be used. If the -10V to +10V FSR (full scale resolution) of the board is to be used then the supplies must be at least plus and minus 12 volts. The positive voltage (+12V) J7 Pin 6 should be connected to an auxiliary positive supply or to the +12V supply in your system (if so equipped). The remaining ground wire from J7 must be connected to the system ground or the auxiliary supply ground depending on your installation. This wire must also be 'daisy chained' to the negative supply 'common'.

-11.4V to -16V + 1% @ 100 MA

The negative supply voltage can be obtained several different ways. Refer to Sheet 4 of the CA-22 schematics (OSI 574). Connector J7 Pin 5 is a direct connection to the -12V bus of the CA-22. If a negative regulated auxiliary supply is to be used then it may be connected directly to J7 Pin 5. If this is done the regulator (REG.1) must be removed from the board. The ground return of the negative supply must be connected to the ground of the CA-22. This completes the auxiliary regulated supply connections.

An unregulated negative supply voltage may also be used for the CA-22. This voltage can be from negative 15V to negative 35V absolute maximum and the source must have a current rating of at least 100 MA. This voltage must be connected to the input of the regulator (Pin 3 of REG.1). This can be done by a direct solder connection to the regulator input bus or by cutting the appropriate trace from J7 Pin 5 to the negative 12V bus and jumpering J7 Pin 5 to the input of the regulator. J7 Pin 5 could then be used to route the unregulated negative voltage to the board and then to the regulator. The unregulated supply could be an auxiliary supply or the unregulated negative voltage of the system power supply could be used. In the latter case, great case must be exercised.

On Board Supplies

The capability of on board D.C. to D.C. regulator mounting and interconnection is provided on the CA-22. Refer to Sheet 4 of the CA-22 schematics (OSI 574). The D.C. to D.C. regulator (PS3) could be installed to supply the +12V and -12V. If this is done the regulator (REG. 1) must be removed from the board and

PS3 is installed and the CA-22 is mounted to the standard bus in a C8P-DF or similar computer with +12V on the motherboard then +12V connection to the backplane must be cut.

If the negative only D.C. to D.C. converter (PS1) is installed, then the +12V and +5V must still be supplied via the aforementioned methods and REG.1 must be left installed.

If either PSL or PS3 is installed then C9, C64 and C61A should be installed. In either case the +5V supply is used to drive the converters and must be accounted for when determining +5V current requirements.

CA-22 Board
OSI 574 I/O Pin Assignments

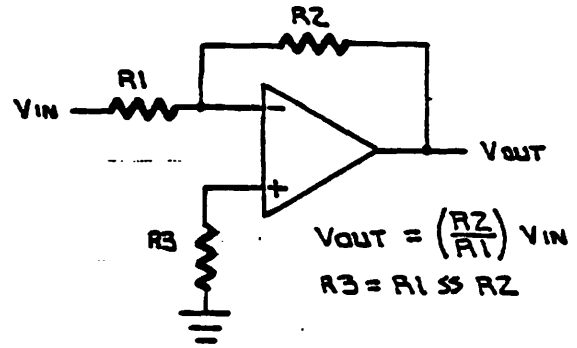
J2		J3	
1	AIN0	1	AIN8
2	AIN1	2	AIN9
3	GND	3	GND
4	AIN2	4	AIN10
5	AIN3	5	AIN11
6	AIN4	6	AIN12
7	GND	7	GND
8	AIN5	8	AIN13
9	AIN6	9	AIN14
10	AIN7	10	AIN15
11	GND	11	GND
12	DAC1	12	DAC2

J4		J6		J7	
1	GND	1	SPARE	J7-1	+5V
2	IOIN4	2		J7-2	+5V
3	IOIN5	3		J7-3	GND
4	IOIN6	4		J7-4	GND
5	/BLANKING	5		J7-5	-12V
6	IOUT0	6		J7-6	+12V
7	IOUT1	7			
8	IOUT2	8			
9	IOUT3	9			
10	IOUT4	10			
11	IOUT5	11			
12	GND	12			

AIN(N) = ANALOG INPUT PORT (N)
IOIN(N) = I/O INPUT BIT (N) DIGITAL, NEGATIVE LOGIC
IOUT(N) = I/O OUTPUT BIT (N) DIGITAL, NEGATIVE LOGIC

EXAMPLES OF CIRCUITS THAT COULD BE POPULATED ON THE CA-22

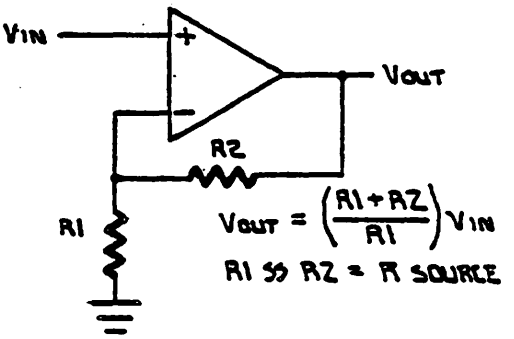
INVERTING AMPLIFIER



$V_{OUT} = \left(\frac{R2}{R1}\right) V_{IN}$

$R3 = R1 \,\$\$\, R2$

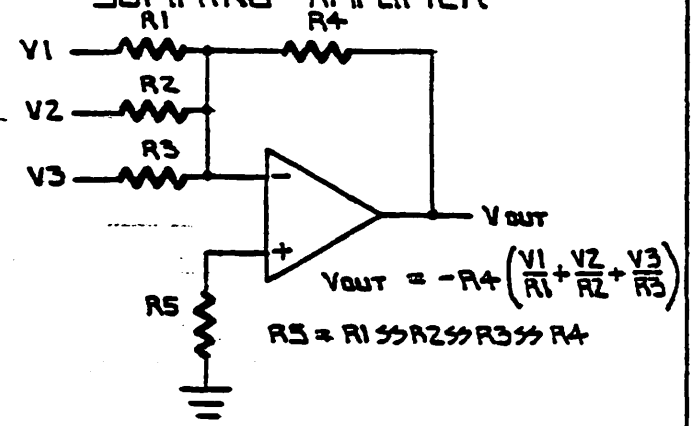
NON-INVERTING AMPLIFIER



$V_{OUT} = \left(\frac{R1+R2}{R1}\right) V_{IN}$

$R1 \,\$\$\, R2 = R$ SOURCE

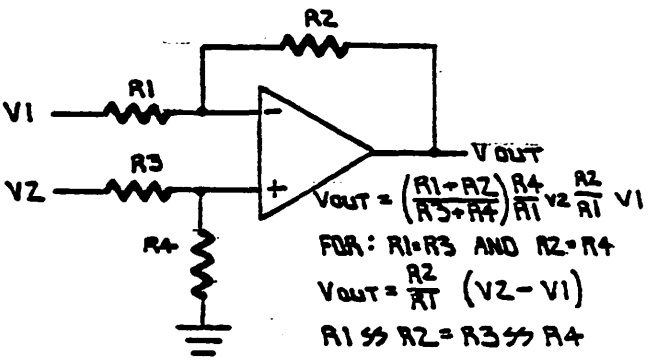
SUMMING AMPLIFIER



$V_{OUT} = -R4\left(\frac{V1}{R1}+\frac{V2}{R2}+\frac{V3}{R3}\right)$

$R5 = R1 \,\$\$\, R2 \,\$\$\, R3 \,\$\$\, R4$

DIFFERENCE AMPLIFIER



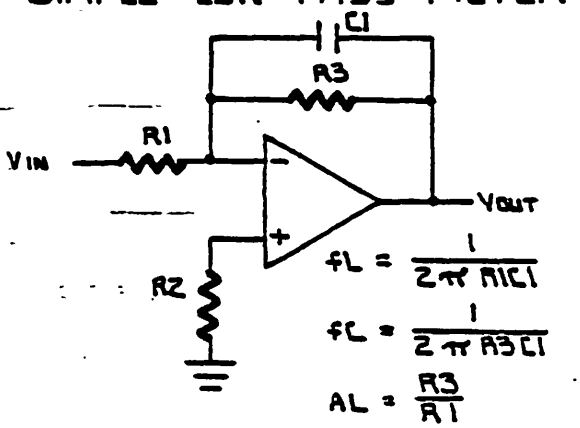
$V_{OUT} = \left(\frac{R1+R2}{R3+R4}\right)\frac{R4}{R1} V2 \frac{R2}{R1} V1$

FOR: $R1=R3$ AND $R2=R4$

$V_{OUT} = \frac{R2}{R1}(V2-V1)$

$R1 \,\$\$\, R2 = R3 \,\$\$\, R4$

SIMPLE LOW PASS FILTER

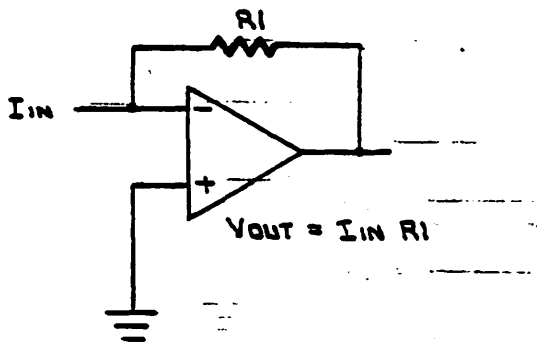


$f_L = \frac{1}{2\pi R1C1}$

$f_L = \frac{1}{2\pi R3C1}$

$A_L = \frac{R3}{R1}$

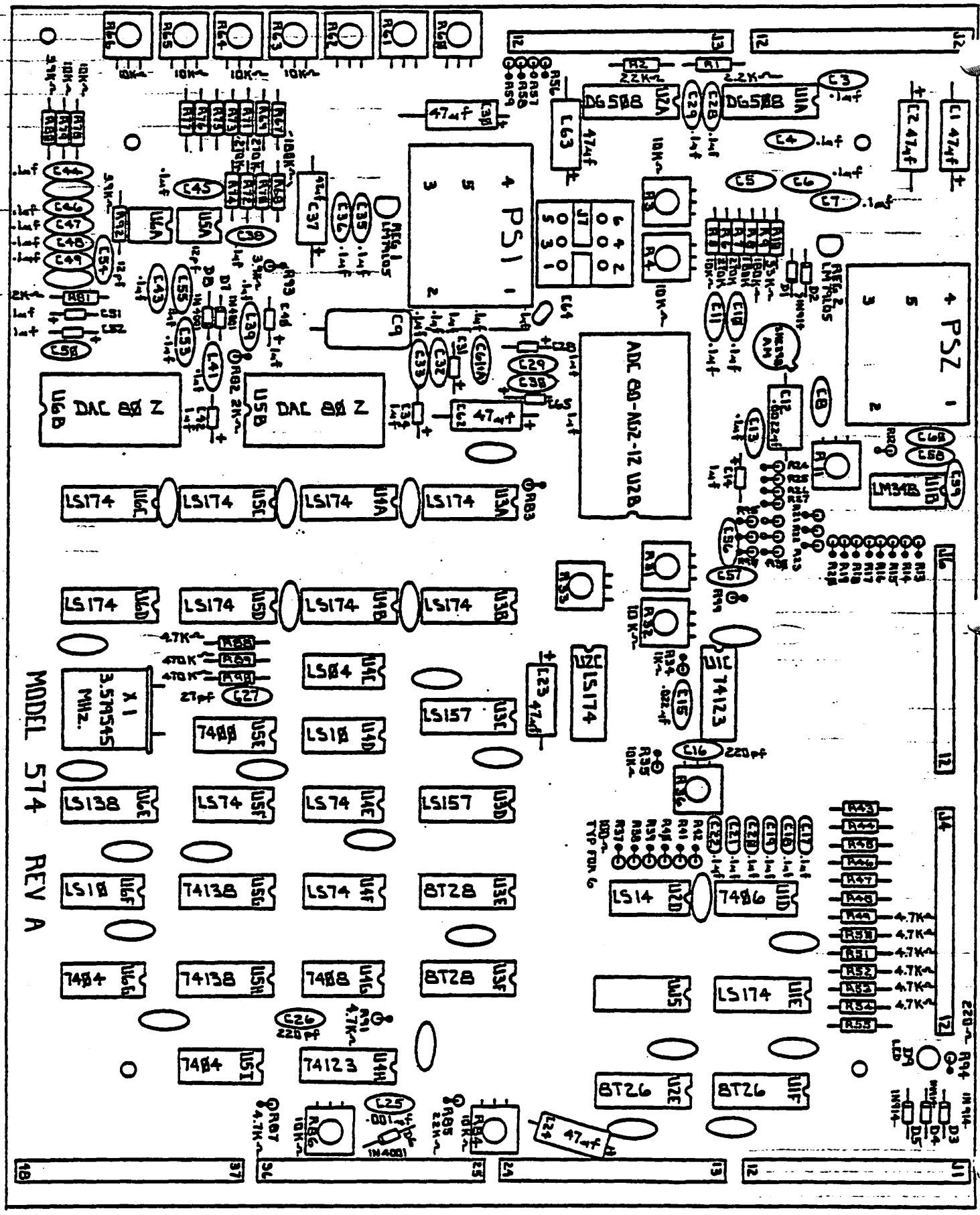
CURRENT TO VOLTAGE CONVERTER

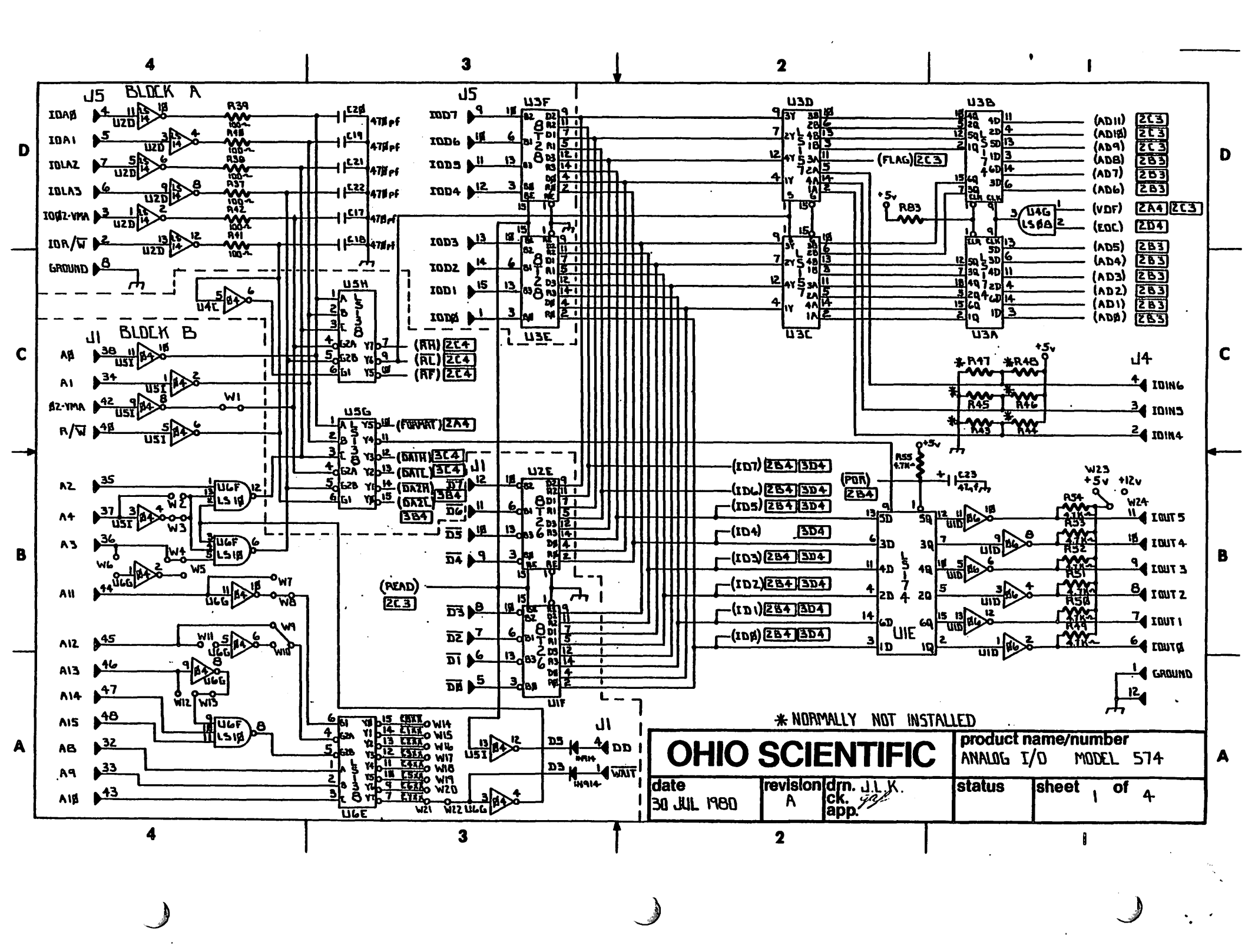


$V_{OUT} = I_{IN} R1$

$\$\$$ = PARALLEL RESISTANCE OF.

ALL UNMARKED CAPACITORS ARE .1uf BYPASS




J5 BLOCK A
IOA0
IOA1
IOA2
IOA3
IOØZ-VMA
IOR/W
GROUND
R39
R38
R37
R42
R41
C20
C19
C21
C22
C17
C18
47Ø pf
J1 BLOCK B
AØ
A1
ØZ-VMA
R/W
A2
A4
A3
A11
A12
A13
A14
A15
A8
A9
A10
W1
W2
W3
W4
W5
W6
W7
W8
W9
W10
W11
W12
W13
U5H
U5G
U6E
U6F
U6G
U5I
U4C
(RH) 2C4
(RL) 2C4
(RF) 2C4
(FORMAT) 2A4
(DATH) 3C4
(DATL) 3C4
(DAZH) 3B4
(DAZL) 3B4
(READ) 2C3
J5
IOD7
IOD6
IOD5
IOD4
IOD3
IOD2
IOD1
IODØ
U3F
U3E
U2E
U1F
D7
D6
D5
D4
D3
D2
D1
DØ
U3D
U3C
(FLAG) 2C3
+5v
R83
U3B
U3A
(AD11) 2C3
(AD10) 2C3
(AD9) 2C3
(AD8) 2B3
(AD7) 2B3
(AD6) 2B3
(VDF) 2A4 2C3
(EOC) 2B4
(AD5) 2B3
(AD4) 2B3
(AD3) 2B3
(AD2) 2B3
(AD1) 2B3
(ADØ) 2B3
U4G
J4
R47
R48
R45
R46
R43
R44
IOIN6
IOIN5
IOIN4
(ID7) 2B4 3D4
(ID6) 2B4 3D4
(ID5) 2B4 3D4
(ID4) 3D4
(ID3) 2B4 3D4
(ID2) 2B4 3D4
(ID1) 2B4 3D4
(IDØ) 2B4 3D4
(POR) 2B4
R55 4.7K
C23 47pf
U1E
W23
+5v
+12v
W24
R54
R53
R52
R51
R50
R49
IOUT5
IOUT4
IOUT3
IOUT2
IOUT1
IOUTØ
GROUND
U1D
J1
D5
D3
IN914
DD
WAIT
* NORMALLY NOT INSTALLED
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product name/number
ANALOG I/O MODEL 574
date
30 JUL 1980
revision
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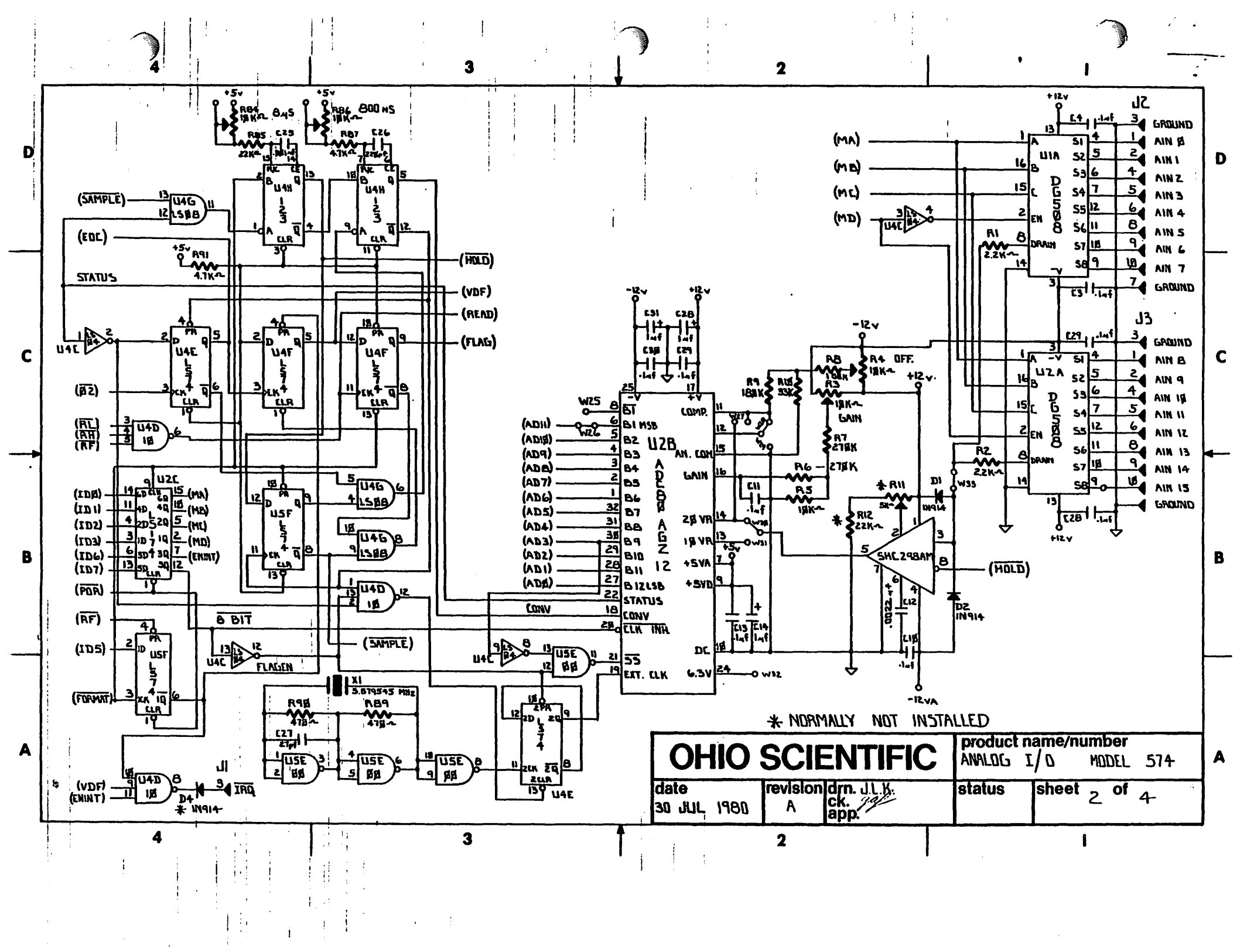
status
sheet 1 of 4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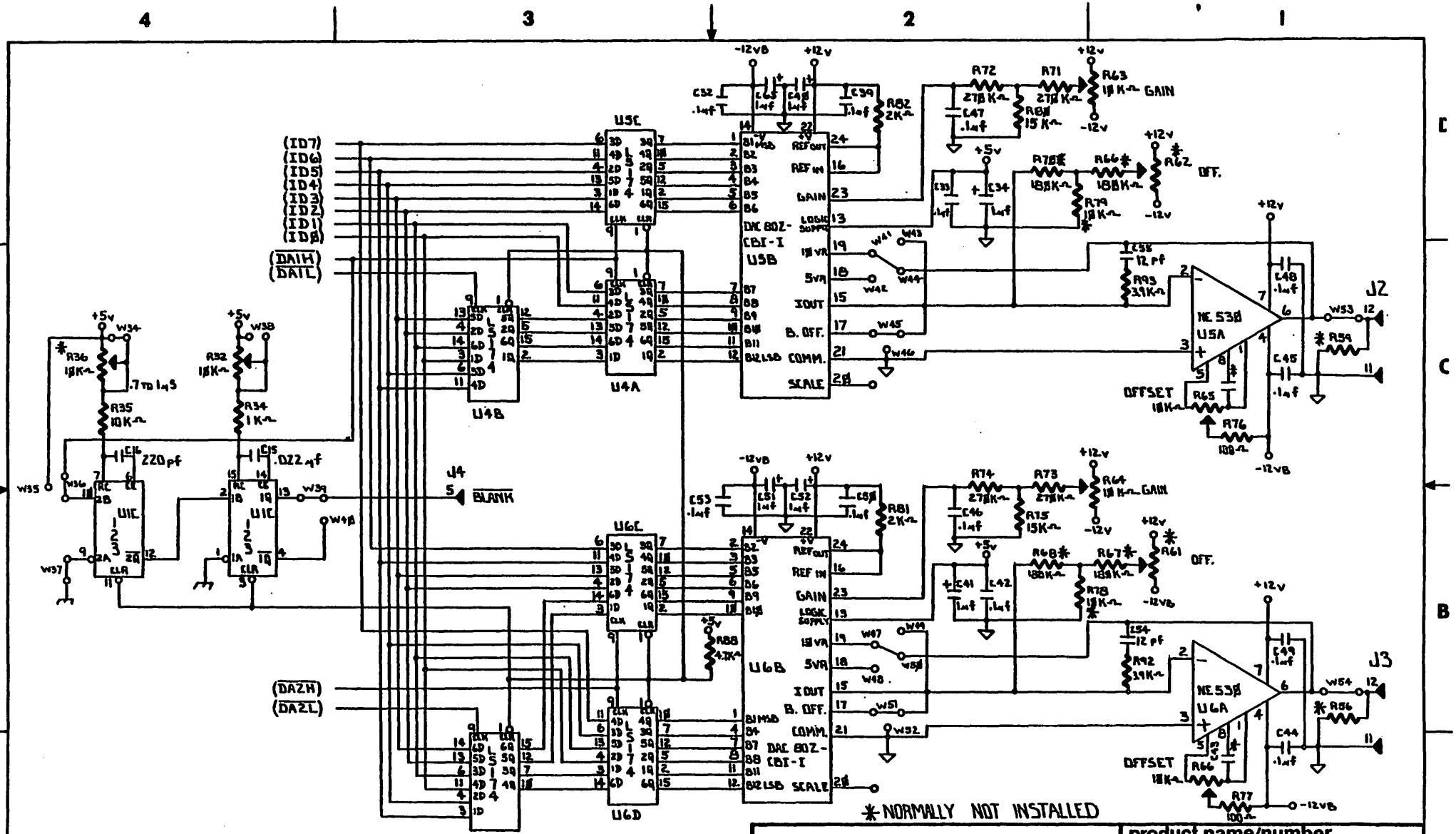
(ID7)
(ID6)
(ID5)
(ID4)
(ID3)
(ID2)
(ID1)
(ID0)
(DA1H)
(DA1L)
(DA2H)
(DA2L)
U5C
U4A
U4B
U5B
U6C
U6D
U5D
U6B
U1E
U1C
DAC 80Z-CBI-I
NE 538
U5A
U6A
OFFSET
GAIN
OFF.
BLANK
J4
J2
J3
R82 2K
R81 2K
R72 27.8K
R71 27.8K
R63 15K GAIN
R64 15K GAIN
R62 OFF.
R61 OFF.
R78 15K
R79 15K
R65 15K
R66 15K
R76 100
R77 100
R95 3.9K
R92 3.9K
R59
R56
R88 4.7K
R36 15K .7 TO 1.45
R32 15K
R35 10K
R34 1K
C52 .1uf
C53 .1uf
C47 .1uf
C46 .1uf
C58 12 pf
C54 12 pf
C48 .1uf
C49 .1uf
C45 .1uf
C44 .1uf
C16 220 pf
C15 .022 uf
W35
W36
W37
W38
W39
W40
W41
W43
W44
W45
W46
W47
W49
W48
W51
W52
W53
W54
+5v
+12v
-12vB
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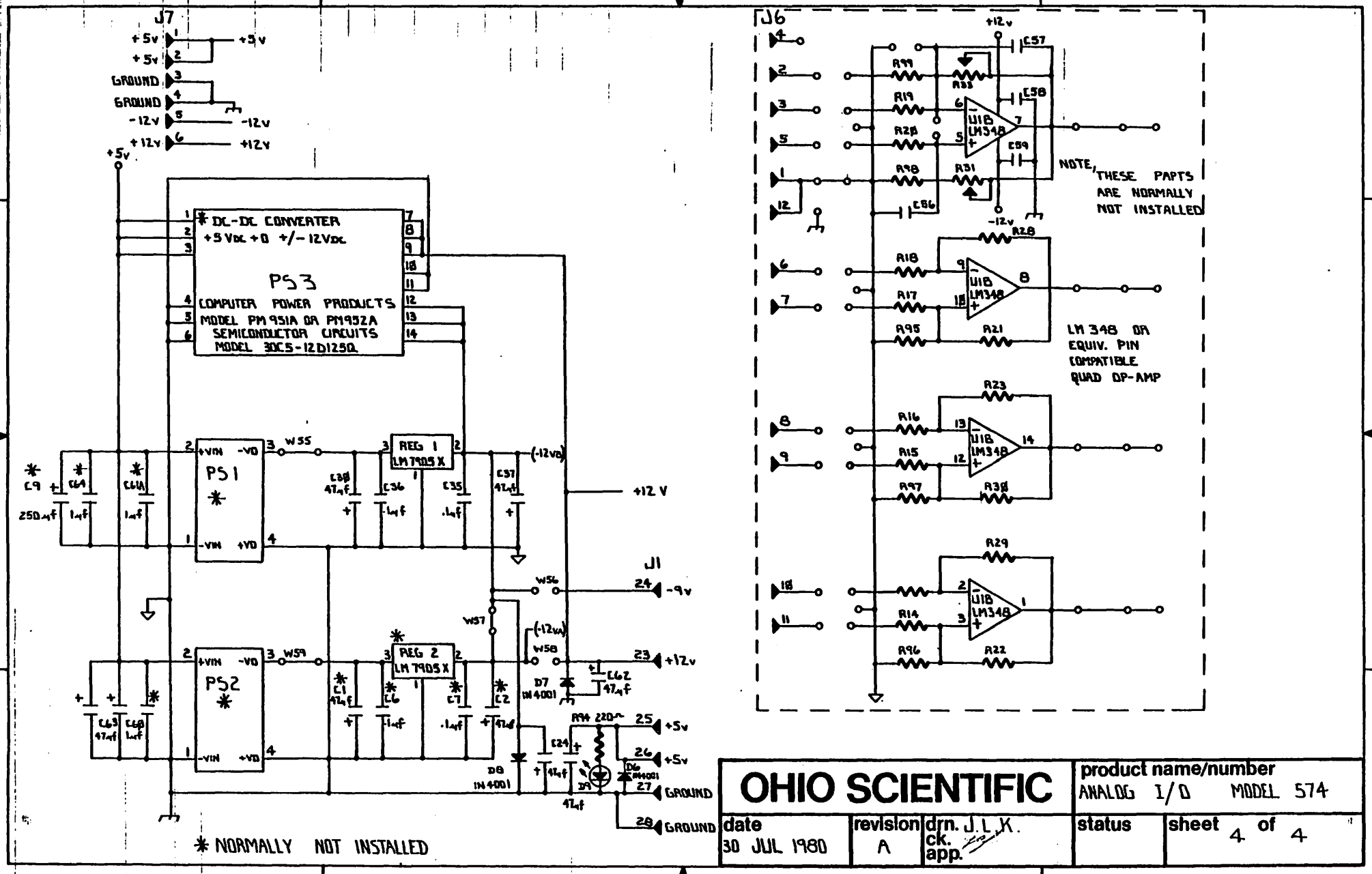

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date 30 JUL 1980	revision A	drn. J.L.K. ck. app.	status	sheet 4 of 4

BURR-BROWN

ADC80

IC ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- **COMPACT DESIGN - Self-contained with internal clock, comparator, and reference**

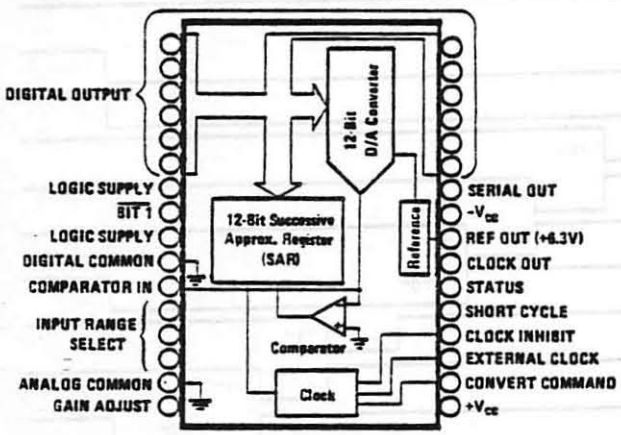
  32-pin ceramic package

- **FAST CONVERSION SPEEDS**
  Provide fast signal sampling rates
  12-bits - 25µsec, 10-bits - 21µsec
  Faster conversion speeds obtainable with "Short-Cycling" and optional external clock

- **LOW COST**

- **WIDE SUPPLY RANGE - Will operate with ±10.8V to ±16V supplies (Z models)**

FUNCTIONAL DIAGRAM



DESCRIPTION

The Model ADC80AG-10 and ADC80AG-12 are 10- and 12-bit successive approximation A/D converters. They utilize state-of-the-art IC and laser-trimmed thin-film components, and are packaged in a compact 32-pin ceramic package.

Complete with internal reference, the ADC80 offers versatility and performance formerly offered only in larger modular or rack-mount packages.

Thin-film internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V or 0 to +10V.

Gain and offset errors may be externally trimmed to zero, offering initial accuracies of better than ±0.0122% (±1/2LSB). The model ADC80 is specified for -25°C to +85°C operation.

The fast conversion speeds of 25µsec for 12-bit and 21µsec for 10-bit resolution make the ADC80 excellent for a wide range of applications where system throughput sampling rates from 40kHz to 47kHz are required. In addition, the ADC80 may be short cycled and an external clock may be used to obtain faster conversion speeds at lower resolutions.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are DTL/TTL-compatible. Two power supply ranges are available: ±15V and ±12V (Z models). A +5V logic supply is also required.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

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PDS-333F Printed in October, 1978

DISCUSSION OF PERFORMANCE

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent QUANTIZATION ERROR of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including GAIN, OFFSET, LINEARITY, DIFFERENTIAL LINEARITY and POWER SUPPLY SENSITIVITY. Initial GAIN and OFFSET errors may be adjusted to zero. GAIN drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits OFF) and OFFSET drift shifts the line left or right over the operating temperature range. LINEARITY error is unadjustable and is the most meaningful indicator of A/D converter accuracy. LINEARITY error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A DIFFERENTIAL LINEARITY error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB ±1/2LSB.

The ADC80 is also MONOTONIC, assuring that the output digital code either increases or remains the same for increasing analog input signals. A monotonic converter can have missing codes; therefore, Burr-Brown specifies no missing codes over a temperature range.

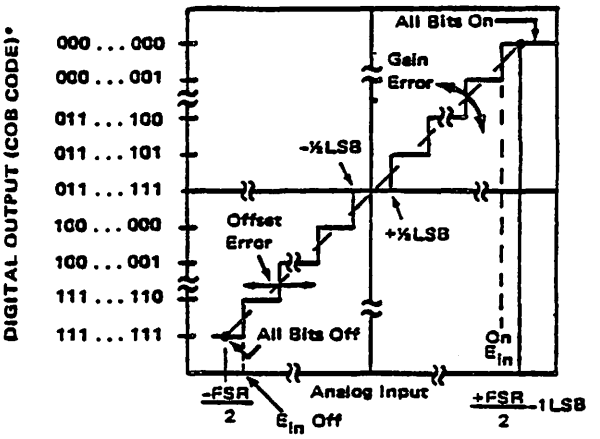


FIGURE 1. Input vs output for an ideal bipolar A/D converter.
*See Table I for digital code definitions.

TIMING CONSIDERATIONS

The timing diagram of the ADC80 (Figure 2) assumes an analog input such that the positive true digital word 10011000-1001 exists. The output will be complementary as shown in Figure 2 (011001110110 is the digital output).

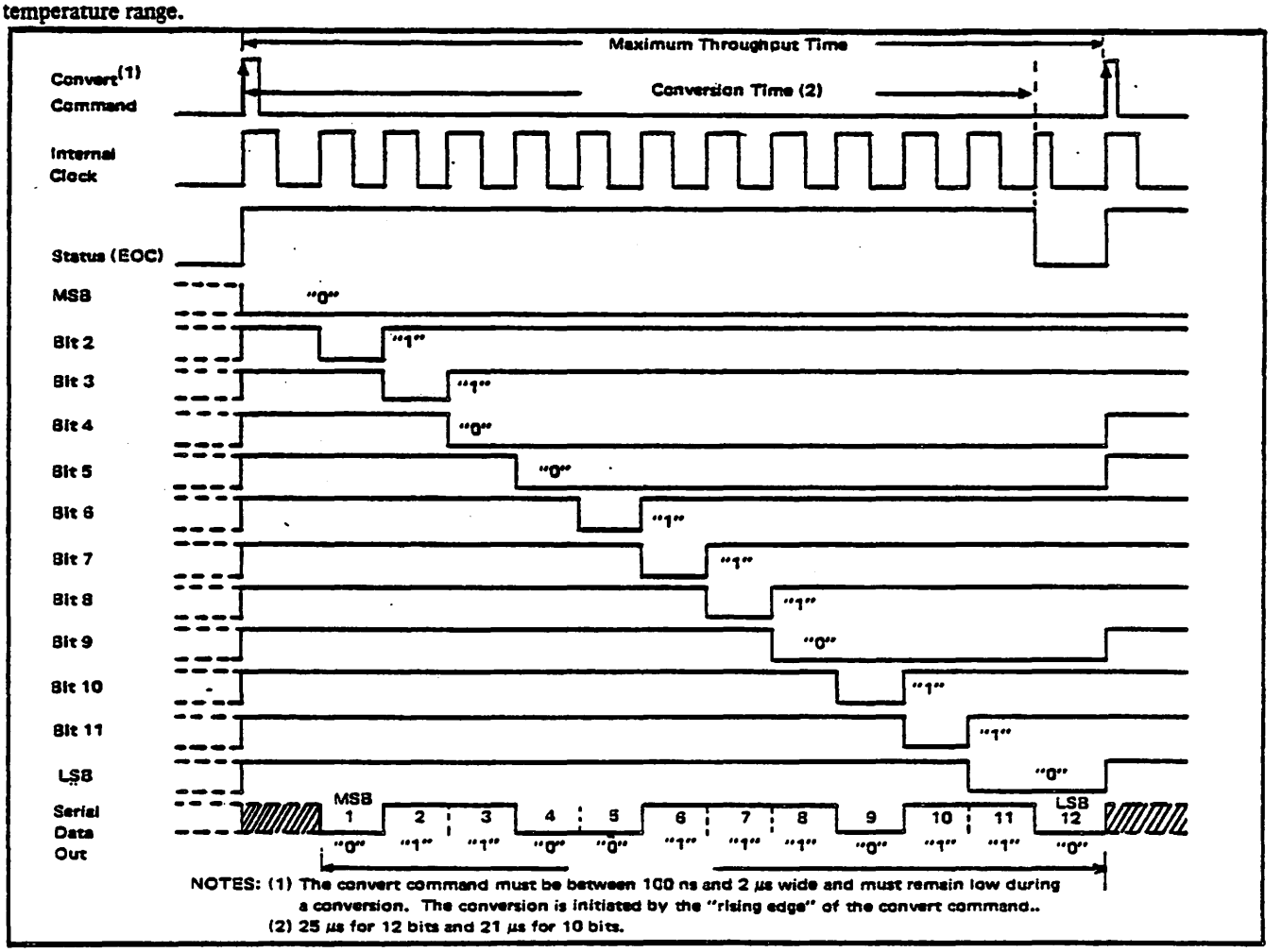


FIGURE 2. ADC80 Timing Diagram.

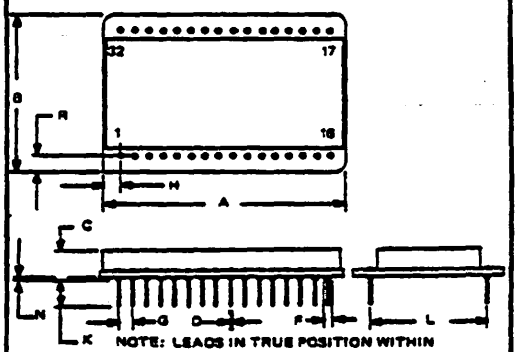
ELECTRICAL SPECIFICATIONS

Typical at 25°C and rated power supplies unless otherwise noted.

MODEL	ADC80AGZ-12 ADC80AG-12	ADC80AGZ-10 ADC80AG-10	Units
RESOLUTION	12	10	Bits
INPUT			
ANALOG INPUTS			
Voltage Ranges - Bipolar	±2.5, ±5, ±10		V
- Unipolar	0 to +5, 0 to +10		V
Impedance (Direct Input)			
0 to +5V, ±2.5V	2.5		kΩ
0 to +10V, ±5V	5		kΩ
±10V	10		kΩ
DIGITAL INPUTS[1]			
Convert Command	Positive Pulse 100ns Wide (min) 2μsec Wide (max).		
Logic Loading	1		TTL Load
External Clock	1		TTL Load
TRANSFER CHARACTERISTICS			
ERROR			
Gain Error[2,3]	±0.1		%
Offset Error[2,3] - Unipolar	±0.05		% of FSR[2]
- Bipolar	±0.1		% of FSR
Linearity Error (max)[4]	±0.012	±0.048	% of FSR
Inherent Quantization Error	±1/2		LSB
Differential Linearity Error	±1/2		LSB
No Missing Codes Temp. Range	0 to +50	0 to +70	°C
Power Supply Sensitivity			
±15V	±0.0030		% of FSR/%V,
+5V	±0.0015		% of FSR/%V,
DRIFT			
Specification Temperature Range	-25 to +85		°C
Total accuracy, bipolar (max)[8]	±23		ppm/°C
Gain, (max)	±30		ppm/°C
Offset - Unipolar	±3		ppm of FSR/°C
- Bipolar, (max)	±15		ppm of FSR, °C
Linearity, (max)	±3		ppm of FSR/°C
Monotonicity	GUARANTEED		
CONVERSION SPEED(max)[5]	25	21	μsec
OUTPUT			
DIGITAL DATA			
(all codes complementary)			
Parallel			
Output Codes[6] - Unipolar	CSB		
- Bipolar	COB, CTC		
Output Drive	2		TTL Loads
Serial Data Codes (NRZ)	CSB, COB		
Output Drive	2		TTL Loads
Status	Logic "1" during conversion		
Status Output Drive	2		TTL Loads
Internal Clock			
Clock Output Drive	2		TTL Loads
Frequency[7]	500		kHz
INTERNAL REF. VOLTAGE	6.3		V
Max. External Current (with no degradation of specifications)	200		μA
Tempco of Drift (max)	±20		ppm/°C
POWER REQUIREMENTS			
Rated Voltages	±15, +5		V
Z models	±12, +5		V
Range for Rated Accuracy	4.75 to 5.25 and ±14.0 to ±16.0		V
Z models	4.75 to 5.25 and ±10.8 to ±16.0		V
Supply Drain +15V or +12V	+20		mA
-15V or -12V	-20		mA
+5V	+70		mA
TEMPERATURE RANGE			
Specification	-25 to +85		°C
Operating (derated spec)	-55 to +100		°C
Storage	-55 to +125		°C
PRICES (1 - 24)	$82.50	$77.50	$
Z models	$84.50	$79.50	$

1. DTL/TTL compatible i.e., Logic "0" = 0.8V max, Logic "1" = 2.0V min for inputs and for digital outputs. Logic "0" = +0.4V max and "1" = 2.4V min.
2. FSR means Full Scale Range - for example, unit connected for ±10V range has 20V FSR.
3. Adjustable to zero with external trimpots.
4. Error shown is the same as ±1/2 LSB max for resolution of A/D converter.
5. Conversion time with internal clock.
6. See Table I. CSB - Complementary Straight Binary.
   COB - Complementary Offset Binary.
   CTC - Complementary Two's Complementary.
7. For conversion speeds specified.
8. Includes drift due to linearity, gain, and offset drifts.

MECHANICAL



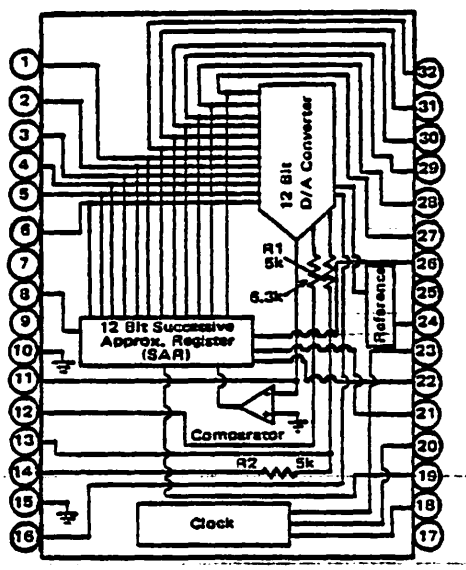
NOTE: LEADS IN TRUE POSITION WITHIN .010" (.25mm)R @ MMC AT SEATING PLANE.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.700	1.760	43.18	44.70
B	1.120	1.160	28.45	29.46
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.110	.130	2.79	3.30

PINS: Pin material and plating composition conform to method 2003 (Solderability) of Mil-Std-883 (except paragraph 3.2).
CASE: Ceramic
MATING CONNECTOR: 2302MC - Set of two 16-pin strips $7 per set.
WEIGHT: 13 grams (0.46 oz).

Connection Diagram

TOP VIEW



PIN CONNECTIONS

1. Bit 6	32. Bit 7
2. Bit 5	31. Bit 8
3. Bit 4	30. Bit 9
4. Bit 3	29. Bit 10 (LSB-10 Bits)
5. Bit 2	28. Bit 11
6. Bit 1 (MSB)	27. Bit 12 (LSB-12 Bits)
7. +5V Analog Supply	26. Serial Out
8. Bit 1 (MSB)	25. -15V or -12V (Z Models)
9. +5V Digital Supply	24. Ref. Out (+6.3V)
10. Digital Common	23. Clock Out
11. Comparator IN	22. Status
12. Bipolar Offset	21. Short Cycle
13. R1 10V Range	20. Clock Inhibit
14. R2 20V Range	19. External Clock
15. Analog Common	18. Convert Command
16. Gain Adjust	17. +15V or +12V (Z Models)

TYPICAL PERFORMANCE CURVES

FIGURE 3. Linearity error vs conversion time.

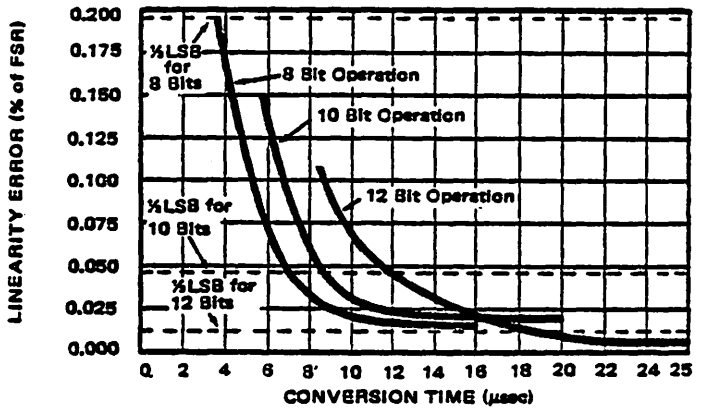


FIGURE 4. Differential linearity error vs conversion time.

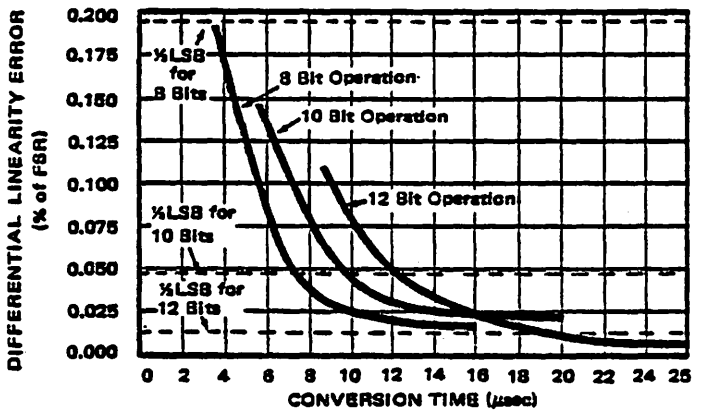


FIGURE 5. Gain drift error (% of FSR) vs temperature.

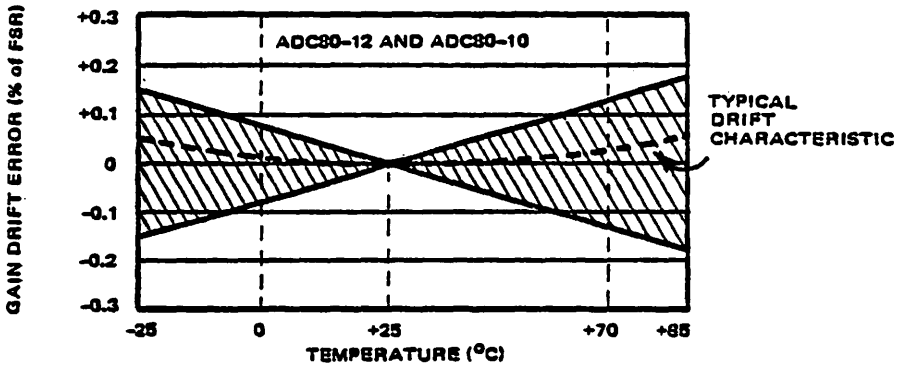
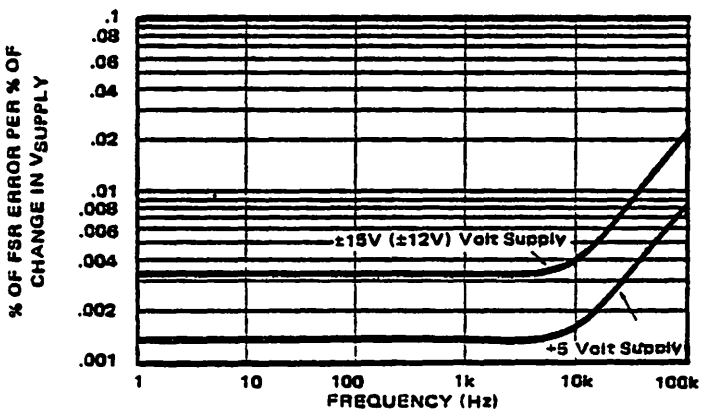


FIGURE 6. Power supply rejection vs power supply ripple frequency.



DEFINITION OF DIGITAL CODES

PARALLEL DATA

Three binary codes are available on the ADC80 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary two's complement (CTC) and complementary offset binary (COB) for bipolar input signal ranges.

Table I describes the LSB, transition values and code definitions for each possible ADC80 analog input signal range for 8, 10 and 12 bit resolutions.

SERIAL DATA

Two straight binary (complementary) codes are available on the serial output line of the ADC80; they are CSB and COB. The serial data is available only during conversion and appears with the most significant bit (MSB) occuring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES					
Analog Input Voltage Range	Defined As:	±10V	+5V	±2.5V	0 to +10V	0 to +5V
Code Designation		COB or CTC*	COB or CTC*	COB or CTC*	CSB**	CSB**
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values MSB LSB						
000...000***	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB
011...111	Mid Scale	0	0	0	+5V	+2.5V
111...110	-Full Scale	-10V +½LSB	-5V +½LSB	-2.5V +½LSB	0 + ½LSB	0 +½LSB

* COB = Complementary Offset Binary
** CSB = Complementary Straight Binary
* CTC = Complementary Two's complement - obtained by using the complement of the most significant bit ($\overline{MSB}$). $\overline{MSB}$ is available on pin 8.
*** Voltages given are the nominal value for transition to the code specified.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

DISCUSSION OF SPECIFICATIONS

The ADC80 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors and conversion speed effects on accuracy. The ADC80 is factory trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial GAIN and OFFSET errors are factory trimmed to ±0.1% of FSR (±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown on page 6.

ACCURACY DRIFT VS TEMPERATURE

Three major drift parameters degrade A/D converter accuracy over temperature; they are gain, offset and linearity drift. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, these errors do not add algebraically, but are random variables which behave as root-sum-squared (RSS) or 1σ errors as follows:

$$RSS = \sqrt{\in_g^2 + \in_o^2 + \in_e^2}$$

where $\in_g$ = gain drift error (ppm/°C)
$\in_o$ = offset drift error (ppm of FSR/°C)
$\in_e$ = linearity error (ppm of FSR/°C)

For unipolar operation, the total RSS drift is ±30.3ppm/°C.

ACCURACY VS SPEED

In successive approximation A/D converters, the conversion speed affects linearity and differential linearity errors. Conversion speed and its effect on linearity and differential linearity errors for the ADC80 are shown in Figures 3 and 4.

The ADC80 conversion speeds are specified for a maximum linearity error of ±½LSB and a differential linearity error of ±½LSB with the internal clock. Faster conversion speeds up to 23μs for 12 bits, 12μsec for 10 bits and 6μs for 8 bits are possible with an external clock (see page 7).

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect the accuracy of the ADC80. The ADC80 power supply sensitivity is specified for ±0.003% of FSR/%Vs for ±15V (±12V) supplies and ±0.0015% of FSR/%Vs for +5V supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with the ADC80. See layout precautions and power supply decoupling on page 6.

LAYOUT and OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected internally in the ADC80 but should be connected together as close to the unit as possible, preferably to a large ground plane under the ADC80. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. Analog and digital +5 volt supplies are also not connected internally; they should be connected together at the unit as shown below in Figure 7 (Pins 7 and 9).

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic type capacitors as shown in Figure 7 to obtain noise free operation. These capacitors should be located close to the ADC80. 1μF electrolytic type capacitors should be bypassed with 0.01μF ceramic capacitors for improved high frequency performance.

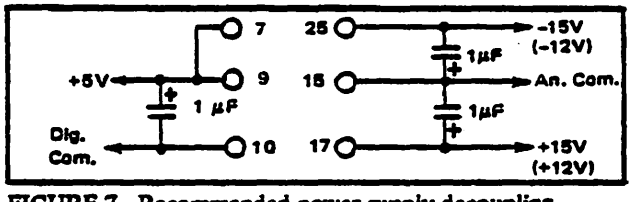


FIGURE 7. Recommended power supply decoupling.

INPUT SCALING

The ADC80 input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 8 for circuit details.

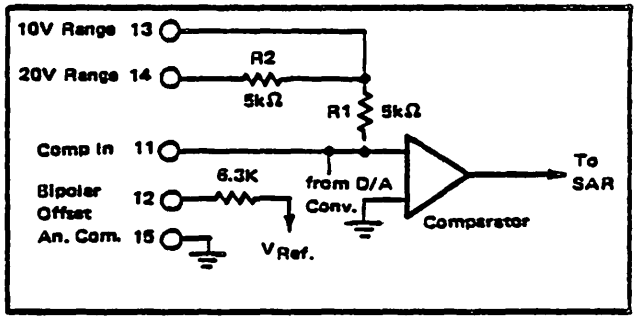


FIGURE 8. ADC80 Input scaling circuit.

Input Signal Range	Output Code	Connect Pin 12 To Pin	Connect Pin 14 To	Connect Input Signal To
±10V	COB or CTC	11	Input Signal	14
±5V	COB or CTC	11	Open	13
±2.5V	COB or CTC	11	Pin 11	13
0 to +5V	CSB	15	Pin 11	13
0 to +10V	CSB	15	Open	13

TABLE II. ADC80 Input scaling connections.

Optional External Gain and Offset Adjustments

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC80 as shown in Figures 9 and 10. Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for minimum drift over temperature and time. These pots may be any value from 10 kΩ to 100 kΩ. All resistors should be 20% carbon or better. Pin 16 (Gain Adjust) may be left open if no external adjustment is required.

ADJUSTMENT PROCEDURE

OFFSET - Connect the OFFSET potentiometer as shown in Figure 9. Sweep the input through the end point transition voltage that should cause an output transition to all ones.

Adjust the OFFSET potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

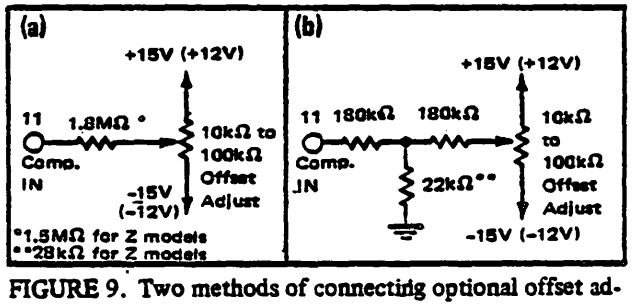


FIGURE 9. Two methods of connecting optional offset adjust with a 0.4% of FSR range of adjustment.

GAIN - Connect the GAIN adjust potentiometer as shown in Figure 10. Sweep the input through the end point transition voltage that should cause an output transition to all zeros.

Adjust the GAIN potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.
Table I details the transition voltage levels required.

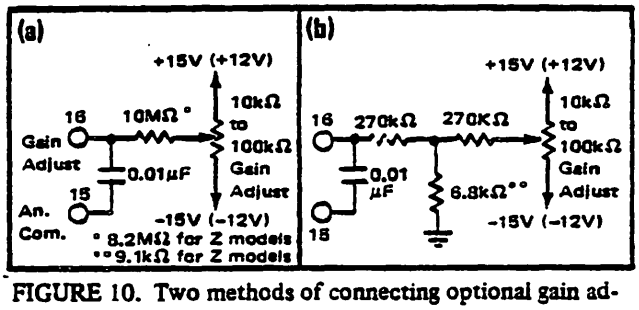


FIGURE 10. Two methods of connecting optional gain adjust with a 0.6% range of adjustment.

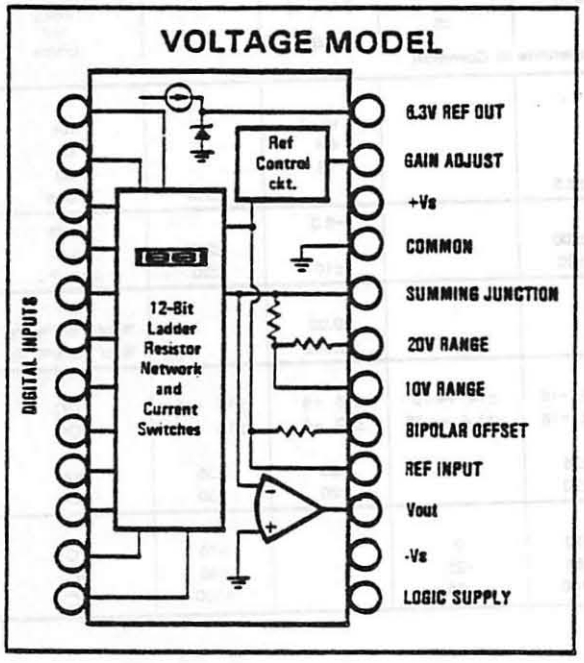
BURR-BROWN

DAC80

Integrated Circuit
DIGITAL-TO-ANALOG CONVERTER

FEATURES:

- WIDE POWER SUPPLY RANGE MODELS AVAILABLE (Z MODELS)
- 12-BIT, 3-DIGIT RESOLUTION
- ±1/2LSB MAXIMUM NONLINEARITY
- COMPLETE WITH INTERNAL REFERENCE AND OUTPUT AMPLIFIER (V MODELS)
- FAST SETTLING - 300nsec to ±0.01% (I MODELS)
- CERAMIC DUAL-IN-LINE PACKAGE
- LOW COST



DESCRIPTION

Use this popular 12-bit digital-to-analog converter for low cost precision performance applications.

DAC80, with internal reference and optional output amplifier, offers a maximum nonlinearity error of ±0.012%, ±30ppm/°C maximum gain drift, and monotonicity - all over a 0°C to 70°C operating range. In the bipolar configuration, total accuracy drift is guaranteed to be less than ±25ppm/°C. Select TTL compatible complementary 12-bit binary (CBI) or 3-digit BCD (CCD) input codes.

Packaged within DAC80's 24-pin dual-in-line ceramic case are fast-settling switches and stable, laser-trimmed thin-film resistors that let you select output voltage ranges of ±2.5, ±5, ±10, 0 to +5, 0 to +10 volts (V models) or output current ranges of ±1mA or 0 to -2mA (I models). Voltage output models settle to ±0.01% of FSR in 3μsec for a 10V step change.

By specifying the new DAC80Z model with a supply range of ±11.4V to ±16.0V, you can use this proven D/A converter in microprocessor and semiconductor memory systems.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

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PDS-322F

Printed in U.S.A. February, 1979

SPECIFICATIONS

Typical at 25°C and rated power supplies unless otherwise noted.

ELECTRICAL

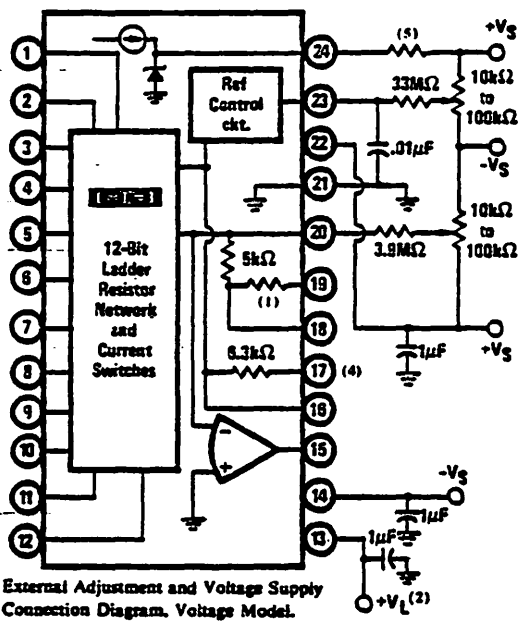
MODEL	DAC80CBI			DAC80CCD			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
DIGITAL INPUT							
Resolution			12				Bits
						3	Digits
Logic Levels (TTL/Compatible)[1]							
Logical "1" (at +40µA)	+2		+5.5	+2		+5.5	VDC
Logical "0" (at -1.0mA)	0		+0.8	0		+0.8	VDC
ACCURACY							
Linearity Error at 25°C		±1/4	±1/2		±1/8	±1/4	LSB
Differential Linearity Error		±1/2	+1, -3/4		±1/4	±1/2	LSB
Gain Error[2]		±0.1	±0.3		±0.1	±0.3	%
Offset Error[2]		±0.05	±0.15		±0.05	±0.15	% of FSR[3]
Monotonicity Temp. Range, min	0		+70	0		+70	°C
DRIFT[4] (0°C to +70°C)							
Total bipolar drift, max (includes gain, offset, and linearity drifts)[5]			±25			±25	ppm of FSR/°C
Total error over 0°C to +70°C[6]							
Unipolar		±0.05	±0.15		±0.05	±0.15	% of FSR
Bipolar		±0.05	±0.12		±0.05	±0.12	% of FSR
Gain		±15	±30		±15	±30	ppm/°C
Exclusive of internal reference			±10			±10	ppm/°C
Unipolar Offset		±1	±3		±1	±3	ppm of FSR/°C
Bipolar Offset		±7	±15		±7	±15	ppm of FSR/°C
Differential Linearity 0°C to +70°C		±1/2	+1, -7/8		±1/2	+1, -7/8	LSB
Linearity Error 0°C to +70°C			±1/2			±1/2	LSB
CONVERSION SPEED/V models							
Settling Time to ±0.01% of FSR For FSR Change							
with 10kΩ Feedback		5			5		µsec
with 5kΩ Feedback		3			3		µsec
For 1LSB Change		1.5			1.5		µsec
Slew Rate	10	20		10	20		V/µsec
CONVERSION SPEED/I models - of FSR							
Settling Time to ±0.01% For FSR Change							
10Ω to 100Ω Load		300			300		nsec
1kΩ Load		1			1		µsec
ANALOG OUTPUT/V models							
Ranges[7]	±2.5, ±5, ±10, 0 to +5, 0 to +10				0 to +10		Volts
Output Current	±5			±5			mV
Output Impedance (DC)		0.05			0.05		ohms
Short Circuit Duration	Indefinite to Common						
ANALOG OUTPUT/I models							
Ranges		±1, 0 to -2			0 to -2		mA
Output Impedance - Bipolar		4.4			4.4		kΩ
Output Impedance - Unipolar		15			15		kΩ
Compliance			±2.5			±2.5	Volts
INTERNAL REFERENCE VOLTAGE		+6.3			+6.3		Volts
Maximum External Current[8]			±200			±200	µA
Tempco of Drift, max		±10	±20		±10	±20	ppm/°C
POWER SUPPLY SENSITIVITY							
+15V Supply		±0.02			±0.02		% of FSR/% Vs
-15V and +5V Supplies		±0.002			±0.002		% of FSR/% Vs
POWER SUPPLY REQUIREMENTS							
DAC80	±14, +4.75	±15, +5	±16, +16	±14, +4.75	±15, +5	±16, +16	VDC
DAC80Z[7]	±11.4, +4.75	±12, +5	±16, +16	±11.4, +4.75	±12, +5	±16, +16	VDC
Supply Drain							
±15V/±12V (including 5mA load)		±25	±35		±25	±35	mA
+5V (logic supply)		+20	±30		+20	±30	mA
TEMPERATURE RANGE							
Specification	0		+70	0		+70	°C
Operating (double above specs)	-25		+85	-25		+85	°C
Storage	-55		+100	-55		+100	°C

NOTES:

1. Adding external CMOS hex buffers CD 4009A will provide CMOS input compatibility.
2. Adjustable to zero with external trim potentiometer.
3. FSR means "Full Scale Range" and is 20V for ±10V range, 10V for ±5V range, etc.
4. To maintain drift spec internal feedback resistors must be used for current output models.
5. See "Computing Total Accuracy Over Temperature."
6. With gain and offset errors adjusted to zero at 25°C. See discussion on last page.
7. DAC80Z supply range is ±12.0V min to ±16.0V max for 0 to +10V and ±10V outputs.
8. Maximum with no degradation of specifications.

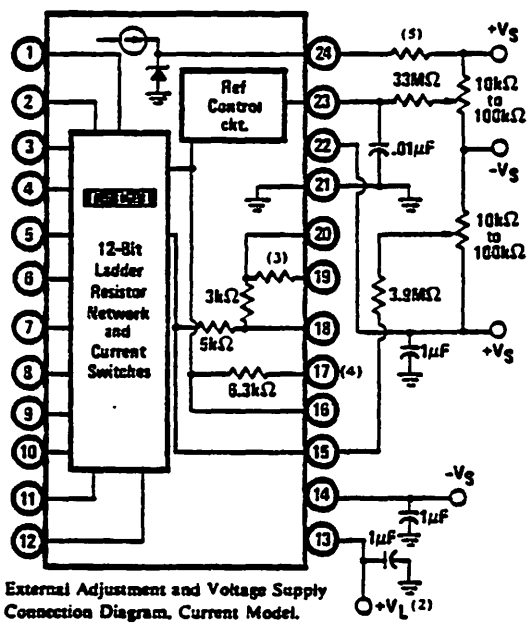
CONNECTION DIAGRAMS

VOLTAGE MODEL



External Adjustment and Voltage Supply Connection Diagram, Voltage Model.

CURRENT MODEL



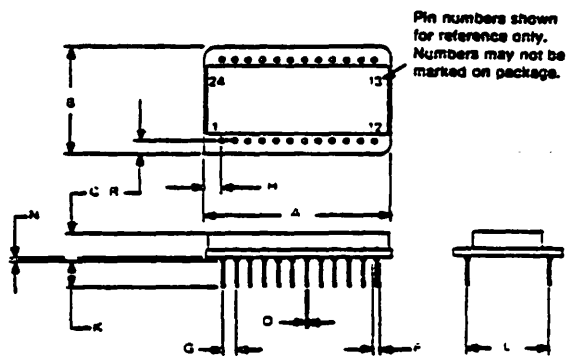
External Adjustment and Voltage Supply Connection Diagram, Current Model.

NOTES:
1. 3kΩ for CCD models, 5kΩ for CBI models.
2. If connected to+Vs, which is permissible, power dissipation increases 200mW.
3. CBI model, 2kΩ; CCD model, 0Ω and pin 20 has no internal connection.
4. 6.3kΩ resistor internally grounded on CCD models.
5. Resistor required only for Z models, see "Operating Instructions".

PIN ASSIGNMENTS

I Models	Pin No.	V Models
(MSB) Bit 1	1	Bit 1 (MSB)
Bit 2	2	Bit 2
Bit 3	3	Bit 3
Bit 4	4	Bit 4
Bit 5	5	Bit 5
Bit 6	6	Bit 6
Bit 7	7	Bit 7
Bit 8	8	Bit 8
Bit 9	9	Bit 9
Bit 10	10	Bit 10
Bit 11	11	Bit 11
(LSB) Bit 12	12	Bit 12 (LSB)
LOGIC SUPPLY	13	LOGIC SUPPLY
-Vs	14	-Vs
IOUT	15	VOUT
REF. INPUT	16	REF. INPUT
BIPOLAR OFFSET	17	BIPOLAR OFFSET
SCALING NETWORK	18	10V RANGE
SCALING NETWORK	19	20V RANGE
SCALING NETWORK	20	SUMMING JUNCTION
COMMON	21	COMMON
+Vs	22	+Vs
GAIN ADJUST	23	GAIN ADJUST
6.3V REF. OUT	24	6.3V REF. OUT

MECHANICAL



NOTE:
Leads in true position within .010" (.25mm)R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.310	1.360	33.27	34.54
B	.770	.810	19.56	20.57
C	.150	.210	3.81	5.33
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.600 BASIC		15.24 BASIC	
N	.002	.010	0.05	0.25
R	.085	.105	2.16	2.67

CASE: Black Ceramic
MATING CONNECTOR: 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).
WEIGHT: 8.4 grams (0.3 oz.)
HERMETICITY: Conforms to method 1014 condition C step 1 (fluorocarbon) of MIL-STD-883 (gross leak).

DISCUSSION

DIGITAL INPUT CODES

The DAC80 accepts complementary digital input codes in either binary (CBI) or decimal (CCD) format. The CBI model may be connected by the user for any one of three complementary codes: CSB, CTC or COB.

TABLE I. Digital Input Codes.

	DIGITAL INPUT	ANALOG OUTPUT		
	MSB LSB	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
CBI Models	000000000000	+Full Scale	+Full Scale	-LSB
	011111111111	+1/2 Full Scale	Zero	-Full Scale
	100000000000	Mid-scale -1LSB	-1 LSB	+Full Scale
	111111111111	Zero	-Full Scale	Zero
CCD Models	MSB LSB	CCD Complementary Coded Decimal - 3 Digits		
	0110 0110 0110	+Full Scale		
	1111 1111 1111	Zero		

* Invert the MSB of the COB code with an external inverter to obtain CTC code.

ACCURACY

Linearity of a D/A converter is the true measure of its performance. The linearity error of the DAC80 is specified over its entire temperature range. This means that the analog output will not vary by more than ±1/2LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range of 0°C to +70°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over a 0°C to +70°C range is guaranteed in the DAC80 to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point differences for each DAC80 model at 0°C, +25°C and +70°C; 2) calculating the gain error with respect to the 25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm/°C and is given in the electrical specifications both with and without internal reference.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range. The offset is measured at 0°C, +25°C and +70°C. The maximum change in Offset is referenced to the Offset at 25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each DAC80 model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 1).

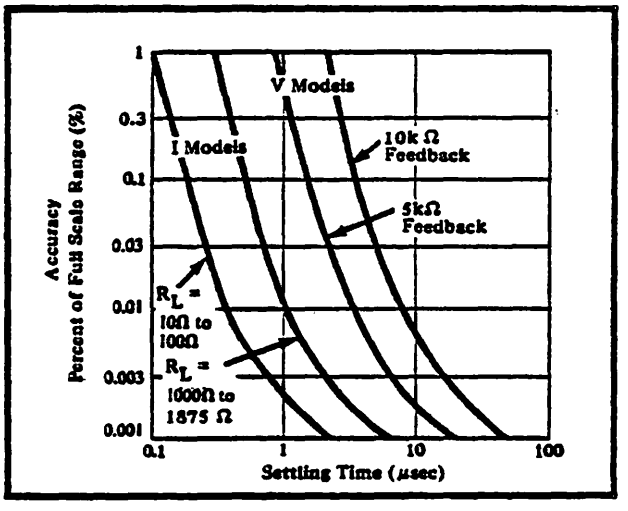


FIGURE 1. Full Scale Range Settling Time vs Accuracy

Voltage Output Models: Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20V, 10V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst case settling time occurs.

Current Output Models: Two settling times are specified to ±0.01% of FSR. Each is given for current models connected with two different resistive loads: 10Ω to 100Ω and 1000Ω to 1875Ω. Internal resistors are provided for connecting nominal load resistances of approximately 1000Ω to 1800Ω for output voltage range of ±1V and 0 to -2V. See Table IV.

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of all current output models is ±2.5V. Maximum safe voltage swing permitted without damage to the DAC80 is ±5V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in

either the positive, negative, or logic supplies about the nominal power supply voltages (see Figure 2).

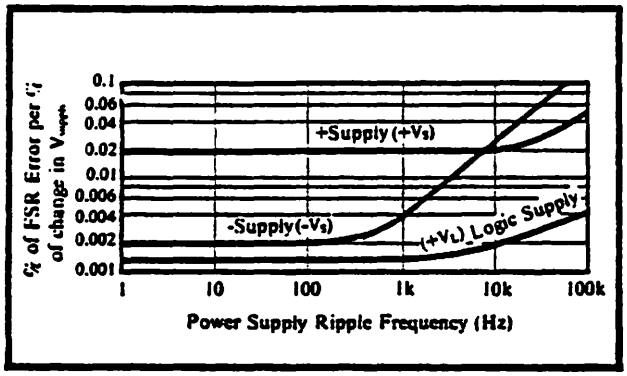


FIGURE 2. Power Supply Rejection vs Power Supply Ripple.

REFERENCE SUPPLY

All DAC80 models are supplied with an internal 6.3 volt reference voltage supply. This voltage (pin 24) has a tolerance of ±5% and must be connected to the Reference Input (pin 16) for specified operation. This reference may be used externally also, but external current drain is limited to 200μA. An external buffer amplifier is recommended if this reference will be used to drive other system components.

OPERATING INSTRUCTIONS

±12 VOLT SUPPLY OPERATION

The Z models will operate with supply voltages as low as ±11.4V. For operation with supplies less than ±14V an external resistor must be connected between the positive supply and pin 24. This provides additional current required by the internal reference. The required resistor value for supply voltages of ±11.4V to ±12.6V is 2.0kΩ and for supplies of ±12.6V to ±14V is 3.9kΩ.

It is recommended that output voltage ranges -10V to +10V and 0 to +10V not be used with the Z model if the supply voltages are ever less than the recommended ±12V. The output amplifier may saturate if $|V_{supply}| - |V_{out}\ max| < 2.0V$. This applies to units with both CBI and CCD input codes. Except for operation at lower supply voltages, the DAC80Z and DAC80 operation is identical.

POWER SUPPLY CONNECTIONS

Decoupling: For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagrams. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the DAC80. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in the connection diagrams and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 33MΩ resistors (20% carbon or better) should be located close to the DAC80 to prevent noise pickup. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in each case. The Gain Adjust (pin 23) is a high impedance point and a 0.001μF to 0.01μF ceramic capacitor should be connected from this pin to Common (pin 21) to prevent noise pickup. Refer to Figures 4 and 5 for relationship of Offset and Gain adjustments to unipolar and bipolar D/A converters.

Offset Adjustment: For unipolar (CSB, CCD) configurations, apply the digital input code that should produce zero potential output and adjust the Offset potentiometer for zero output.

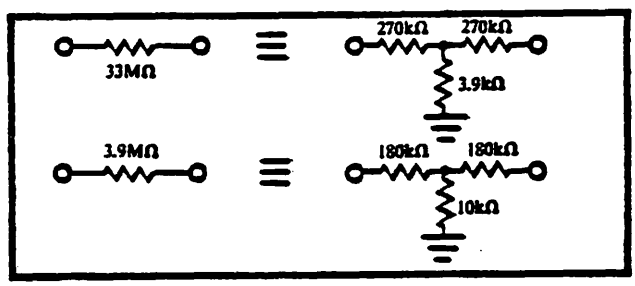


FIGURE 3. Equivalent Resistances.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is -10V. See Table II for corresponding codes and the Connection Diagrams for offset adjustment connections.

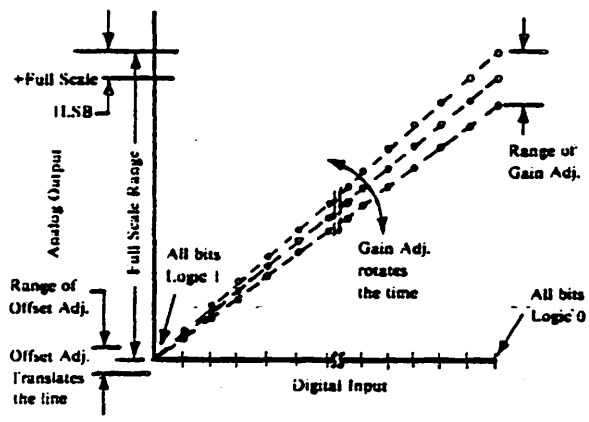


FIGURE 4. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

TABLE II. Digital Input/Analog Output.

	DIGITAL INPUT	ANALOG OUTPUT			
		VOLTAGE*		CURRENT	
		0 to +10V	±10V	0 to -2mA	±1mA
CBI Models	12-Bit Resolution MSB LSB				
	000000000000	+9.9976V	+9.9951V	-1.9995mA	-0.9995mA
	011111111111	+5.0000V	0.0000V	-1.0000mA	0.0000mA
	100000000000	+4.9976V	-0.0049V	-0.9995mA	+0.0005mA
	111111111111	0.0000V	-10.0000V	0.0000mA	+1.000mA
	One LSB	2.44mV	4.88mV	0.488μA	0.488μA
CCD Models	3-Digital Resolution MSB LSB				
	0110 0110 0110	+9.990V**	N/A	-1.249mA	N/A
	0110 0110 1111	+9.900V	N/A	-1.238mA	N/A
	0110 1111 1111	+9.000V	N/A	-1.125mA	N/A
	1111 1111 1111	0.000V	N/A	0.000mA	N/A
	One LSB	10.00mV	N/A	1.25μA	N/A

** Normal full scale range with correct codes; output can go higher if illegal codes are applied.
* To obtain values for other binary (CBI) ranges: 0 to +5V range: divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

Gain Adjustment: For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the Gain potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the Connection Diagrams for gain adjustment connections.

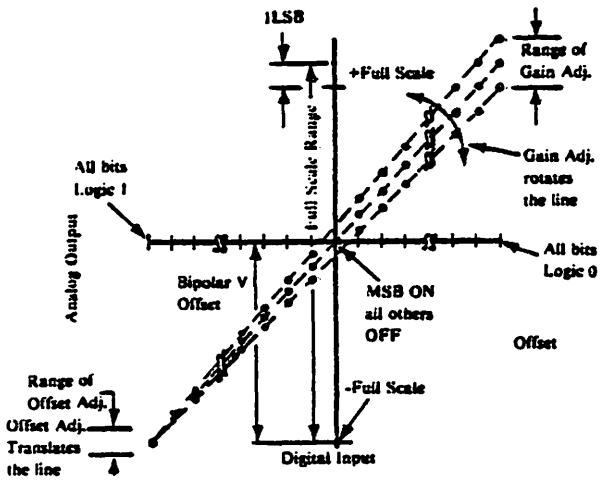


FIGURE 5. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

VOLTAGE OUTPUT MODELS

OUTPUT RANGE CONNECTIONS

Internal scaling resistors provided in the DAC80 may be connected to produce bipolar output voltage ranges of ±10V*, ±5V or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V*. See Figure 6.

*Refer to ±12V Supply Operation discussion.

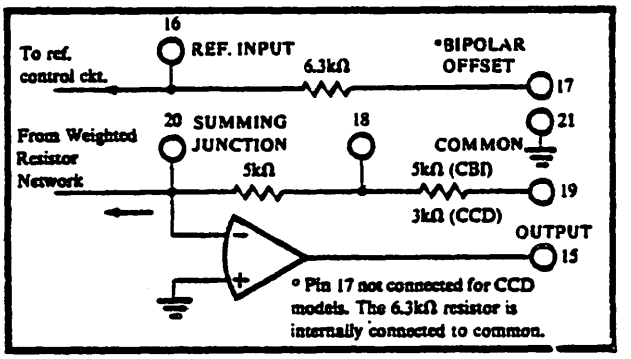


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

Gain and offset drift are minimized in the DAC80 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table III. Settling time is specified for a full scale range change: 5 microseconds for 8kΩ or 10kΩ feedback resistors; 3 microseconds for a 5kΩ feedback resistor.

TABLE III. Output Voltage Range Connections - Voltage Model DAC80.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB or CTC	19	20	15	24
±5	COB or CTC	18	20	N.C.	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	20	24
0 to +10V	CCD	19	N.C.	15	24

CURRENT OUTPUT MODELS

The equivalent output circuit and resistive scaling network of the current model differ from the voltage model and are shown in Figures 7 and 8. Instructions for using the DAC80-XXX-I with a resistor or an external op amp follow. External R_{LS} or R_{LP} resistors are required to produce exactly 0 to -2V or ±1V output. TCR of these resistors should be ±100ppm/°C or less to maintain the DAC80 output specifications. If exact output ranges are not required, the external resistors are not needed.

Internal resistors are provided to scale an external op amp or to configure a resistive load to offer two output voltage ranges of ±1V or 0 to -2V. These resistors (R_{LI}) are an integral part of the DAC80 and maintain gain and bipolar offset drift specifications. If the internal resistors are not used, external R_L (or R_F) resistors should have a TCR of ±25 ppm/°C or less to minimize drift. This will typically add ±50 ppm/°C + the TCR of R_L (or R_F) to the total drift.

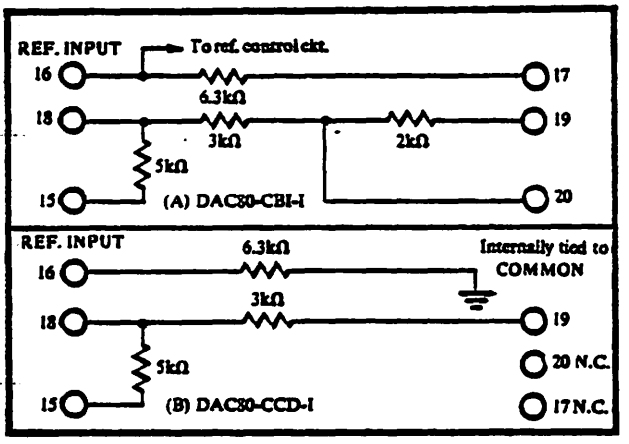


FIGURE 7. Internal Scaling Resistors.

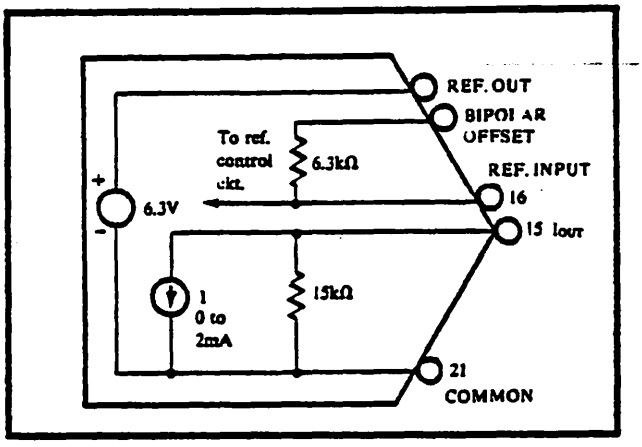


FIGURE 8. DAC80 Current Model Equivalent Output Circuit.

DRIVING A RESISTIVE LOAD UNIPOLAR

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 9 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2mA \left(\frac{15k\Omega \times R_L}{15k\Omega + R_L} \right)$$

Where R_L max = 1.36kΩ
and V_{OUT} max = -2.5V

To achieve specified drift, connect the internal scaling resistor (R_{LI}) as shown in Table IV to an external metal film trim resistor (R_{LS}) to provide full scale output voltage range of 0 to -2V. With $R_{LS} = 0$, $V_{OUT} = -1.82V$.

CCD Input Code: Connect the internal scaling resistors as shown in Table IV and add an external metal film

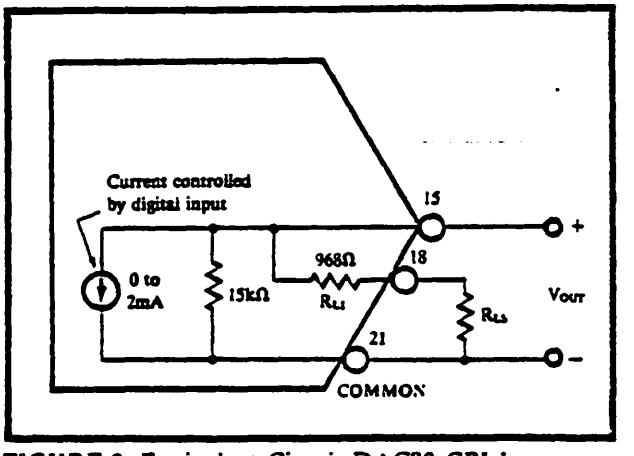


FIGURE 9. Equivalent Circuit DAC80-CBI-I Connected for Unipolar Voltage Output with Resistive Load.

TABLE IV. DAC80-XXX-I Resistive Load Connections.

Digital Input Codes	Output Range	Internal Resistance R_{LI}	1% Metal Film External Resistance R_{LS}	1% Metal Film External Resistance R_{LP}	R_{LI} Connections: Connect Pin 15 to	R_{LI} Connections: Connect Pin 18 to	R_{LI} Connections: Connect Pin 20 to	Reference: Connect Pin 16 to	Bipolar Offset: Connect Pin 17 to	Bipolar Offset: R_{LS}	Bipolar Offset: R_{LP}
CSB	0 to -2V	0.968kΩ	105Ω	N/A	20	19 & R_{LS}	15	24	Com (21)	Between Pin 18 & Com (21)	N/A
CCD	0 to -2V	1.875kΩ	N/A	36.5kΩ	19	Com (21)	N.C.	24	N.C.	N/A	Between Pin 15 & 21
COB or CTC	±1V	1.2kΩ	90.9Ω	N/A	18	19	R_{LS}	24	15	Between Pin 20 & Com (21)	N/A

resistor (R_{LP}) in parallel as shown in Figure 10 to obtain a 0 to -2V full scale output voltage range for CCD input codes:

$$\text{With } R_L = \frac{R_{LI} \times R_{LP}}{R_{LI} + R_{LP}}$$

$$V_{OUT} = -1.25\text{mA} \left(\frac{15.6\text{k}\Omega \times R_L}{15.6\text{k}\Omega + R_L} \right)$$

If $R_{LP} = \infty$, $V_{OUT} = -2.08\text{V}$

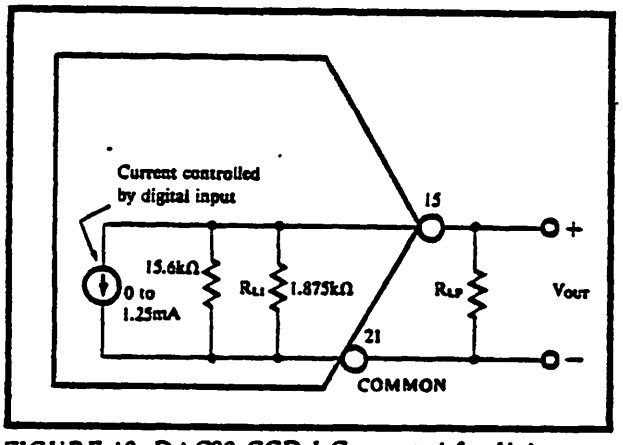


FIGURE 10. DAC80-CCD-I Connected for Voltage Output with Resistive Load.

DRIVING A RESISTOR LOAD BIPOLAR

The equivalent ouptut circuit for a bipolar output voltage range is shown in Figure 11, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1\text{mA} \left(\frac{R_L \times 4.44\text{k}\Omega}{R_L + 4.44\text{k}\Omega} \right)$$

Where R_L max = 5.72kΩ

V_{OUT} max = ±2.5V

To achieve specified drift, connect the internal scaling resistors (R_{LI}) as shown in Table IV for the COB or CTC

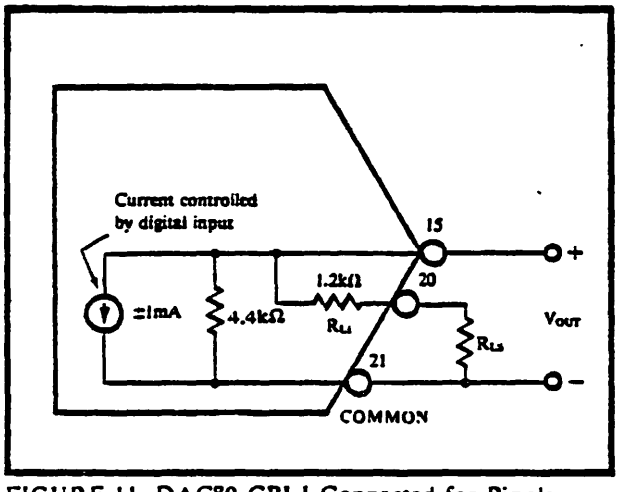


FIGURE 11. DAC80-CBI-I Connected for Bipolar Output Voltage with Resistive Load.

codes and add an external metal film resistor (R_{LS}) in series to obtain a full scale output range of ±1V.

With $R_{LS} = 0$, $V_{OUT} = \pm 0.944\text{V}$.

DRIVING AN EXTERNAL OP AMP

The current model DAC80 will drive the summing junction of an op amp used as a current to voltage converter to produce an output voltage. See Figure 12.

$$V_{OUT} = I_{OUT} \times R_F$$

where I_{OUT} is the DAC80 output current and R_F is the feedback resistor. Using the internal feedback resistors of the current model DAC80 provides output voltage ranges the same as the voltage model DAC80. To obtain the desired output voltage range when connecting an external op amp, refer to Table V.

TABLE V. Voltage Range of Current Output DAC80.

Output Range	Digital Input Codes	Connect Ⓐ to	Connect Pin 17 to	Connect Pin 19 to	Conect Pin 16 to
±10V	COB or CTC	19	15	Ⓐ	24
±5V	COB or CTC	18	15	N.C.	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	15	24
0 to +10V	CCD	19	N.C.	Ⓐ	24

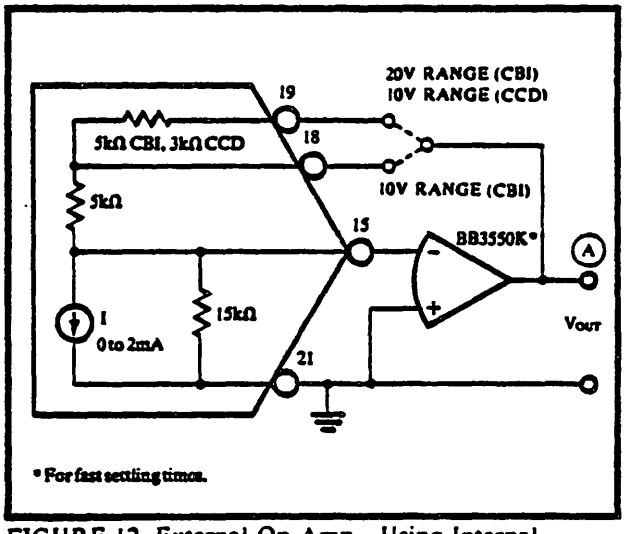


FIGURE 12. External Op Amp - Using Internal Feedback Resistors.

OUTPUT LARGER THAN 20V RANGE

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and -2mA for unipolar voltage ranges. See Figure 13. Use protection diodes when a high voltage op amp is used.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the

lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50 ppm/°C + R_F drift to total drift.

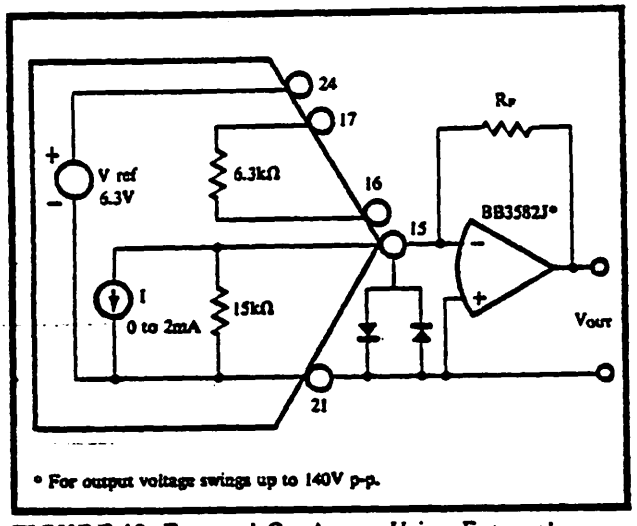


FIGURE 13. External Op Amp - Using External Feedback Resistors.

COMPUTING TOTAL ACCURACY OVER TEMPERATURE

The accuracy drift with temperature of a DAC80 consists of three primary components: Gain drift, unipolar or bipolar offset drift, and linearity drift. To obtain the worst case accuracy drift, most users would assume that all drift errors are random and would simply add them algebraically. However, the worst case accuracy drift for a DAC80 operating in the bipolar mode is about one-half of the algebraic sum of the individual drift errors.

To explain this fact, it is necessary to consider the unipolar and bipolar modes of operation separately. Note that the linearity drift of both modes is negligible. (Total linearity error is less than ±1/2LSB over 0°C to +70°C.)

In the unipolar mode of operation, offset drift (±1 ppm/°C) is due primarily to voltage offset drift of the output op amp and, to a lesser extent, to the leakage current through the quad current switches. Gain drift consists of several components: 1) ±10 ppm/°C due to ratio drift of current weighting resistors to the reference resistor and current switch V_{BE} to the reference transistor (refer to Model 4550 data sheet); and 2) ±20 ppm/°C due to the zener reference. The sum of these two components, ±30 ppm/°C, is the maximum gain drift.

Because the parameters described could all drift in the same direction, the worst case accuracy drift in the unipolar mode is simply the sum of the components, or ±31 ppm/°C.

In the bipolar mode the major portion (67%) of gain drift is due to the zener reference. The gain and offset drifts caused by reference drift are always in opposite directions. Therefore, the accuracy drift will be the difference rather than the sum of these drifts.

First, consider the effect of reference variations on offset drift. Figure 14 shows a simplified circuit diagram of a DAC80 operating in the bipolar mode with all bits off. The current switch leakage current is negligible, so

$$V_{\text{-FULL SCALE}} = -\frac{R_F}{R_{BPO}} \times V_{REF}$$

$$= -\frac{10k\Omega}{6.3k\Omega} \cdot 6.3V = -10V$$

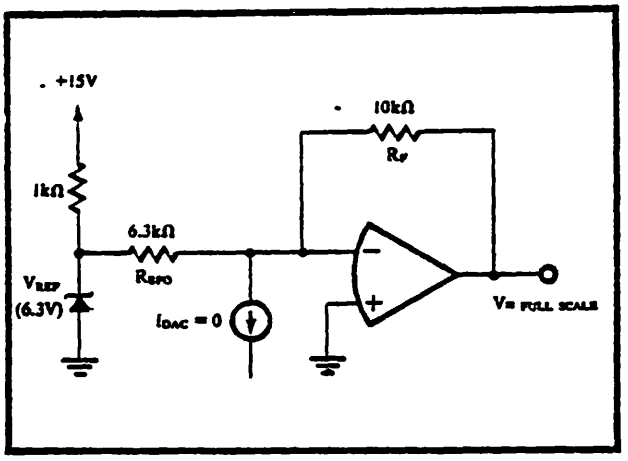


FIGURE 14. Simplified Diagram of DAC80 with "All Bits Off" Operating in Bipolar ±10V Range.

This equation shows that if V_{REF} increases, the output voltage will decrease and vice versa. If the V_{REF} drift is +20 ppm/°C, this is equivalent to (+20 ppm/°C) x (+6.3V) = +126μV/°C. This will result in a voltage drift at the amplifier output of

$$\frac{\Delta V_{-FS}}{\Delta T} = -\frac{R_F}{R_{BPO}} \cdot \frac{\Delta V_{REF}}{\Delta T}$$

$$= -\frac{10k\Omega}{6.3k\Omega} \cdot 126\mu V/°C = -200\mu V/°C.$$

Since the DAC80 is operating in the ±10V range this is equivalent to (-200μV/°C) ÷ (20V range) = -10 ppm of FSR/°C.

Now consider the effect of reference changes on gain drift. When all the bits are turned on it can be shown that:

$$\frac{\Delta V_{\text{+FULL SCALE}}}{\Delta T} = +\frac{R_F}{R_{BPO}} \cdot \frac{V_{REF}}{\Delta T}$$

$$= +\frac{10k\Omega}{6.3k\Omega} \cdot 126\mu V/°C = +200\mu V/°C$$

$$\text{and, } \frac{+200\mu V/°C}{20V \text{ Range}} = +10\text{ppm/°C of FSR.}$$

This result indicates that the drift of the minus full scale voltage will be equal in magnitude to, and in the opposite direction of, the drift of the plus full scale voltage and that zener reference variations have virtually no effect on the zero point (see Figure 15). This equation also indicates that the gain drift is equal to the V_{REF} drift in ppm/°C, and the magnitude of the minus full scale drift and plus full scale drift is equal to one-half of the V_{REF} drift.

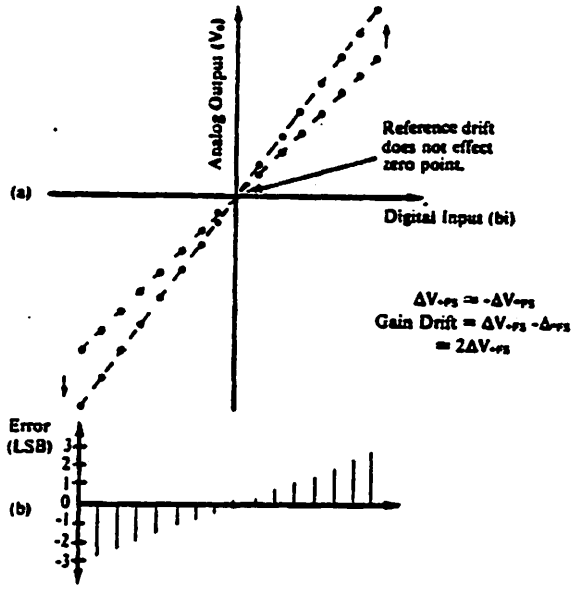


FIGURE 15. (a) Effect of a Positive Reference Drift on the Ideal D/A Transfer Function; (b) Error Distribution Due to Reference Voltage Drift in a DAC80.

Using this relationship, the worst case accuracy drift for a bipolar DAC80 can be computed. The maximum TCR of the zener reference is ±20ppm/°C. The gain drift due to the reference then is also ±20ppm/°C. The full scale drift and bipolar offset drift are each half that amount or ±10ppm/°C. The maximum gain and offset drifts of the DAC80, exclusive of the reference, are ±10ppm/°C and ±5ppm/°C respectively. Adding this to the full scale drift due to the reference gives a worst case total accuracy drift of ±25ppm/°C. (Random drifts, which these are, can be in the same direction, so they add directly.) This is much less than the total drift obtained by simply adding the maximum gain and bipolar offset drifts (±45ppm/°C). The maximum zero point drift is equal to one-half of the gain drift exclusive of the reference plus the offset drift exclusive of the reference, or ±10ppm of FSR/°C.

The DAC80 is specified over a 0°C to +70°C temperature range giving a maximum excursion from room temperature (+25°C) of 45°C. Assuming that gain and offset errors have been adjusted to zero at room temperature,

total worst case accuracy error
= Linearity error + Accuracy drift x ΔT
= ±0.01% + ±25ppm/°C (45°C)(100)
= ±0.12%;

total worst case bipolar zero point error
= Bipolar zero drift x ΔT
= ±10ppm of FSR% (45°C)(100)
= ±0.045%.

ORDERING INFORMATION

DAC80 — Low Cost 12-Bit D/A Converter Family
Example: DAC80-CBI-V Binary DAC80 with voltage output

X — Z = Wide Supply Range; Blank = Standard

XXX — INPUT CODE
CBI = Complementary 12-bit binary
CCD = Complementary 3-digit BCD

X — OUTPUT
V = Voltage
I = Current

PRICES

MODEL	1 - 24	25 - 99	100 - 249
DAC80-CBI-V	$28.50	$26.50	$19.50
DAC80-CBI-I	26.50	24.50	18.50
DAC80-CCD-V	28.50	26.50	19.50
DAC80-CCD-I	26.50	24.50	18.50
DAC80Z-CBI-V	29.50	27.50	20.50
DAC80Z-CBI-I	27.50	25.50	19.50
DAC80Z-CCD-V	29.50	27.50	20.50
DAC80Z-CCD-I	27.50	25.50	19.50

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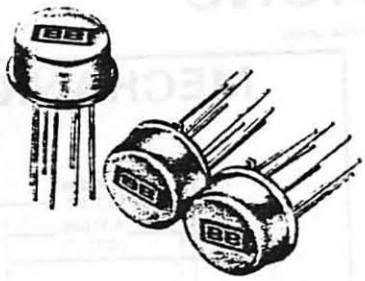
SHC298AM



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LOW COST MONOLITHIC
SAMPLE-HOLD AMPLIFIER

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- 12 Bit Throughput Accuracy
- Less Than 10 µsec Acquisition Time
- Wideband Noise Less Than 20 µV rms
- Reliable Monolithic Construction
- $10^{10}\,\Omega$ Input Resistance
- TTL/PMOS/CMOS Compatible Logic Input

DESCRIPTION

The SHC298AM is a high performance monolithic sample/hold circuit which features very high DC accuracy with fast acquisition times and a low droop rate. With the addition of one external holding capacitor, 12 bit accuracy can be achieved with a 6 microsecond acquisition time. Droop rates less than 5 millivolts per minute can be achieved with a one microfarad holding capacitor.

The fully differential logic inputs have low input currents, and are compatible with TTL, PMOS, and CMOS logic families. The input offset adjustment can be made using a single external potentiometer and resistor, and the adjustment does not degrade input offset drift.

The SHC298AM will operate with power supplies ranging from ±5 volts to ±18 volts. It is available in a hermetically sealed 8 lead low profile package, and is specified for a temperature range from -25 to +85°C. The SHC298AM is the best price/performance bargain in its class. It is well suited for use in data acquisition systems, data distribution systems, analog delay circuits, and pulse amplitude modulation circuits.

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SPECIFICATIONS

Specifications at T_A = +25°C with rated supplies with 1000 pF holding capacitor unless otherwise noted.

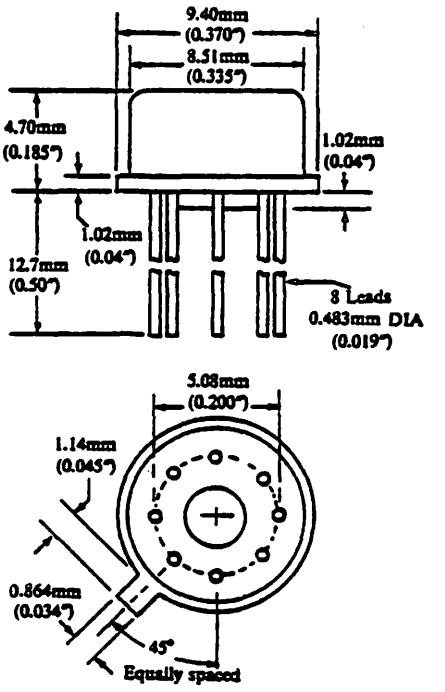
ELECTRICAL

MODELS	SHC298AM MIN	SHC298AM TYP	SHC298AM MAX	UNITS
INPUT				
ANALOG INPUT				
Voltage Range	±(Vcc-2.5)			Volts
Maximum Safe Input Signal		±Vcc		Volts
Resistance		10^{10}		Ohms
Bias Current		10	50	nA
DIGITAL INPUT				
Mode Control Truth Table	Pin 7 / Pin 8 / Circuit State: 0V / +2.4V / Sample (Track); 0V / +0.8V / Hold; +2.4V / +2.8V / Hold; +0.8V / +2.8V / Sample (Track)			
Mode Control and Mode Control Reference Input Current			10	µA
Differential Logic Threshold		1.4		Volts
TRANSFER CHARACTERISTICS				
ACCURACY (25°)				
Throughput Nonlinearity for Hold Time < 1ms		±0.010	±0.015	% of 20V
Gain		+1.0		V/V
Gain Error		±0.004	±0.010	%
Input Voltage Offset (adj to zero)		±2	±7	mV
Droop Rate		±25	±125	µV/ms
Charge Offset		±15	±25	mV
Noise (rms) 10 Hz to 100 kHz		10	20	µV
Power Supply Rejection		±25	±50	µV/V
ACCURACY DRIFT				
Gain Drift		3	4	ppm/°C
Input Offset Drift		15	45	µV/°C
Charge Offset Drift C = 1000 pF		50	150	µV/°C
C = 10,000 pF		20	50	µV/°C
Droop Rate at T_A = +85°C		1	10	mV/ms
DYNAMIC CHARACTERISTICS				
Full Power Bandwidth, C = 1000 pF	75	125		kHz
C = 10,000 pF	10	16		kHz
Output Slew Rate, C = 1000 pF	7	10		V/µs
C = 10,000 pF	1.4	2		V/µs
Aperture Time				
Negative Input Step		125	200	ns
Positive Input Step		30	45	ns
Acquisition Time (C = 1000 pF)				
to ±0.01%, 10V step		6	10	µs
to ±0.01%, 20V step		8	12	µs
to ± 0.1%, 10V step		5	9	µs
to ±0.1%, 20V step		7	11	µs
Sample-to-Hold Transient				
Peak Amplitude		160		mV
Settling to 1 mV		1.0	1.5	µs
Feedthrough (Response to 10V Input Step)		±0.007	±0.015	% of 20V
OUTPUT				
ANALOG OUTPUT				
Voltage Range	±(V_{cc}-2.5)			Volts
Current Range	±2			mA
Impedance		0.5	4	Ohms
TEMPERATURE				
Specification		-25 to +85		°C
Operating		-55 to +125		°C
Storage		-55 to +150		°C
POWER SUPPLY				
Rated Voltage		±15		VDC
Range(1)	±4.75		±18	VDC
Current		±4.5	±6.5	mA
PRICES 1 - 24		$7.95		
25 - 99		$6.90		

Prices and specifications subject to change without notice.

(1) Logic voltage on pin 8 should not exceed V_{cc} - 1 volt.

MECHANICAL

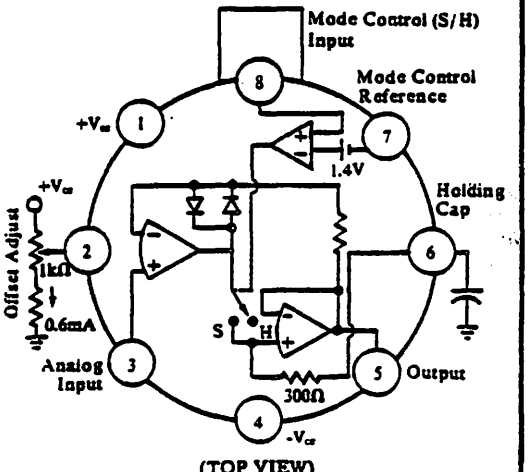


Pin Material and Plating Composition: Conforms to Mil-Std-883 Method 2003 (solderability)

Hermeticity: Conforms to Mil-Std-883, method 1014, Condition C, Step 1, Fluorocarbon (gross leak) and method 1014, Condition A, Helium, 5 x 10^{-8} cc/sec (fine leak)

Connector: None

PIN CONFIGURATION



(TOP VIEW)

TYPICAL PERFORMANCE CURVES

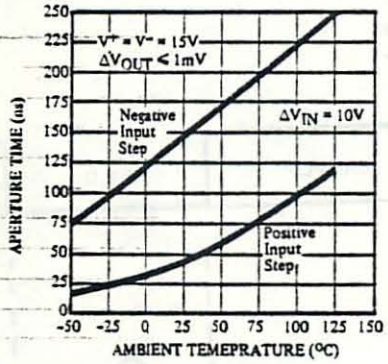


FIGURE 1. Aperture Time

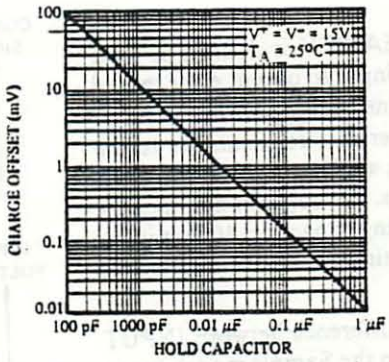


FIGURE 2. Charge Offset

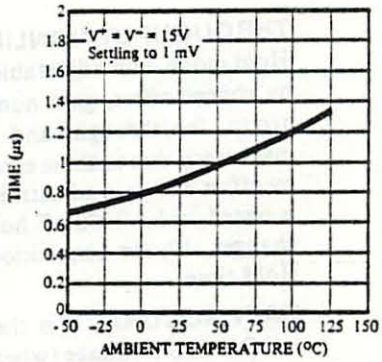


FIGURE 3. Sample-to-Hold Transient Settling Time

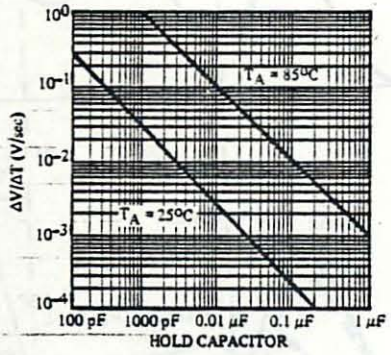


FIGURE 4. Output Droop Rate

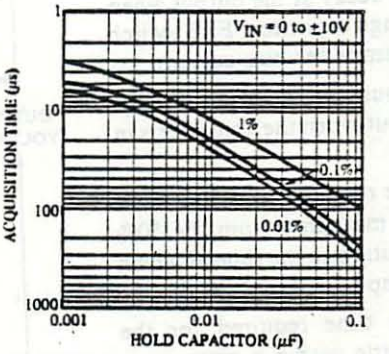


FIGURE 5. Acquisition Time

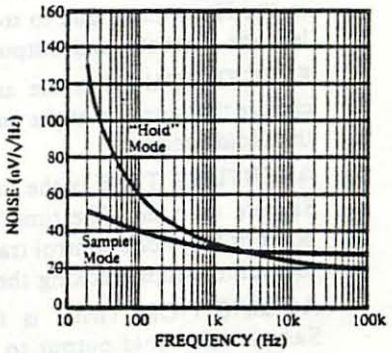


FIGURE 6. Output Noise

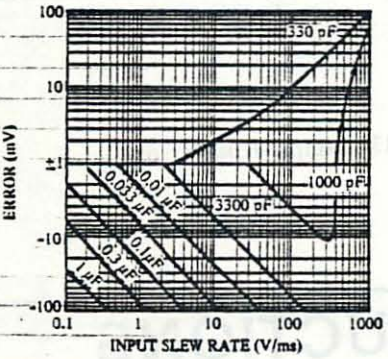


FIGURE 7. Dynamic Sampling Error

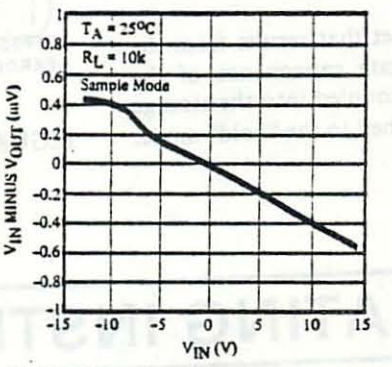


FIGURE 8. Gain Error

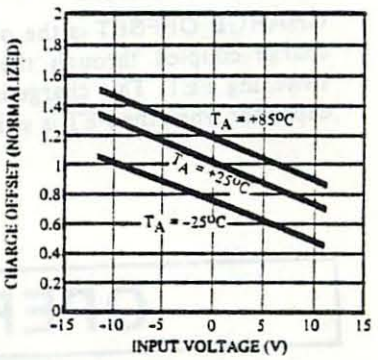


FIGURE 9. Charge Offset

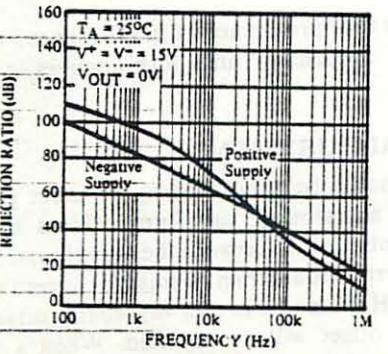


FIGURE 10. Power Supply Rejection

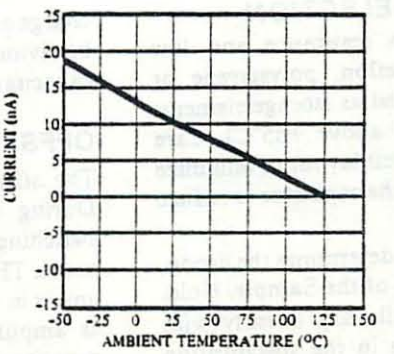


FIGURE 11. Input Bias Current

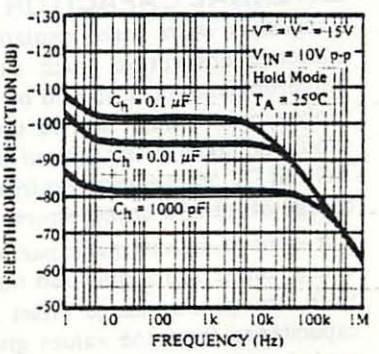


FIGURE 12. Feedthrough Rejection (Hold Mode)

DISCUSSION OF SPECIFICATIONS

THROUGHPUT-NONLINEARITY is defined as total Hold mode, non-adjustable, input to output error caused by charge offset, gain non-linearity, one millisecond of droop, feedthrough, and thermal transients. It is the inaccuracy due to these errors which cannot be corrected by offset and gain adjustments. Throughput nonlinearity is tested with a 1000 pF holding capacitor, 10 volt input changes, 10μsec acquisition time, and one millisecond Hold time.

GAIN ACCURACY is the difference between INPUT and OUTPUT voltage (when in the Sample mode) due to amplifier gain errors.

DROOP RATE is the voltage decay at the output when in the Hold mode due to storage capacitor, FET switch leakage currents, and output amplifier bias current.

FEEDTHROUGH is the amount of the input voltage change that appears at the output when the amplifier is in the Hold mode.

APERTURE TIME is the time required to switch from Sample to Hold. The time is measured from the 50% point of the mode control transition to the time at which the output stops tracking the input.

ACQUISITION TIME is the time required for the Sample and Hold output to settle within a given error band of its final value when the mode control is switched from Hold to Sample.

CHARGE OFFSET is the offset that results from the charge coupled through the gate capacitance of the switching FET. This charge is coupled into the storage capacitor when the FET is switched to the "hold" mode.

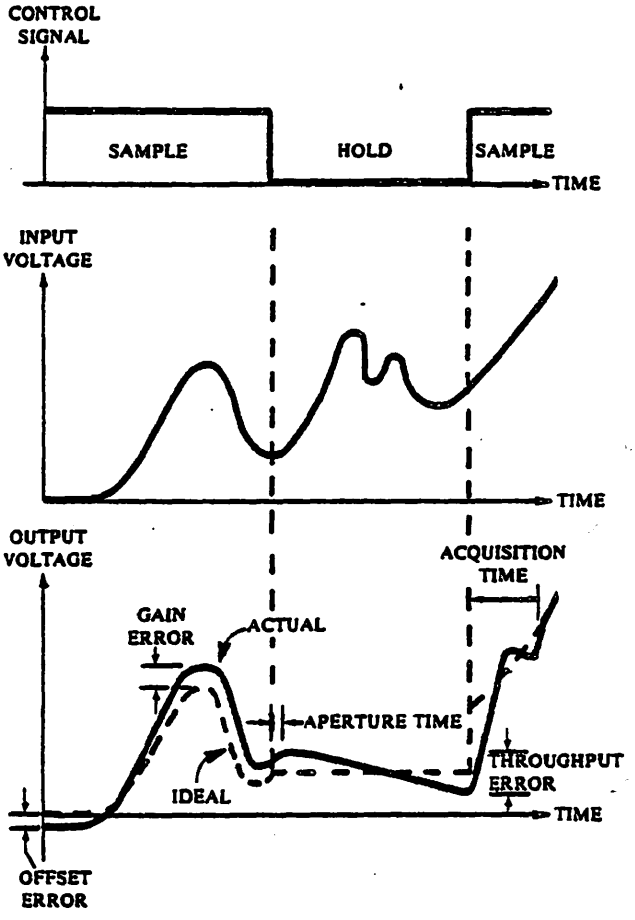


FIGURE 13. Sample-Hold Errors

OPERATING INSTRUCTIONS

EXTERNAL CAPACITOR SELECTION

Capacitors with high insulation resistance and low dielectric absorption, such as teflon, polystyrene or polypropylene units, should be used as storage elements (polystyrene should not be used above +85°C). Care should be taken in the printed circuit layout to minimize AC and DC leakage currents from the capacitor to reduce charge offset and droop errors.

The value of the external capacitor determines the droop, charge offset and acquisition time of the Sample/Hold. Both droop and charge offset will vary linearly with capacitance from the values given in the specification table for a 0.001μF capacitor. With a capacitor of 0.01μF the droop will reduce to approximately 2.5μV/ms and the charge offset to approximately 1.5mV. Figure 5 shows the behavior of acquisition time with changes in external capacitance.

OFFSET ADJUSTMENT

The offset should be adjusted with the input grounded. During the adjustment, the Sample/Hold should be switching continuously between the Sample and the Hold mode. The error should then be adjusted to zero when the unit is in the Hold mode. In this way, charge offset as well as amplifier offset will be adjusted. When a 0.001μF capacitor is used, it will not be possible to adjust the full offset error at the Sample Hold. It should be adjusted elsewhere in the system.