OSI APP NOTE

Subject: System Expansion #2

This very important App Note covers the recommended OSI 400 expansion configuration and acts as the manual for the OSI Model 480 Backplane Board.

The memory maps on the following two pages specify systems directly supported by OSI software, that is, software which is or will be available which will run on these systems without modification.

The principally supported systems are the 4K memory 65A or 65V based 6502 system and the 8K 68A or 68V based system. The 6502 system can be systematically expanded since the stack must always be on page 1 of the system. The 6800, however, should really have its stack at the highest available RAM address. This means that the PROM monitor should be modified as memory is added beyond the basic 1K system. Therefore, we recommend the 8K configuration as a good compromise.

Assembling a System with Expansion in Mind

Careful consideration and planning of your system should be done before the 400 board is assembled. This is necessary since the OSI 400 is designed to be either a single board computer or the CPU in a large system. If the 400 board is assembled in conjunction with a 480 Backplane Board and a 420 Memory Board, construction is greatly simplified! The OSI 400 Board does not fully decode its 1K of on-board RAM. This memory occupies the entire address space except for FXXX. This is done so that small programs written for any memory location will run on the board without modification. If the 1K RAM is permanently installed on the board, the user must implement the fully decoded address scheme on page A-7 of the 400 manual to add accessory boards to the system. This requires two additional ICs and several jumpers. This circuitry is duplicated on the Model 420 Memory Expansion Board if it is set to address 0000 through 3XXX. A better approach is to either socket the eight 2102s, IC-C through IC-J of the Superboard and the two 7403s, IC-N and IC-O and to transfer the memories over to a 420 memory board when added or to simply install these memories on a 420 board right from the start.

Either approach eliminates the use of the "fully decoded memory scheme." Another work saving hint is the bus pull up resistors. These pull ups can be much more easily installed on a backplane board than on the 400 board, but, are required for system operation. Considerable construction work can be saved if the 480 board and a 420 memory board are assembled in conjunction with the 400 board.

6502 System (All)

Address	Use
0000 up	User Page Zero Locations
00FF down	Monitor Page Zero Locations
0128 down	User Stack
0129 - 012F	Go Locations for 65A and 65V
0130	NMI Vector
01C0	IRQ Vector
01B0 - 01FF	65A Breakpoint
0200	Standard User Program Start Address (Cold Start)
0200 up	User Program
0FFF down	12S-1 Utilities
1FFF down	Deluxe Video Monitor Utilities

6800 Systems (68A 1K and 68V 1K)

Address	Use
0000 up	User Page Zero Locatio
0128 down	User Stack
0129 - 0131	Go Locations
01E0	NMI
01D0	IRQ
0200 up	User Program

6800 Systems (68A 8K and 68V 8K)

Address	Use
0000 up	User Page Zero Utilities
0100 up	User Program
1DXX	MIK Bug Linker Utilities
1EXX	Replaces A0XX (MIK Bug)
1FXX	Replaces 01XX (Superbug)

All Systems

Address	Use
AXXX	OSI-DOS 4K Buffer
BXXX CXXX	Reserved for Future OSI Boards
D000 up	440 Alphabetic Memory
D4XX up	440 Graphics Memory
DFFF	440 Keyboard Input
EXXX	Fast I/O
FXXX	Fully Decoded on Unmodified 400 Board
FBXX	430 I/O Board
FCXX	400 ACIA Interface
FDXX	400 PIA Interface
FEXX FFXX	OSI System Monitors

The OSI Model 480 Backplane Board is designed to connect together eight 400 series boards in a single processor system.

A. System with 2 to 8 slots

Refer to the attached 480 diagram. The 480 Backplane rear surface is the side with conductive foil. This discussion is for operation with two to eight slots. Eight to thirty-two KK-156 series Molex connectors are inserted through the front of the board and soldered in place as indicated by the 32 black lines. Power connections can be made via the right card edge or an unused slot with wires or KK-156 series connectors. If the right edge is used, a jumper should be placed on B_{24} across the prototyping area (labled E). If two or three slots are being used, this is all that needs to be done. Any board can be placed in any slot on the board (1 through 8 inclusive) as long as only one is a CPU board (400 board) and no two boards have the same memory address. If four or more system boards are used, additional bus terminators should be installed on the left-hand side of the board. Twenty 220 ohm resistors should be installed on B_{29} to B_{48} as indicated by H. When this is done, a modification to B_{42} on your 400 board should be made. In original form, B_{42} (Ø·VMA) is not buffered via a 7417 on board and will not drive seven system boards so the following board modification should be made.

Cut the foil from pin 8 of IC-T on the 400 Board. Jumper pin 8 of IC-T to pin 3 of IC-R. Install a jumper from pin 4 of IC-R to B_{42}. The CPU board should be located at slot 8 for the cleanest bus signals and the 440 Video Graphics Board should be located at slot 1 to minimize video pick-up of logic noise.

Summary of two to eight slot use:

AA. Install 8 to 32 Molex connectors.

BB. Connect ground +5, -9 and any other supply voltages.

If four or more boards are used:

CC. Install twenty 220 ohm resistors as indicated by H.

DD. Install the Ø2·VMA modification on your 400 Board.

EE. Install the 400 Board at slot 8 and the 440, if used, at slot 1. Any other boards can be installed at any other locations on the board.

B. System with 9 or more slots

The 480 boards may be linked together to provide up to 250 slots via the following procedure. After eight slots are used, the 20 address and control lines from the processor (B_{29} through B_{48}) must be buffered every eight slots via 7417s to drive the next eight slots. Similarly, the four open collector OR wired control lines B1 through B_4 to the processor must be buffered every eight slots via 7417s. Since the 7417s are symmetrical, they can be rotated 180° on the board to define the signal direction on the board. The recommended configuration is to add additional backplanes to the right. That is, slot 8 of the main mother board would be closest to slot 1 of the first expansion board.

For this configuration, the four 7417s on the main mother board would be installed such that pin 14 of each 7417 is at (B). Pin 14 of each 7417 (B) would be connected to the +5 bus and pin 7 of each 7417 (A) would be connected to ground. If only one expansion board is used, the expansion board will not need 7417s. If three or more backplanes are used, all but the last board will require buffers. Each expansion backplane

board will require the twenty 220 ohm pull ups indicated by H and will, additionally, require the 4.7K pull ups at B_1 through B_4 as indicated by G. The backplane boards may be connected together via wire jumpers (be sure only to connect +5 to B_{25} and B_{26}) or via KK-156 series Molex connectors. The standard right angle female Molex connectors can be installed at the right side of the board by shearing off about 1/4" of the board (indicated by C). The holes at the end of the board are large enough to accept both the connectors and the pull up resistors. However, the resistors will have to be stood up on end with a lead going to +5. Standard male Molex connectots can be used on the mating board by bending the pins to a right angle with pliers or, preferably, right angle Molex connectors can be used.

Summary of board instructions with 9 or more slots

AA.-EE. Follow steps AA-EE of instructions for 2 to 8 slots.

FF. Install four 7417s as indicated in the diagram with pin 14 corresponding to (B).

GG. Jumper pin 14 (B) of each 7417 to +5 and pin 7 (A) to ground.

HH. On each accessory board, follow steps AA through DD. Install the pull up resistors at the same time as the interconnection jumpers or connectors. Include the four 4.7K pull ups indicated by G on the Diagram.

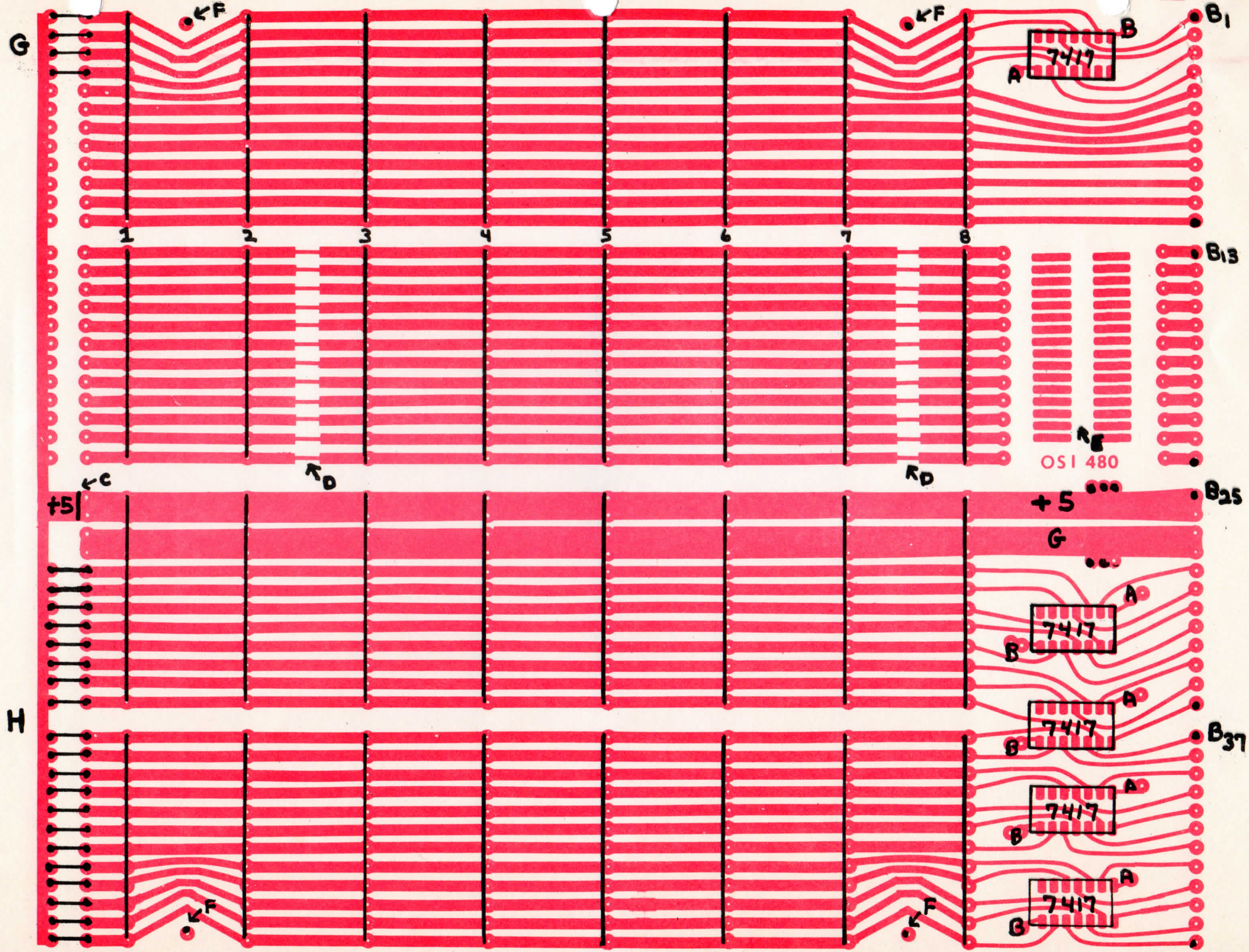
II. On all but the last accessory board, follow steps FF and GG.

JJ. Jumper B_{24} and any other of the system spares across the prototyping area of each backplane board.

Other Backplane Information

The prototyping area labeled E is for interfacing the OSI bus to other systems. Specifically, two 8T26 buffers can be placed there to interface to the KIM-1, the Motorola Development Kit, and other systems. For more specific information, request our App Note entitled "Interfacing to Other Systems."

The bus "spares" B_{13} through B_{23} are narrowed down at the areas marked D to allow easy cutting of the foils. This feature would be used to route special control signals to some of the boards. This feature will be used by some OSI boards also. The board can be mounted by enlarging the four holes labeled F and mounting the 480 board against a firm support. If a conductive surface is to be used for support, the 480 board should be backed by 1/4" masonite. Refer to the OSI App Note on "Construction Hints" for further details.


G
H
F
F
F
F
C
D
D
E
1
2
3
4
5
6
7
8
B1
B13
B25
B37
7417
A
B
OSI 480
+5
+5
G