Model 500

Description:

The state-of-the-art Model 500 Single Board Computer is fully compatible with the Ohio Scientific 48-pin bus and all Ohio Scientific Accessory Boards. The Model 500 is based on the 6502 microprocessor by MOS Technology. This chip is second sourced by Synertek and third sourced by Rockwell International. The Model 500 accepts 8 2K X 8 2616 Mask programmed ROMs (normally containing our 8K BASIC by Microsoft). 2704s, 2708s, 2716s, or similar parts can be used instead of the ROMs if the user has a custom application using his own software. Space is alsq provided for 4K of 2102-type RAM, an ACIA based serial interface which can be populated for RS-232 or 20ma current loop. Options include a PIA based parallel I/O port, 256K Memory Management (allows the system to address up to 256K memory), and up to three 1702-type PROMs.

Applications:

The 500 CPU Board can be used as a powerful small system. It is especially powerful because if has "instant 8K BASIC" and because of its 4K of on-board RAM memory. It can also be used as the basis of a larger Challenger type system. It is capable of supporting additional memory, our 430B Audio Cassette Interface, our 440B Video Graphics Board, our Floppy Disk Drive, and all other peripheral devices offered by Ohio Scientific. If a person already has an Ohio Scientific system, the 500 Board can be used to store 8K BASIC in ROM and as a 4K RAM board.

Specifications:

Mechanical: 8" X 10" G-10 Double-Sided Plated Through Hole Board

Electrical: +5 Volts at 2 Amps
-9 Volts at 500ma

Processors: Supports the 6502 or 6502A. Can be used as the controller for the 560Z which offers Z-80 and 6100.

PROM: Supports three 1702-type PROMs. Ohio Scientific offers 65A Serial PROM Monitor, 65V Video PROM Monitor, and Floppy Disk Bootstrap PROMs.

RAM: Can support up to 4K X 8 2102 type RAM

Firmware: 8K BASIC in ROM (User can supply own software in ROM)

Serial I/O: Serial Interface can be configured for RS-232 or 20ma. loop. 5 possible baud rates are jumper selectable.

Other Features: Buffering to drive up to 250 Ohio Scientific System Boards.
Memory Management for up to 256K Bytes of Memory.
PIA based parallel port also available.

OHIO SCIENTIFIC			product name/number 500/C2-0/C2-1/C2-8V/C2-8S/C2-4P	
date 8/77	revision A	page 41	status Production	sheet 1 of 1

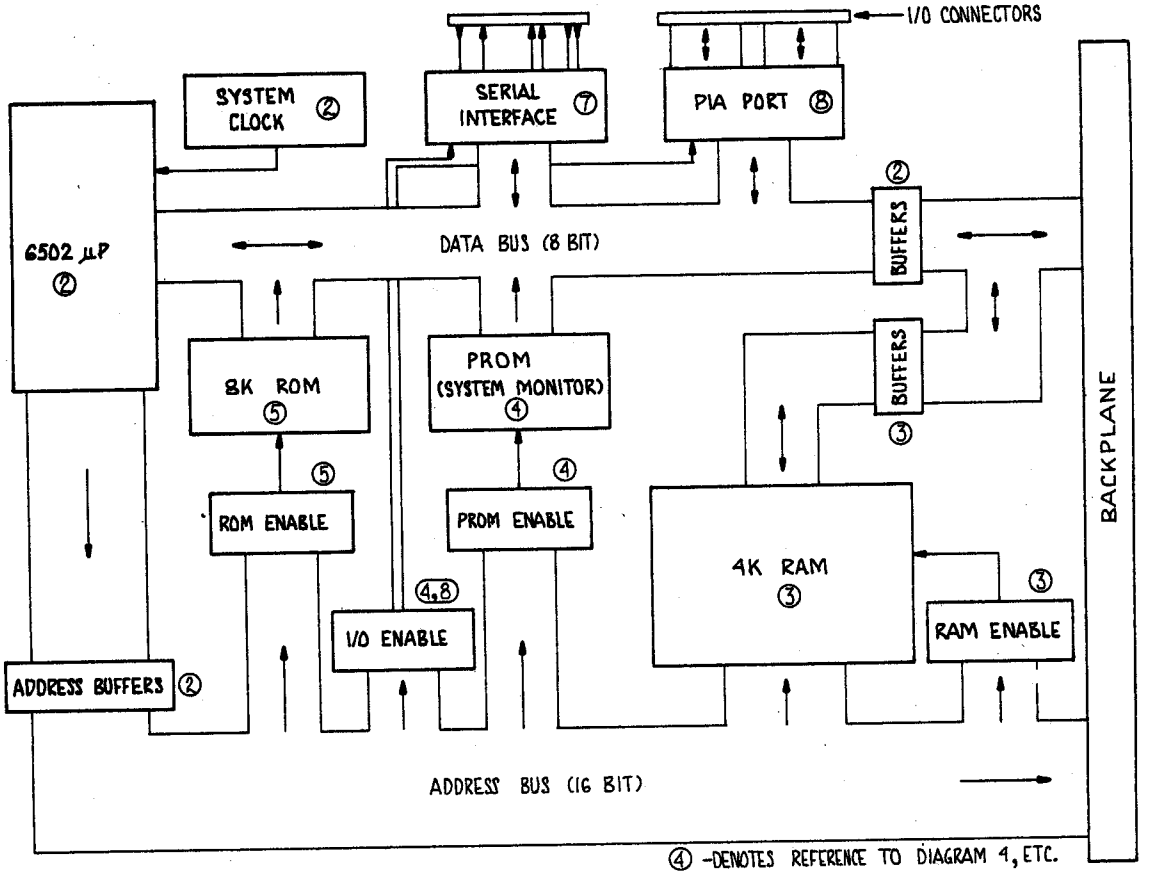


DIAGRAM 1 - SYSTEM OVERVIEW

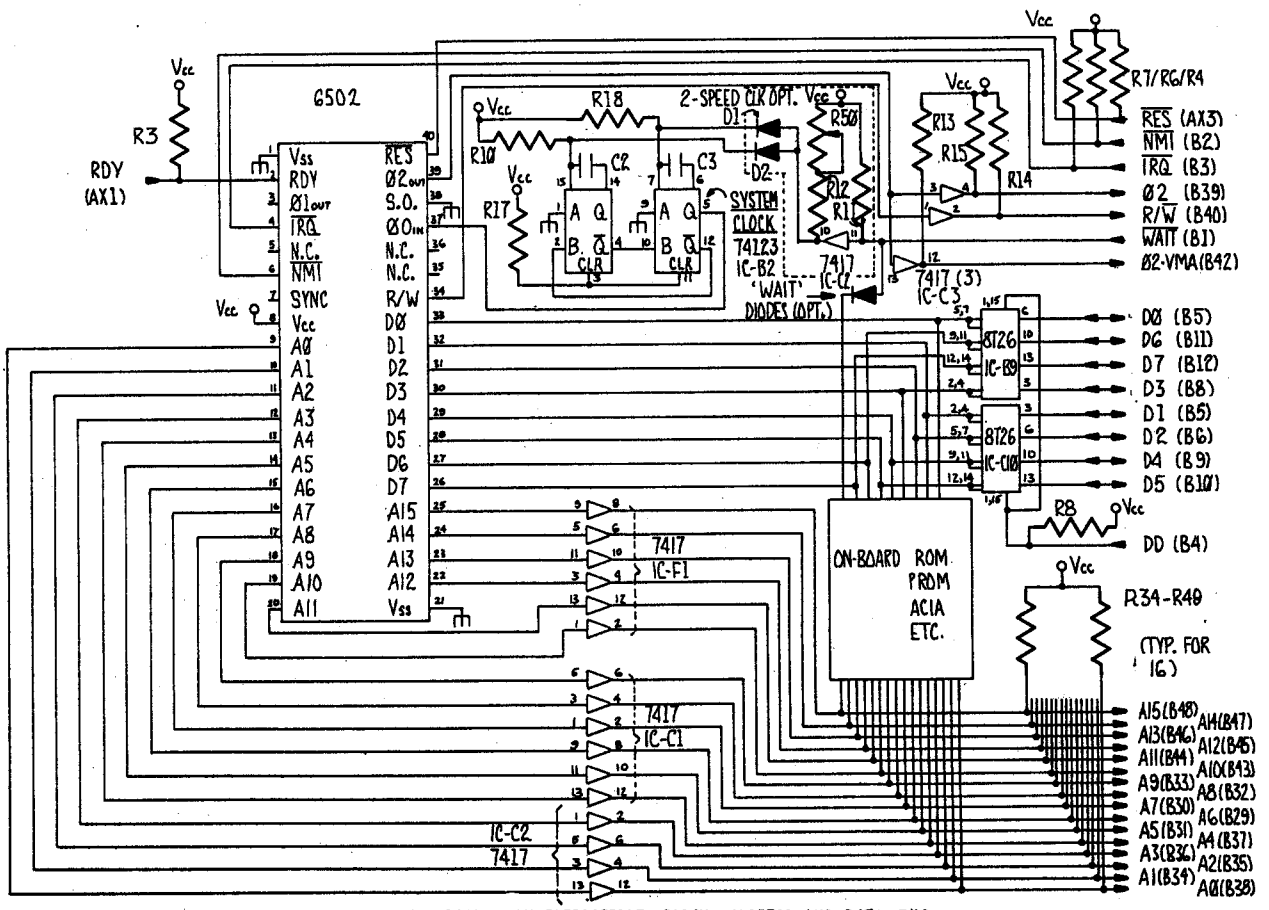


DIAGRAM 2 - MICROPROCESSOR, CLOCK, ADDRESS AND DATA BUS

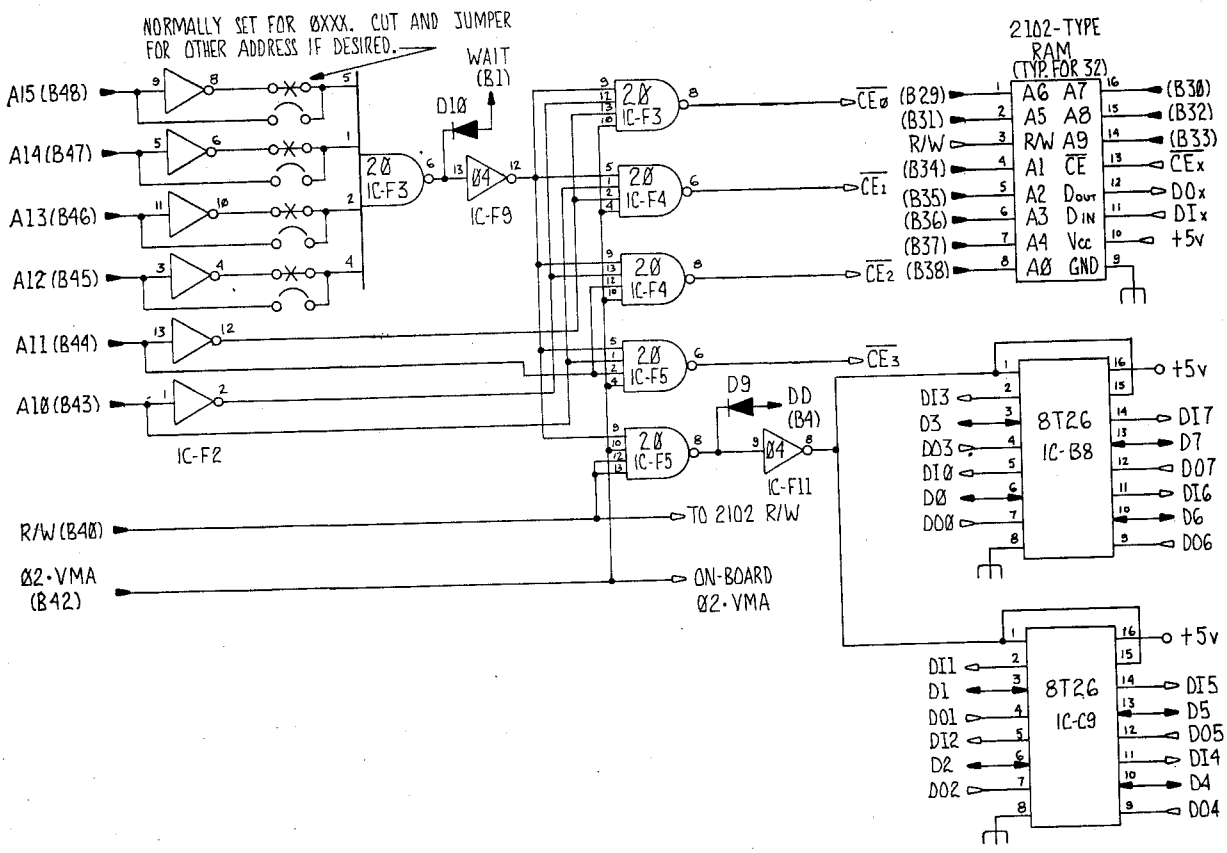


DIAGRAM 3- RAM IMPLEMENTATION

NOTES:

1. MODEL 500 WILL OPERATE WITH MONITOR PROMS IN ONE OF THREE CONFIGURATIONS, REQUIRING THE FOLLOWING BOARD MODIFICATIONS:
   - (A.) ONE PROM AT IC-A5, ADDRESS $\overline{FEXX}$+$\overline{FFXX}$: NO MODIFICATION.
   - (B.) TWO PROMS AT IC-A5, A6 , ADDRESS $\overline{FEXX}$, $\overline{FFXX}$ RESP: CUT AT K1, JUMPER J3 AND J4.
   - (C.) TWO PROMS AT IC-A5,A6, SWITCHABLE, ADDRESS $\overline{FEXX}$+$\overline{FFXX}$ BOTH: CUT AT K2, INSTALL SW-1.

IC-A4 MAY ALWAYS BE INSTALLED.

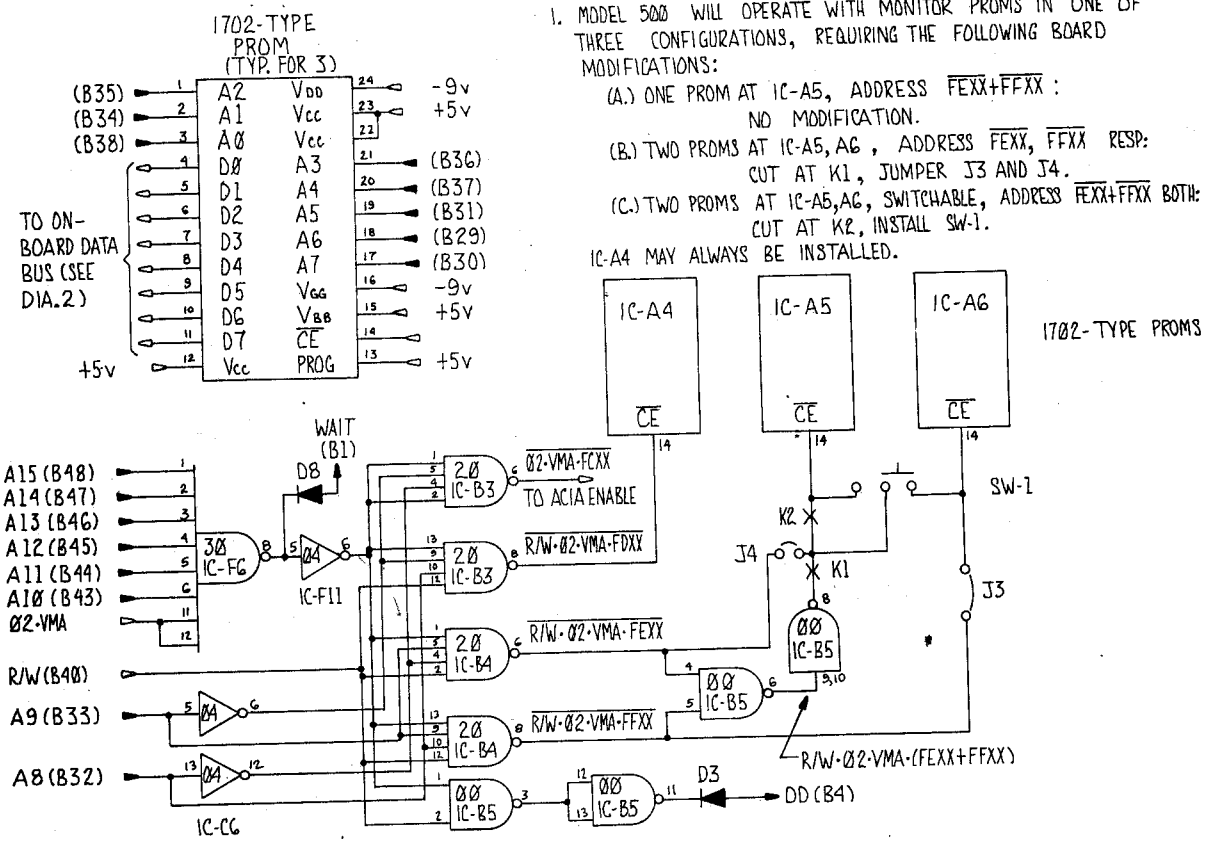
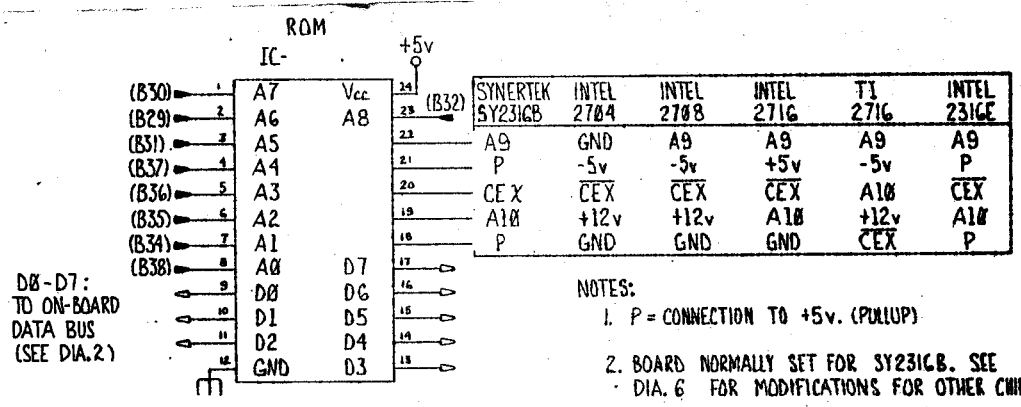


DIAGRAM 4- 1702-TYPE PROM IMPLEMENTATION



SYNERTEK SY2316B	INTEL 2704	INTEL 2708	INTEL 2716	TI 2716	INTEL 2316E
A9	GND	A9	A9	A9	A9
P	-5v	-5v	+5v	-5v	P
CEX	$\overline{CEX}$	$\overline{CEX}$	$\overline{CEX}$	A10	$\overline{CEX}$
A10	+12v	+12v	A10	+12v	A10
P	GND	GND	GND	$\overline{CEX}$	P

NOTES:

1. P = CONNECTION TO +5v. (PULLUP)
2. BOARD NORMALLY SET FOR SY2316B. SEE DIA. 6 FOR MODIFICATIONS FOR OTHER CHIPS.

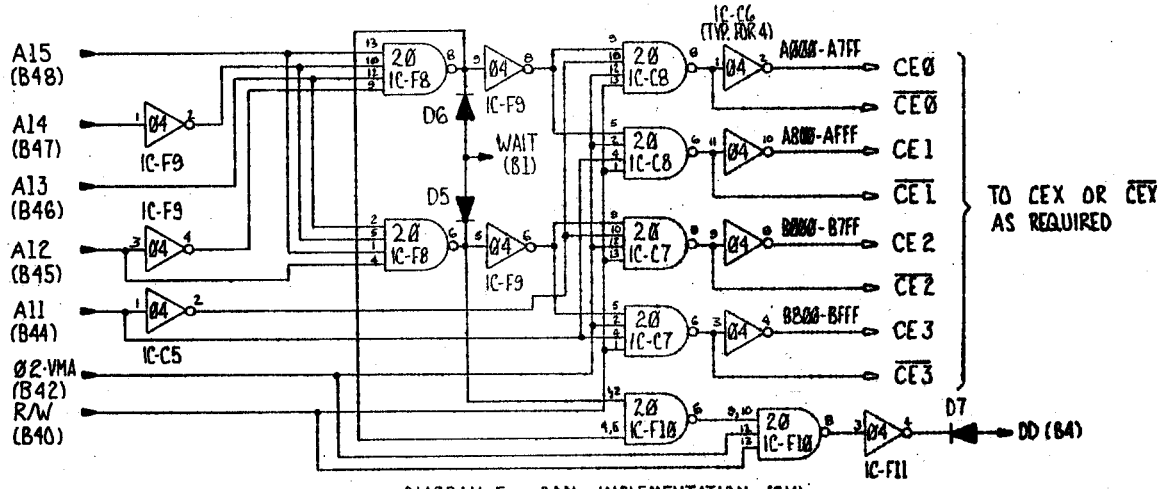
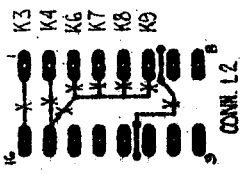
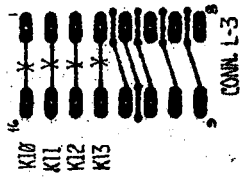


DIAGRAM 5- ROM IMPLEMENTATION (8K)

SYNERTEK SY2316B	INTEL 2704	INTEL 2708	INTEL 2716	TI 2716	INTEL 2316E
CUT	CUT	CUT	CUT	CUT	CUT
NONE REQ'D.	K-3 K-4 K-5 K-10 K-11 K-12 K-13 K-14	K-3 K-4 K-5 K-10 K-11 K-12 K-13	K-5 K-10 K-11 K-12 K-13	K-3 K-4 K-6 K-7 K-8 K-9 K-10 K-11 K-12 K-13	K-10 K-11 K-12 K-13
JUMPER	JUMPER	JUMPER	JUMPER	JUMPER	JUMPER
NONE REQ'D.	L2 p.7-p.6 p.8-p.1 p.9-p.2 L3 p.8-p.7 p.9-p.4 p.10-p.3 p.11-p.2 p.12-p.1	L2 p.7-p.6 p.8-p.1 p.9-p.2 L3 p.9-p.4 p.10-p.3 p.11-p.2 p.12-p.1	L2 p.7-p.6 L3 p.5-p.1 p.5-p.2 p.5-p.3 p.5-p.4	L2 p.8-p.1 p.9-p.2 p.11-p.6 p.12-p.5 p.13-p.4 p.14-p.3 L3 p.5-p.1 p.5-p.2 p.5-p.3 p.5-p.4	L3 p.9-p.4 p.10-p.3 p.11-p.2 p.12-p.1

NOTE: L3 p.9-p.4 means jumper pin 9 to pin 4 of connector L3, etc.





(ABOVE) CONNECTORS L2 AND L3 SHOWING CUT POINTS. VIEW FROM REAR OF BOARD.

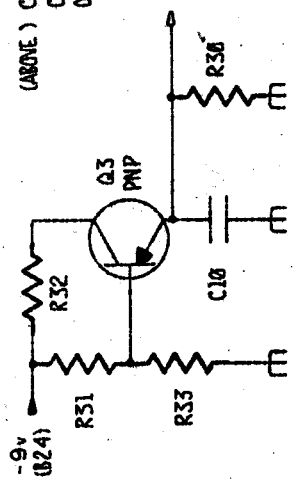


DIAGRAM 6- ROM JUMPER CONFIGURATION AND -5v POWER

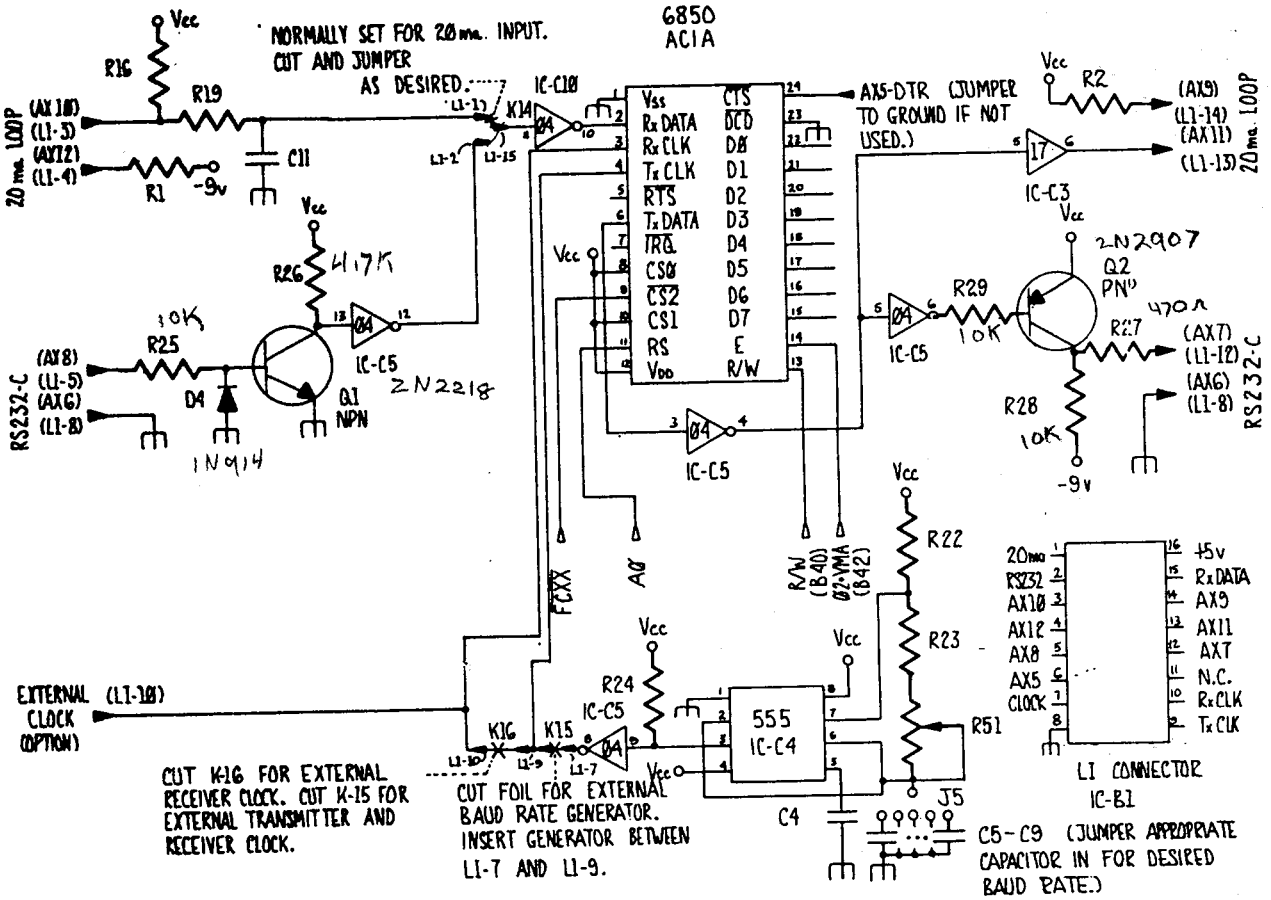
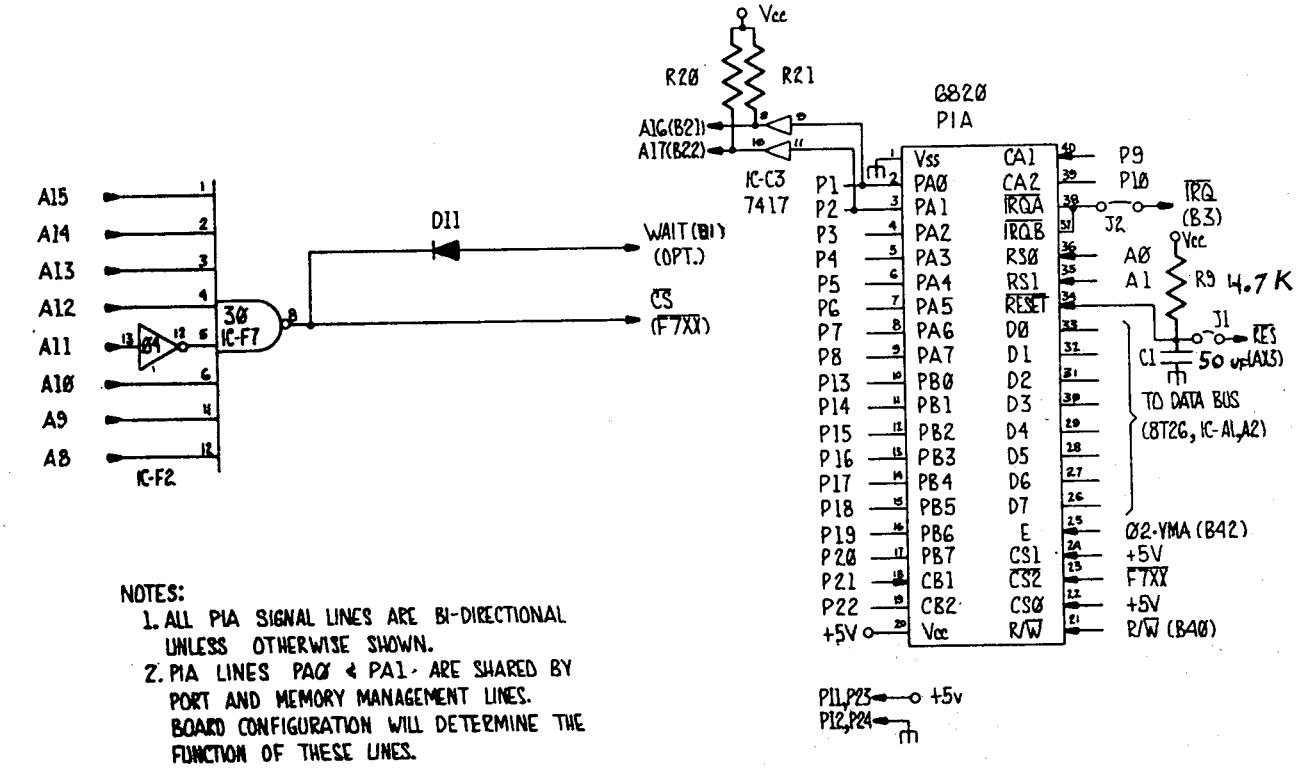
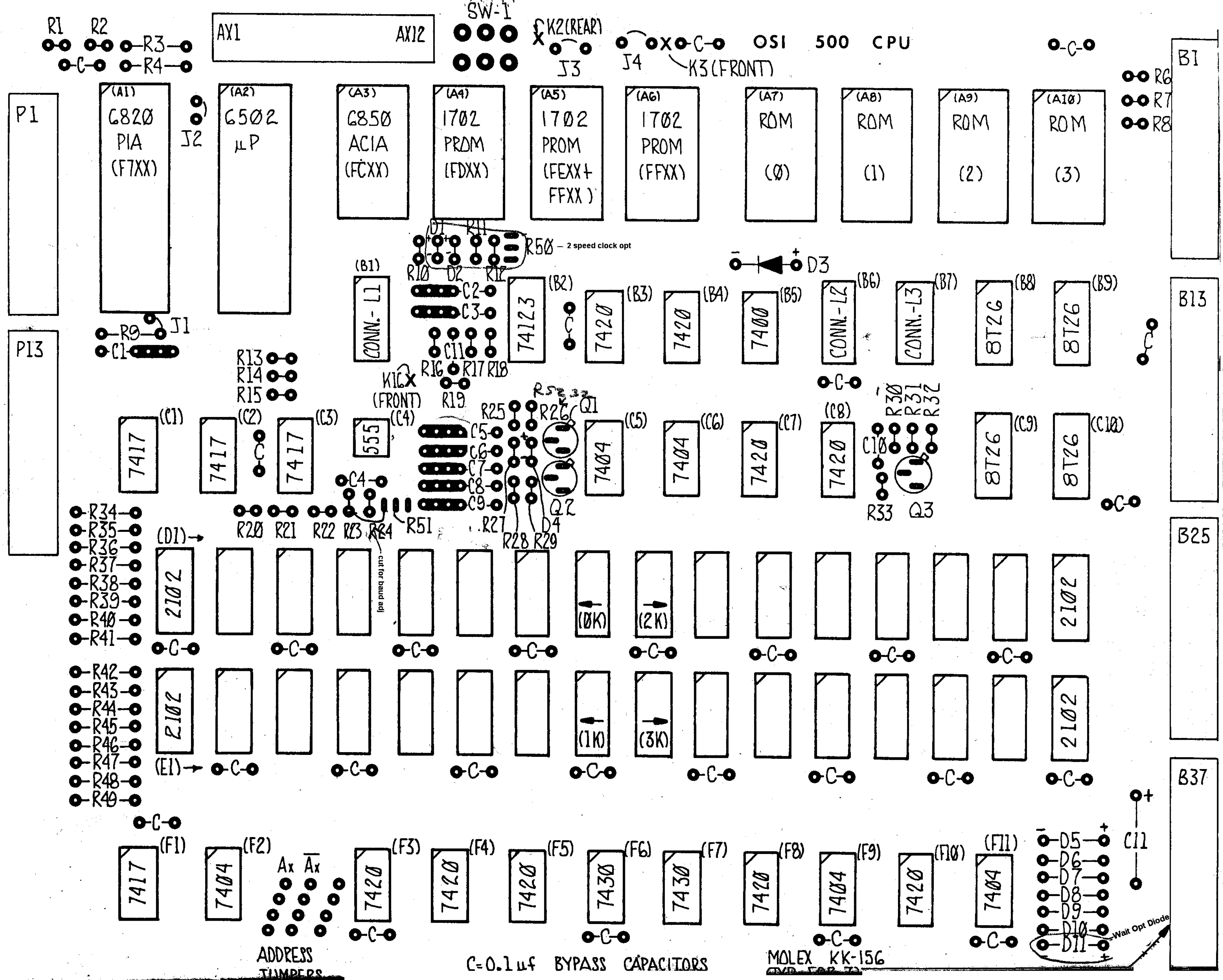


DIAGRAM 7- SERIAL INTERFACE

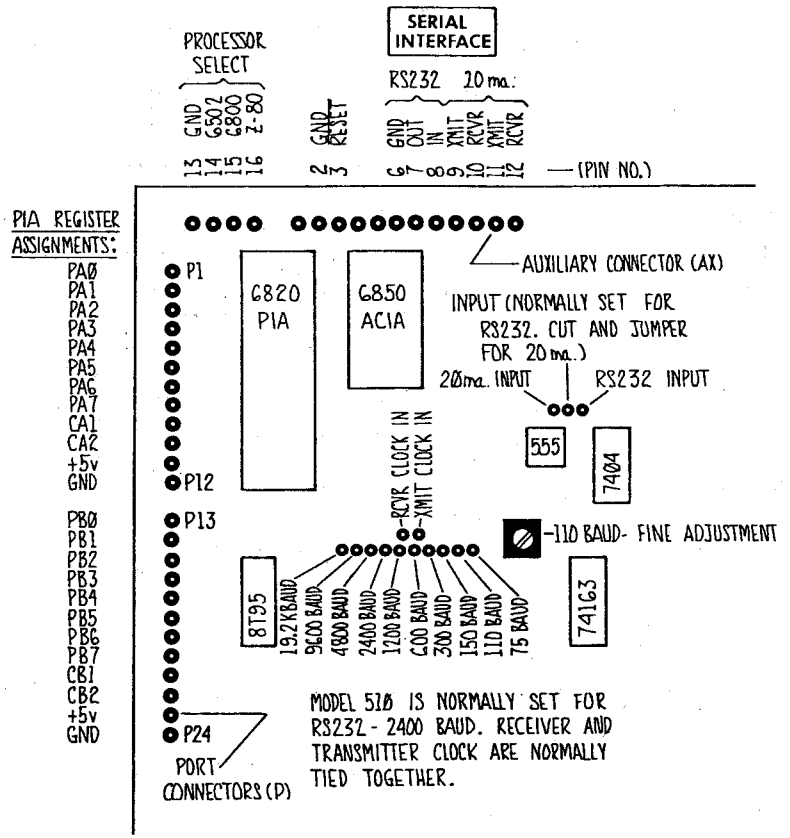


NOTES:
1. ALL PIA SIGNAL LINES ARE BI-DIRECTIONAL UNLESS OTHERWISE SHOWN.
2. PIA LINES PA0 & PA1 ARE SHARED BY PORT AND MEMORY MANAGEMENT LINES. BOARD CONFIGURATION WILL DETERMINE THE FUNCTION OF THESE LINES.

DIAGRAM 8- PIA PORT



OSI 500 CPU
SW-1
AX1
AX12
K2(REAR)
J3
J4
K3(FRONT)
(A1) 6820 PIA (F7XX)
(A2) 6502 µP
(A3) 6850 ACIA (FCXX)
(A4) 1702 PROM (FDXX)
(A5) 1702 PROM (FEXX+ FFXX)
(A6) 1702 PROM (FFXX)
(A7) ROM (Ø)
(A8) ROM (1)
(A9) ROM (2)
(A10) ROM (3)
P1
P13
B1
B13
B25
B37
J1
J2
R50 – 2 speed clock opt
D3
(B1) CONN.-L1
(B2) 74123
(B3) 7420
(B4) 7420
(B5) 7400
(B6) CONN.-L2
(B7) CONN.-L3
(B8) 8T26
(B9) 8T26
K1 (FRONT)
(C1) 7417
(C2) 7417
(C3) 7417
(C4) 555
(C5) 7404
(C6) 7404
(C7) 7420
(C8) 7420
(C9) 8T26
(C10) 8T26
Q1
Q2
Q3
cut for baud adj
(D1)
(E1)
2102
(ØK)
(1K)
(2K)
(3K)
(F1) 7417
(F2) 7404
(F3) 7420
(F4) 7420
(F5) 7420
(F6) 7430
(F7) 7430
(F8) 7420
(F9) 7404
(F10) 7420
(F11) 7404
Ax Āx
ADDRESS JUMPERS
C=0.1µf BYPASS CAPACITORS
MOLEX KK-156
C11
Wait Opt Diode



(UPPER LEFT CORNER OF BOARD. VIEW FROM FRONT.)

MODEL 510 I/O CONNECTIONS

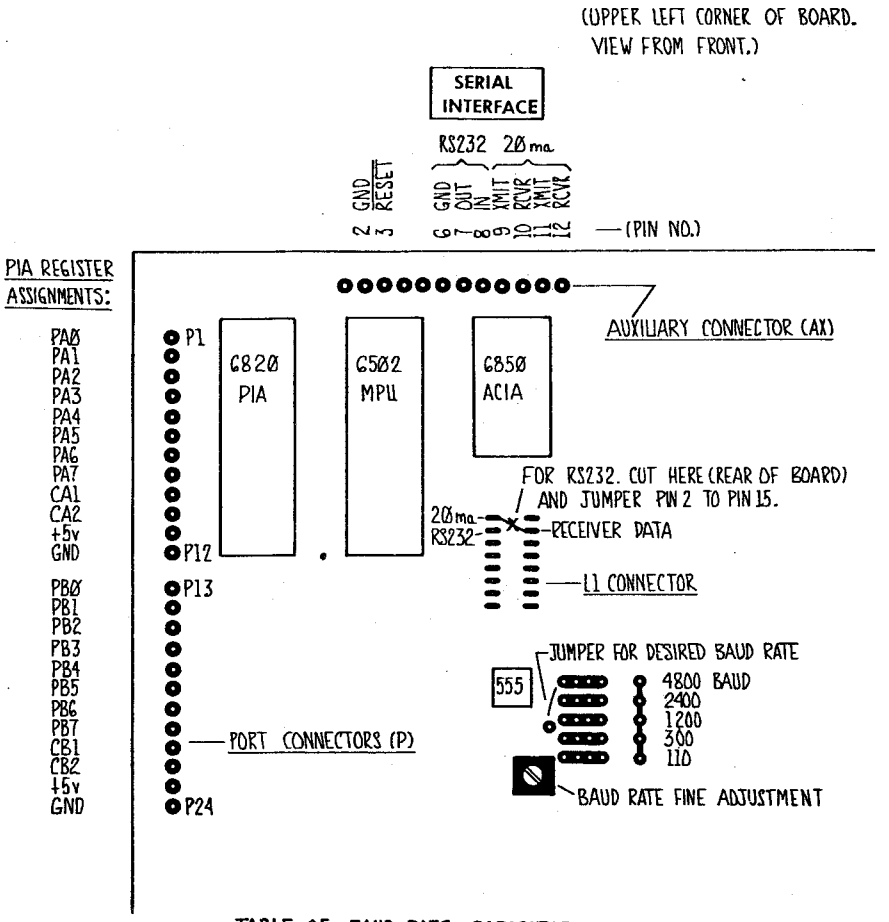


TABLE OF BAUD RATE CAPACITOR VALUES

	MIN	MID-RANGE	MAX
4800 BAUD	.001 µf	.002 µf	.0027 µf
2400	.0022	.0033	.0056
1200	.0045	.0068	.0110
300	.0179	.027	.0446
110	.0489	.082	.1216

MID-RANGE CAPACITANCE VALUES ARE RECOMMENDED, HOWEVER ANY VALUE BETWEEN MIN AND MAX MAY BE SUBSTITUTED. ALL VALUES ARE IN µf.

MODEL 500 I/O CONNECTIONS