MODEL 420C
MEMORY EXPANSION BOARD

OSI

OHIO SCIENTIFIC INSTRUMENTS

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OSI MODEL 420C MEMORY EXPANSION BOARD

Theory of Operation

The OSI Model 420C Board is the 400 series memory board. The board can be populated for 8 bit or 12 bit operation and two boards may be paralleled for 16 bit operation. The board can be populated with 1K, 2K, 3K, or 4K of 2102 type memories. The board can be used with any 2102 type memory with any access time, and is well suited for operation with ultra-high speed versions such as the 2102A-2 (250nsec. worst case).

The 420C has full battery backup capability via both of its two on-board Nicad AA cells and an external diode isolated input. The board has both logic level and switch operated write protect. It also has two additional address lines for memory management operation. This feature is particularly useful in 6502 systems which could be limited because of the limited stack and page zero memory space.

The operation of the board is broken down into four parts; address operation, data operation, battery back-up and special features.

Address Operation

Address lines A_0 through A_9 are fed to all memory chips all the time. This feature is important for high speed operation. Both the 6502 and 6800 microprocessors set up the current address during the clock Ø1 and then enable the memory during Ø2. By providing the addresses to memories during Ø1, the memory cycle time may be 100 to 400 nanoseconds longer than Ø2.

Lines A_{10} and A_{11} are decoded via inverters and nand gates into four distinct states to enable the appropriate 1K section of memory. The upper four address lines are available both high true and low true in

a jumper area at the lower right side of the board for use as inputs to a four input nand gate which generates the board enable signal ($\overline{BE}$). By appropriate jumpering, the address of the memory can be in any 4K increment from 0XXX to FXXX so that 16 4K memory boards can be added to a 6502 or 6800 system. The board enable signal is gated with system Ø2 and A_{10} and A_{11} to enable individual 1K memory segments on the board.

Data Operation

The 420C Memory Board is interfaced to the bi-directional data bus via 8T26 bus transceivers. These buffers split the bus into two unidirectional buses which feed the data inputs and data outputs of the 2102 memories. The 8T26s are normally in the listen mode, that is, they are normally passing data from the system bus into the data inputs of the 2102s. If the board is enabled, Ø2 is high and a read is present, the buffers change direction and the data direction line(DP) is pulled low, changing the direction of the 8T26s on the CPU board. Data then flows from the memory board to the processor. If slow memories are used, the board enable signal can be connected to B_1 via a diode (D_1) to bring the system wait line low, stretching Ø2.

The battery backup feature of the 420 board is optional and must be used with some care. First of all, the battery backup mode can only be used with 2102 type memories which are characterized by low power standby mode operation. P2102AL and 2102LFPC chips are characterized for this mode of operation, but many other 2102 type memories are not! Battery backup works by applying approximately 2 volts to the 2102s and their chip enables in case of a power failure. To keep the battery from

attempting to operate the rest of the computer, the memory must be isolated from the +5 power source. This is accomplished by D_3 on the 420 board. This complicates matters because the diode has a .7 volt drop which, if used with a low +5 supply, will yield only about 4.1 volts to the memories. P2102ALs will operate at this voltage but will be much slower than specified (350 nanoseconds) when battery backup is not actuated. SW_2 bypasses the isoloation diode for normal operation. The board accepts two common Nicad AA cells which feed the board via D_5 and are trickle charged via R_{11}. The batteries are out of the circuit when SW_2 is in the normal position. The batteries require about 50 hours to charge in circuit and can be trickle charged indefinitely without danger of overcharging. If SW_2 is in the battery backup mode, the two AA cells will automatically take over in the event of a power failure and hold data for approximately three hours with OSI supplied memories.

An additional external backup power source can be connected to (P_1) instead of or to suppliment the on-board battery backup. The voltage should be between 4.5 and 2.0. This allows the user to connect 420C memory boards to an external power supply when the mainframe will be "down" for prolonged periods of time to save important programs such as operating systems!

The user should be careful not to leave Nicads fully discharged for prolonged periods or the batteries will be permanently damaged.

Special Features

Write Protect- Write operations can be inhibited by SW_1 or a logical low brought in on an unused bus pin. By using both write protect and battery backup, the board effectively operates as a PROM board with much more versatility and much lower cost.

Memory Management- The 420C has two additional address lines, i.e., 18 address bits. These bits can be exercised by OSI's memory management controller or by a simple PIA driven output port. This is very important on 6502 systems because of the inevitable page one and page zero conflicts by large programs and operating systems.

Using the 420C for Graphics Memory

Early 440 manuals refer to use of the 420B as graphics memory. The 420C can be used exactly as per these instructions by simply installing a jumper instead of D_3.

Installing the First 4K Memory Expansion Board

There are three ways to configure the system to accept the first 4K memory board (address range 0000-0FFF).

1. Worst Way: Build the standard 400 board, then, to expand, install the fully decoded memory scheme on page A-7 of the manual. Omit the lowest addressed 1K of memory on the 420 board set for 0XXX. Install a line from the chip enable of the 2102 memories on the 400 board (pin 13 of IC-C through J) to the input of the 1K pull up R_2 on the 420C board. This should be done via an unused bus line such as B_{13}.

2. Better Way: Socket the eight 2102 memories, IC-C through J and the two 7403s, IC-N and IC-O, when building the 400 board. Then, when you add the first 420 board, transfer the 2102s over to it and remove the 7403s. This eliminates using the fully decoded memory scheme!

3. Best Way: Build a 420 board in conjunction with the 400 board. Place the 2102 memories on the 420 board right from the start. Omit IC-M, IC-N, and IC-O also from the 400 board.

420C PARTS LIST

1	Model 420C Memory Expansion Board
2	8T26 Buffers (3 for 12 bit operation)
8 to 48	2102 Type Memories
3	7420
2	7404
1	7430
1	7417
1	IN914 (D_2)
19	Bypass Capcitors .1uf Typical
1	25uf Electrolytic
9	1K 1/4 watt R_1- R_9

Battery Backup (Optional)

1	25uf Capacitor
3	IN4001 (D_3, D_4, D_5)
1	Switch (SW_2)
1	100 ohm 1/4 watt (R_{11})

Write Protect (Optional)

1	Switch (SW_1)

Accessories Not Supplied by OSI (Optional)

4 or 5	Molex KK-156 Connectors (Supplied with Backplane Boards)
2	Nicad "AA" Cells
1	LED and 100 ohm Resistor (R_{10})
1	Wait Diode IN914 (D_1)

Diagram 2. BUS PINOUT

B_1	Wait (optional)
B_2	No Connection
B_3	No Connection
B_4	Data Direction
B_5	D_0
B_6	D_1
B_7	D_2
B_8	D_3
B_9	D_4
B_{10}	D_5
B_{11}	D_6
B_{12}	D_7
B_{13}	D_8
B_{14}	D_9
B_{15}	D_{10}
B_{16}	D_{11}
B_{17}	No Connection
B_{18}	No Connection
B_{19}	No Connection
B_{20}	Write Protect- Optional
B_{21}	A_{17}- Optional
B_{22}	A_{16}- Optional
B_{23}	No Connection
B_{24}	No Connection
B_{25}	+5
B_{26}	+5
B_{27}	Ground
B_{28}	Ground
B_{29}	A_6
B_{30}	A_7
B_{31}	A_5
B_{32}	A_8
B_{33}	A_9
B_{34}	A_1
B_{35}	A_2
B_{36}	A_3
B_{37}	A_4
B_{38}	A_0
B_{39}	No Connection
B_{40}	R/W
B_{41}	No Connection
B_{42}	Ø2·VMA
B_{43}	A_{10}
B_{44}	A_{11}
B_{45}	A_{12}
B_{46}	A_{13}
B_{47}	A_{14}
B_{48}	A_{15}

D_8 – D_{11}: Used Only in 12 Bit Systems

Assembly Instructions

Step 1. Carefully inspect the board for foil shorts. Back light the board and inspect the back side with a magnifying glass. Cut any bridges or shorts apart with a razor or exacto knife. Care at this stage will save a lot of grief later.

Step 2. Install all ICs. Remember to install only the two 8T26s to the left of the board for 8 bit operation. Remember that the low order bit of each 1024 word row is to the left of the board and that the lowest addressed 1K segment is the top row. The board may be populated as 1K, 2K, 3K, or 4K by 8 or 12 bits wide.

Step 3. Install 1K 1/4 watt resistors at R_1 through R_9.

Step 4. Install a 1N914 at D_2. If slow memories are used such that wait states are desired, install a second 1N914 at D_1.

Step 5. Install a switch at SW_1 if write protect is desired. Be careful not to get solder or flux in the switch itself. If flux gets in the switch, spray it with TV contact cleaner.

Step 6. Install Molex connectors if used.

Step 7. Install all 19 bypass capacitors labeled C in the parts overlay.

Step 8. (Address Strapping) For normal use, memory management addresses M_1 and M_2 should be jumpered to R_1 as per the parts overlay. The 4K memory board must be electronically located in the computer memory address space. This is accomplished by the use of four jumpers on the lower right side of the board. The pads the jumpers go between are specified on Diagram 1 and 2 as 1, 2, 3, 4, and A_{12}, $\overline{A}_{12}$, A_{13}, $\overline{A}_{13}$, A_{14}, $\overline{A}_{14}$, A_{15}, and $\overline{A}_{15}$. Four jumpers must be placed as follows: 1 to A_{12} or $\overline{A}_{12}$, 2 to A_{13} or $\overline{A}_{13}$, 3 to A_{14} or $\overline{A}_{14}$ and 4 to A_{15} or $\overline{A}_{15}$. Table 1 gives the address selection combinations.

Step 9. If battery backup is not desired, install a 25uf capacitor at C_1 and a jumper at D_3. If battery backup is desired, install 1N4001s at D_3, D_4, and D_5. Install a 25uf capacitor at C_2 and a 100 ohm 1/4 watt resistor at R_{11}. Install a switch at SW_2 and connector at P_1 (cut down version of standard connector).

Optionally install 2 AA cells at this point. Once the batteries are installed, the board should be treated with respect. An accidental short across power tapes could cause damage to the P.C. board and batteries.

An LED battery indicator can be installed at D_6 with a 100 ohm resistor at R_{10}. For best restults, the LED resistor should be jumpered to the battery side of D_5 as shown in Diagram 1 instead of M+ as the board is laid out for.

Note: Use only a high brightness RED LED.

Step 10. (System Installation) If the 420C Memory Expansion Board is used with a backplane board, install the four Molex connectors. Before connecting to the system, verify that the address space of the memory board is unused. Install the board and verify memory operation with the monitor.

Step 11. (Memory Testing) To verify proper operation of all bits of all memories, a memory test program should be run. Each memory location should be loaded and read with all possible numbers (00-FF). Memory test programs are available from OSI.

Operating Instructions

Remember not to write protect memory containing the stack which would inhibit even monitor operation!

If write protect and battery backup are both actuated, the memory data is virtually indestructible. However, if write protect is not actuated and the power fails, bits can be changed as the processor runs "wild" during power down and power up. This can be corrected by holding reset low when the +5 goes below 4.5 volts.

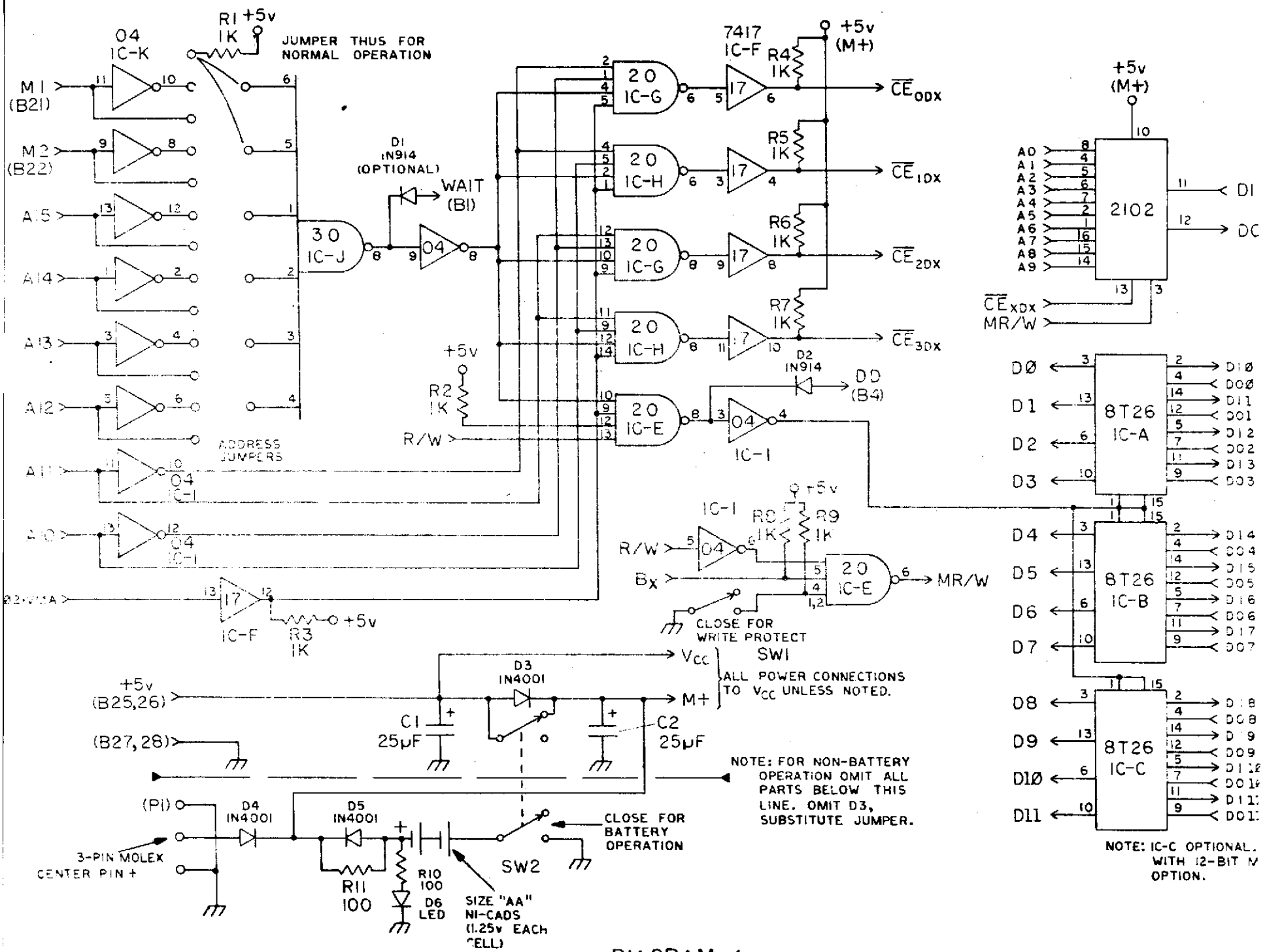
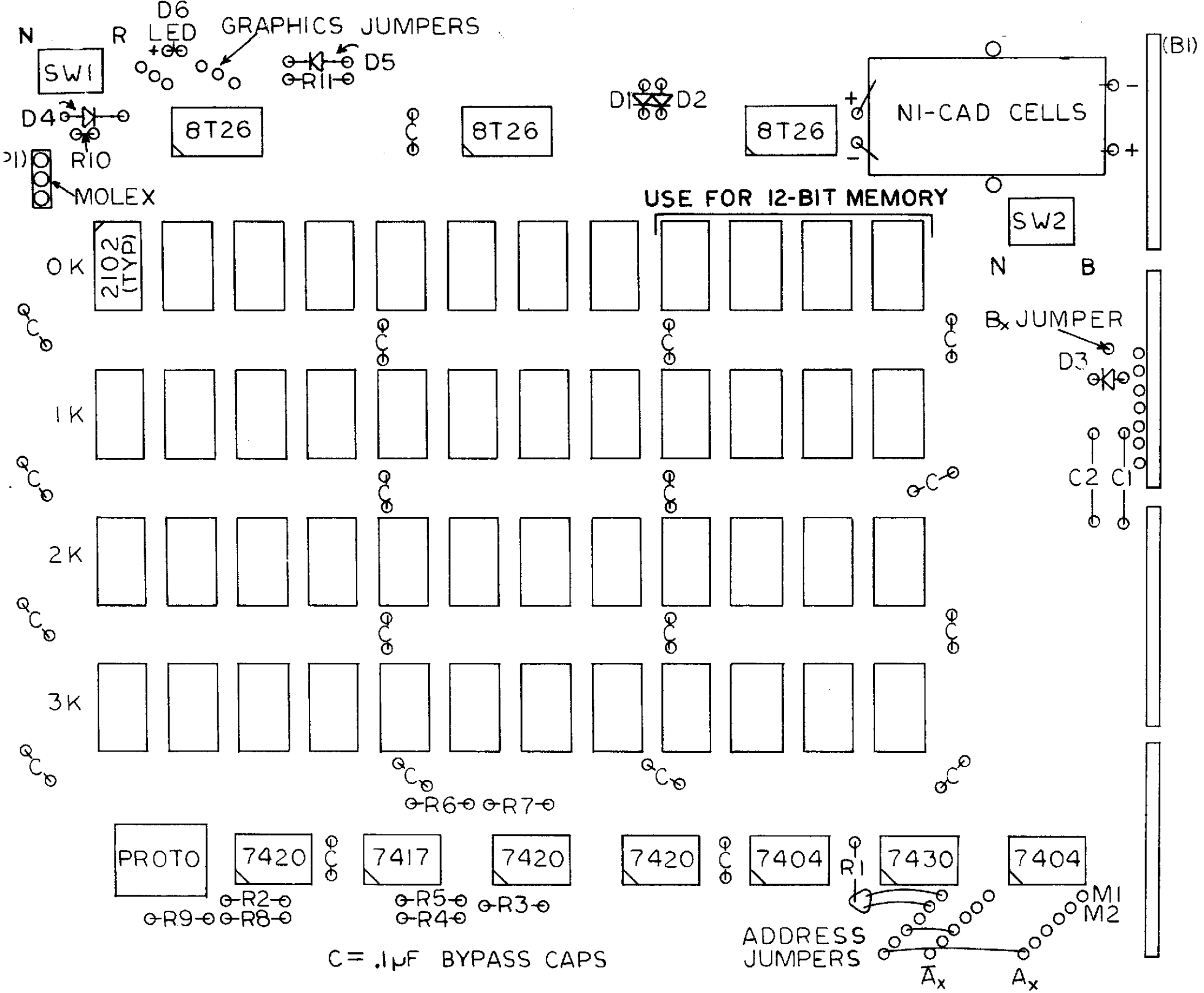
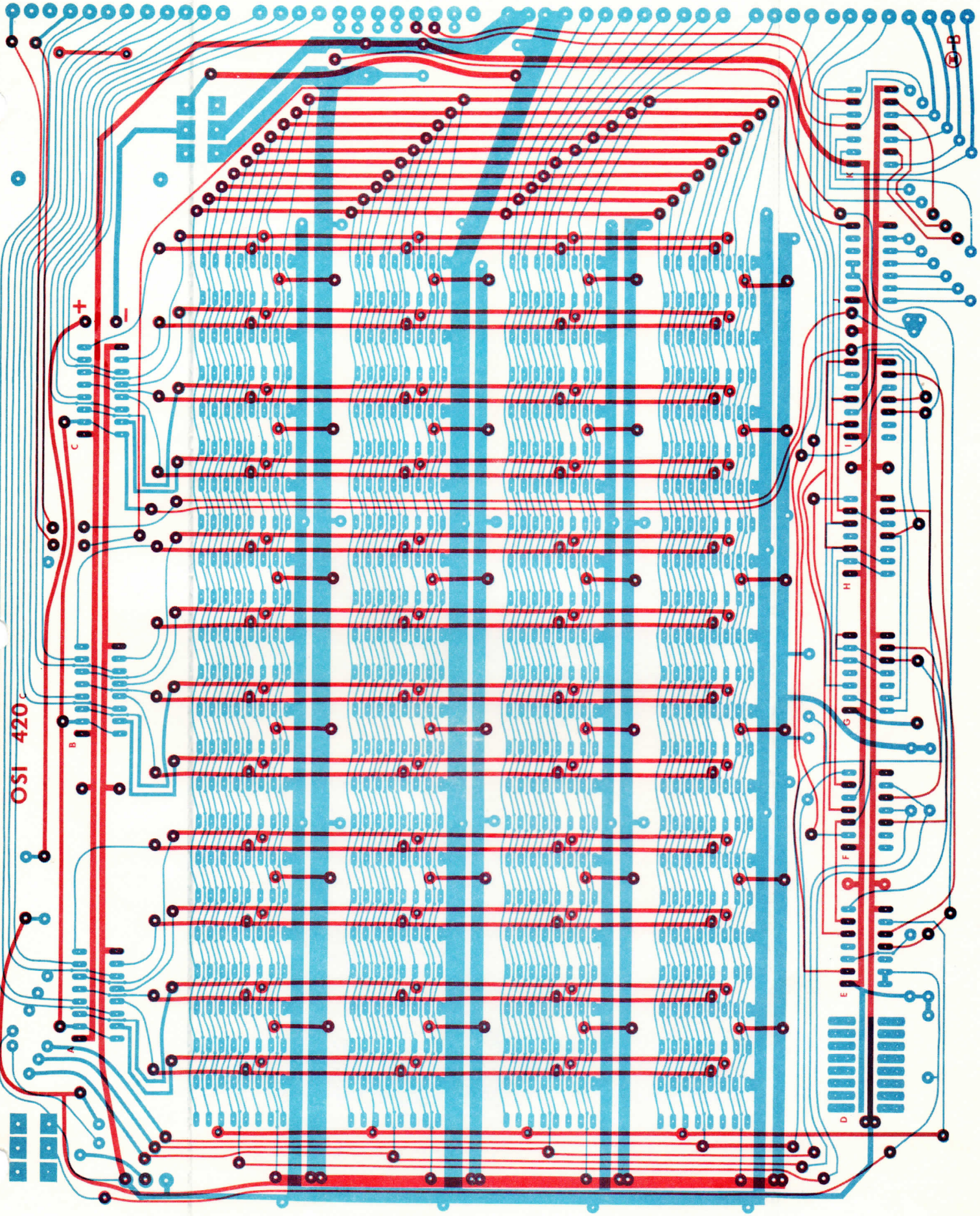

R1 +5v
1K
JUMPER THUS FOR NORMAL OPERATION
04 IC-K
M1 (B21)
M2 (B22)
A15
A14
A13
A12
A11
A10
ADDRESS JUMPERS
30 IC-J
D1 IN914 (OPTIONAL)
WAIT (B1)
04
+5v
R2 1K
R/W
20 IC-G
20 IC-H
20 IC-E
7417 IC-F
+5v (M+)
R4 1K
R5 1K
R6 1K
R7 1K
$\overline{CE}_{0DX}$
$\overline{CE}_{1DX}$
$\overline{CE}_{2DX}$
$\overline{CE}_{3DX}$
D2 IN914
DD (B4)
IC-1
+5v
IC-1
R8 1K
R9 1K
R/W
Bx
20 IC-E
MR/W
CLOSE FOR WRITE PROTECT SW1
IC-F
R3 1K
+5v
+5v (M+)
2102
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
DI
DC
$\overline{CE}_{XDX}$
MR/W
D0
D1
D2
D3
8T26 IC-A
D4
D5
D6
D7
8T26 IC-B
D8
D9
D10
D11
8T26 IC-C
NOTE: IC-C OPTIONAL. WITH 12-BIT M OPTION.
D3 IN4001
+5v (B25,26)
V_{CC}
M+
ALL POWER CONNECTIONS TO V_{CC} UNLESS NOTED.
C1 25µF
C2 25µF
(B27,28)
NOTE: FOR NON-BATTERY OPERATION OMIT ALL PARTS BELOW THIS LINE. OMIT D3, SUBSTITUTE JUMPER.
(P1)
D4 IN4001
D5 IN4001
3-PIN MOLEX CENTER PIN +
R11 100
R10 100
D6 LED
SIZE "AA" NI-CADS (1.25v EACH CELL)
SW2
CLOSE FOR BATTERY OPERATION

DIAGRAM 1

Table 1. Address Selection Combinations

Address	Jumper Locations 1 to:	2 to:	3 to:	4 to:
0XXX	$\overline{A}_{12}$	$\overline{A}_{13}$	$\overline{A}_{14}$	$\overline{A}_{15}$
1XXX	A_{12}	$\overline{A}_{13}$	$\overline{A}_{14}$	$\overline{A}_{15}$
2XXX	$\overline{A}_{12}$	A_{13}	$\overline{A}_{14}$	$\overline{A}_{15}$
3XXX	A_{12}	A_{13}	$\overline{A}_{14}$	$\overline{A}_{15}$
4XXX	$\overline{A}_{12}$	$\overline{A}_{13}$	A_{14}	$\overline{A}_{15}$
5XXX	A_{12}	$\overline{A}_{13}$	A_{14}	$\overline{A}_{15}$
6XXX	$\overline{A}_{12}$	A_{13}	A_{14}	$\overline{A}_{15}$
7XXX	A_{12}	A_{13}	A_{14}	$\overline{A}_{15}$
8XXX	$\overline{A}_{12}$	$\overline{A}_{13}$	$\overline{A}_{14}$	A_{15}
9XXX	A_{12}	$\overline{A}_{13}$	$\overline{A}_{14}$	A_{15}
AXXX	$\overline{A}_{12}$	A_{13}	$\overline{A}_{14}$	A_{15}
BXXX	A_{12}	A_{13}	$\overline{A}_{14}$	A_{15}
CXXX	$\overline{A}_{12}$	$\overline{A}_{13}$	A_{14}	A_{15}
DXXX	A_{12}	$\overline{A}_{13}$	A_{14}	A_{15}
EXXX	$\overline{A}_{12}$	A_{13}	A_{14}	A_{15}
FXXX	A_{12}	A_{13}	A_{14}	A_{15}


D6
LED
GRAPHICS JUMPERS
N
R
SW1
D5
R11
D4
R10
D1
D2
8T26
8T26
8T26
NI-CAD CELLS
(B1)
MOLEX
USE FOR 12-BIT MEMORY
SW2
N
B
0K
2102
(TYP)
1K
2K
3K
Bx JUMPER
D3
C2
C1
R6
R7
PROTO
7420
7417
7420
7420
7404
R1
7430
7404
R2
R9
R8
R5
R4
R3
M1
M2
ADDRESS
JUMPERS
$\overline{A}_x$
A_x
C = .1μF BYPASS CAPS


OSI 420C
+
-
A
B
C
D
E
F
G
H
I
J
K