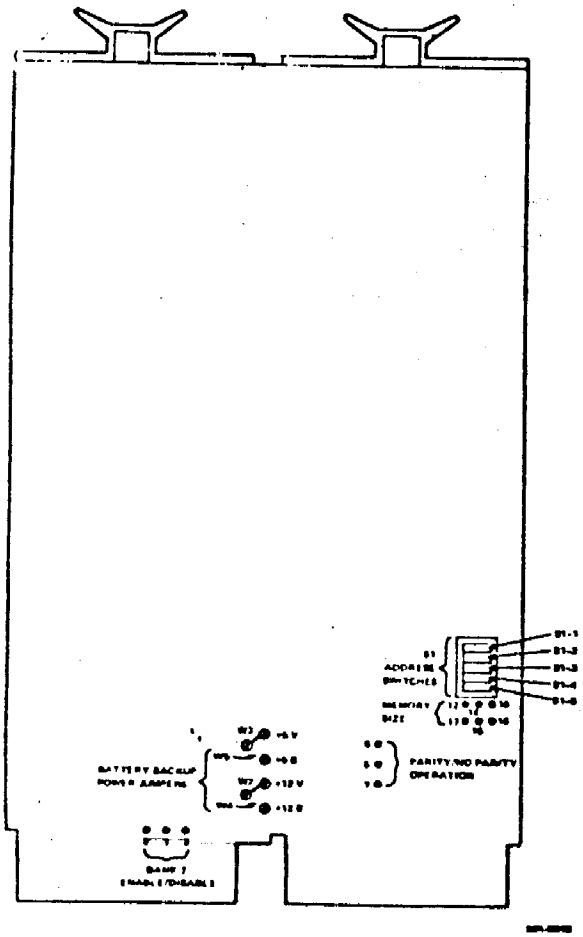
MSV11-DA,-DB,-DC,-DD Configuration Guide

(M8044-AA,-BA,-CA,-DA)

1. Address Selection

I = Inserted
R = Removed

Starting Address	Switch Settings S1-1	S1-2	S1-3	S1-4	S1-5	Banks Selected -DA	-DB	-DC	-DD
0	on	on	on	on	on	0	0-1	0-3	0-7
20000	on	on	on	on	off	1	1-2	1-4	1-10
40000	on	on	on	off	on	2	2-3	2-5	2-11
60000	on	on	on	off	off	3	3-4	3-6	3-12
100000	on	on	off	on	on	4	4-5	4-7	4-13
120000	on	on	off	on	off	5	5-6	5-10	5-14
140000	on	on	off	off	on	6	6-7	6-11	6-15
160000	on	on	off	off	off	7	7-10	7-12	7-16



Note: 1) The present range of addressing for the LSI-11 is through bank 7. Bank 7 is normally reserved for peripheral devices. Therefore, the MSV11-D series memories are designed to disable themselves whenever a received address is a bank 7 address (i.e. bus signal BBS7 is asserted). Because of this feature, it is not necessary, nor is it possible, to disable any banks of memory which overlap bank 7 or higher.

2) Rocker switch positions are defined by depressing the desired side of the rocker, not by the red line on the opposite side of the rocker.

3) Bus Address Lines (BAD) 16 and 17 are used by the MSV11-D memories. These lines are properly terminated by Revision E KD11-F CPU's and by the KD11-HA CPU. However, Revision C and D KD11-F's do not terminate these lines. If BAD 16 and 17 are not terminated, erratic operation will occur. With a Revision C and D KD11-a terminator module such as the TEV11 REV11-A or the BCV1B cable set must be used.

2. Enabling the Lower 2K of Bank 7

It is possible to enable the addressing of the 28K - 30K space (lower 2K of bank 7) on the MSV11-D if the board address covers bank 7, as follows:

enable 28 - 30K	disable 28 - 30K
Remove the jumper between pin 1 and pin 3	Remove the jumper between pin 1 and pin 2
Insert a jumper between pin 1 and pin 2	Insert a jumper between pin 1 and pin 3

Note: The lower 2K of bank 7 is normally reserved for bootstrap loaders or peripherals. Use of memory in this area is not supported by Digital Software and conflicts with the REV11 boot address space.

3. Battery Backup Capability

Mode	W2	W3	W4	W5
Refresh logic powered by separate battery supply	R	R	I	I
Refresh logic powered by backplane power	I	I	R	R

4. Misc.

Pins 5 and 7 are jumpered at the factory. Pin 6 is not connected.* This factory configuration must not be changed.

Pins 10, 12, 14, 15, 16, 17 are jumpered as follows:

Memory Size	Pins Connected	
4K(-DA)	17 and 15	17 and 14
8K(-DB)	17 and 15	12 and 14
16K(-DC)	16 and 15	16 and 14
32K(-DD)	16 and 15	10 and 14

These jumpers should not be changed. Banks of on-board memory cannot be changed, except a 32K memory can be rejumpered to respond as a 16K memory, or an 8K memory can be jumpered to respond as a 4K memory. Note that no memory boards may be upgraded in size by repopulating the memory chips. Additional components on the board must be changed, and this will result in voiding the warranty.

*Note: On some MSV11-D modules, a wire may be wire-wrapped to pin 6 and soldered to the etch board. Do not remove this wire under any circumstances.