HC55185 Ringing SLIC & AK2306/2306LV CODEC Evaluation Board User Guide Supplement

Application Note | **January 2002** | **AN9992**

Author: Don LaFontaine

Functional Description

This application note is intended to supplement AMK's *Evaluation Board User's Guide*. The user's guide describes the Evaluation Board System and use of its software. The system includes the evaluation board and control software 2306.exe.

A good understanding of the material in the user's guide is a prerequisite to this application note. For a detailed engineering analysis of the reference design using the HC55185 and AK2306/2306LV, see *Application Note AN9991*.

The primary focus of this application note is to illustrate the system performance using a Wandel and Golterman (W&G) PCM4. Reference AKM's users guide for additional testing methods.

The AK2306/2306LV Evaluation Board is divided into two areas, one is the CODEC area and the other the SLIC area, as shown in Figures 1 & 2.

The CODEC area consists of one two-channel AK2306 /2306LV CODEC, DIP switches for setting the operating mode, on-board clock generation circuit for PCM I/F, various serial I/F access modes and FPGA for creating serial and PCM I/F signals.

The SLIC area consists of 12 switches to set the operation modes of the SLICs (six switches / SLIC), jumpers for changing the signal path and terminal connectors for connection to the two-wire port.

This application note will first evaluate the DC performance of the system by configuring the jumpers and hardware for the External Clock/PC Control mode. Figure 1 shows the required connection between the Evaluation Board, PC and PCM4 tester.

If the user prefers to evaluate the AC performance first, then skip to Test #5.

Verifying Basic Operation

The operation of the Evaluation Board can be verified by performing the following tests:

1. Normal Loop Feed Verification
   - Tip & Ring Voltage Forward Active State, On Hook
   - Tip & Ring Voltage Forward Active State, Off Hook
   - Tip & Ring Voltage Reverse Active State, On Hook
   - Tip & Ring Voltage Reverse Active State, Off Hook
2. Loop Supervisory Detection
   - On Hook & Off Hook Test
   - Tip Open State, Ground Key Test
   - Forward Loopback Test
3. Ringing Verification
4. Emulation of Phone Conversation
5. Gain Verification–Total System Gain (Digital to Digital)
6. Variable Gain/Frequency
   - Receive Gain (Digital to Analog)
   - Transmit Gain (Analog to Digital)
7. Total Distortion–Receive Gain (Digital to Analog)

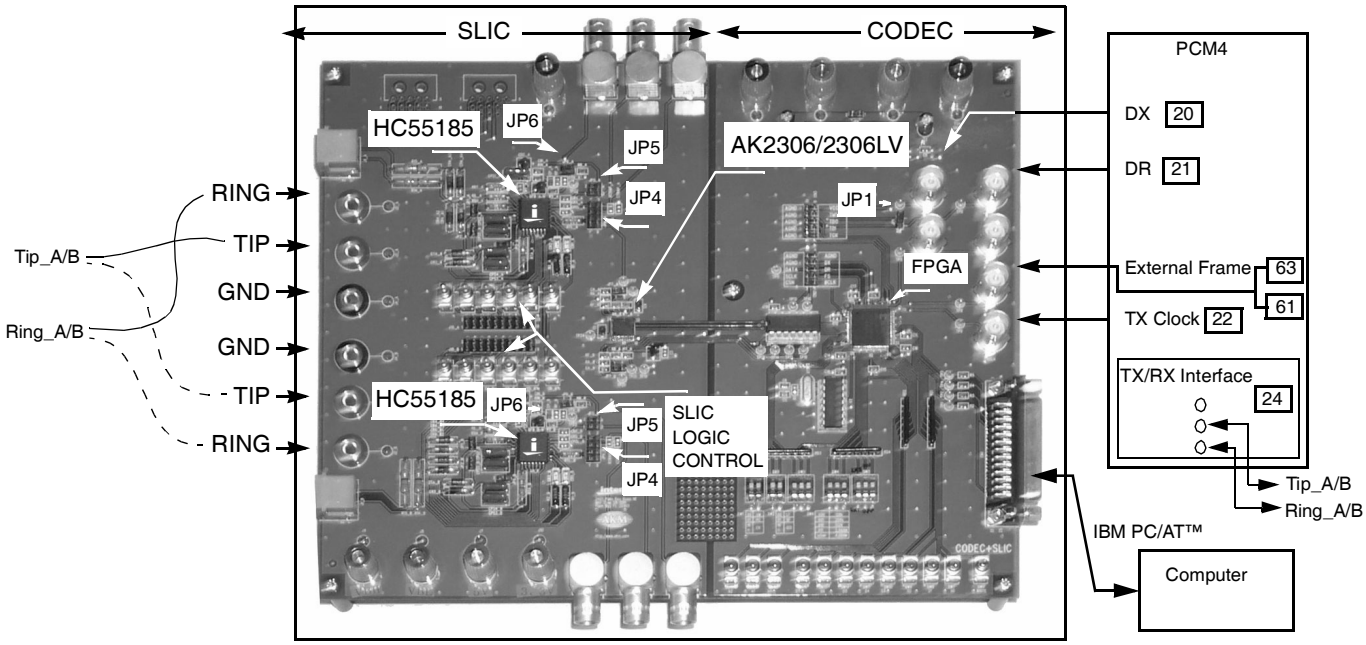


FIGURE 1. AK2306/2306LV EVALUATION BOARD CONNECTION TO PCM4 AND COMPUTER

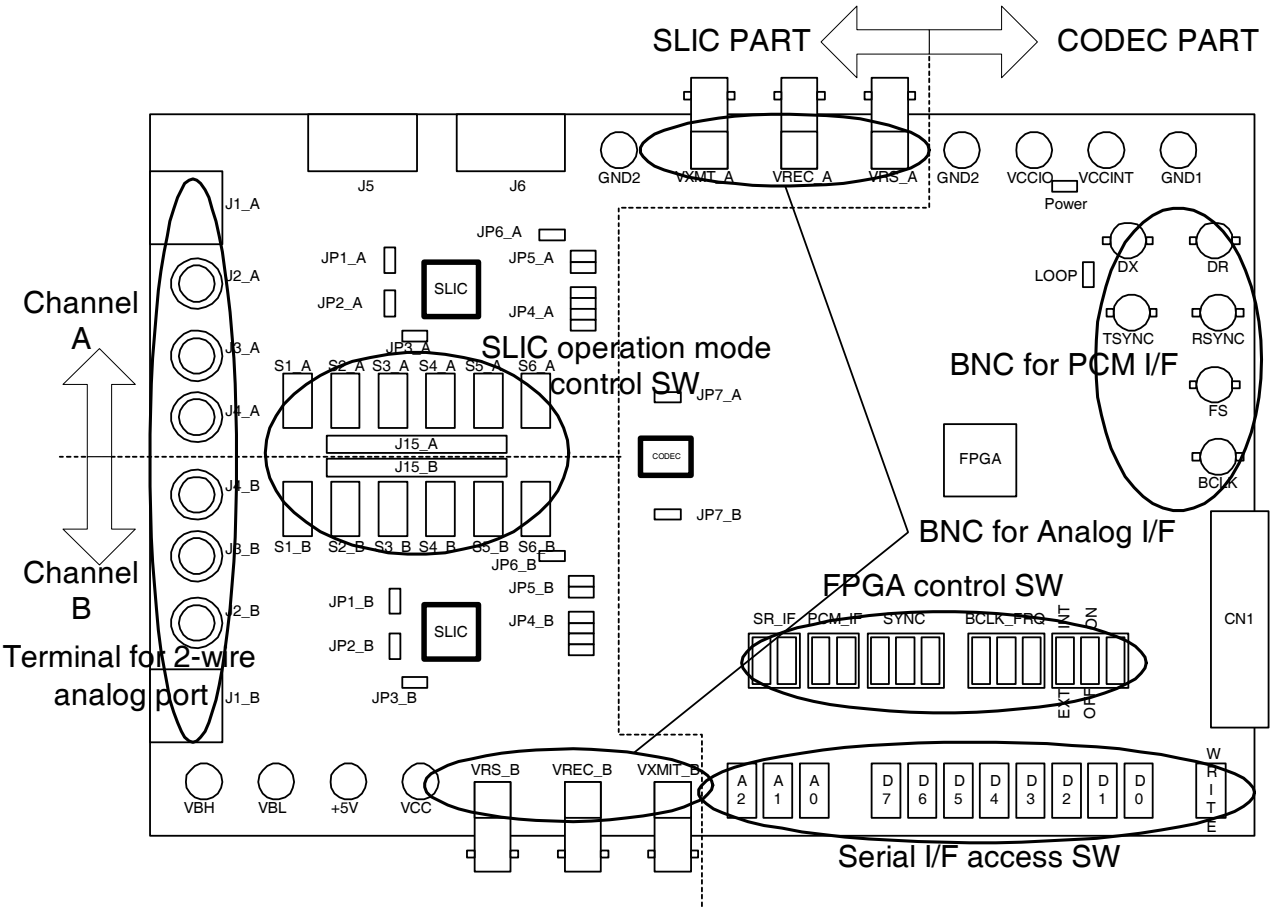


FIGURE 2. AK2306/2306LV MOTHER BOARD CONNECTIONS

HC55185 SLIC

The HC55185 is optimized to match a 600Ω line impedance, have a ring trip threshold of 90mA, a switch hook threshold of 12mA, loop current limit of 24.6mA and a transient current limit of 100mA.

Programming of the logic state of the HC55185 is performed by the toggle switches SW1 through SW6. Table 1 lists the switch name (referenced to the SLIC data sheet), switch number (reference to the PCB board layout), and the switch function. The logic states of the HC55185 are shown in Table 2.

TABLE 1. TOGGLE SWITCHES FOR SLIC

SWITCH NAME	SWITCH No.	FUNCTION
F2	S1	Logic control input
F1	S2	Logic control input
F0	S3	Logic control input
E0	S4	Selects between SHD,GKD and RTD detectors (Table 2)
$\overline{SWC}$	S5	Logic control for uncommitted switch. Logic 0 switch on.
BSEL	S6	Selects either the high or low battery supply for the HC55185 Logic 0 selects low battery Logic 1 selects high battery

TABLE 2. HC55185 OPERATING MODES

MODE	F2	F1	F0	E0=1	E0=0
Low Power Standby	0	0	0	SHD	GKD
Forward Active	0	0	1	SHD	GKD
Unbalanced Ringing	0	1	0	RTD	RTD
Reverse Active	0	1	1	SHD	GKD
Ringing	1	0	0	RTD	RTD
Forward Loop Back	1	0	1	SHD	GKD
Tip Open	1	1	0	SHD	GKD
Power Denial	1	1	1	n/a	n/a

AK2306/2306LV Evaluation Board

The AK2306/2306LV Evaluation Board provides a way to evaluate the operation of AKM's CODEC and Intersil's HC55185 Ringing SLIC. Figure 2 shows the AK2306/2306LV evaluation board component locations.

The programming interface illustrated in this application note is once again the External Clock/PC Control mode. The function of jumpers JP1_A/B through JP7_A/B are explained in Table 3.

TABLE 3. JUMPER CONNECTIONS

JUMPER	FUNCTION
JP1_A/B	Connects uncommitted switch of HC55185 (SW-) directly to the Ring terminal for loopback testing.
JP2_A/B	Connects uncommitted switch of HC55185 (SW+) through a 100Ω test load and diode to the Tip terminal for loopback testing.
JP3_A/B	Connects the VBH supply terminal to the VBL supply terminal for single supply applications.
JP4_A/B	Short 1 to 2: Connects external VRS input to HC55185 VRS input.
	Short 3 to 4: Connects external VRS input through TRAP (RC network) to HC55185 VRS input.
	Short 5 to 6: Connects AK2306/2306LV ringing output to the HC55185 VRS input.
	Short 7 to 8: Connects the AK2306/2306LV receive output to the HC55185 VRS input.
JP5_A/B	Short 1 to 2: Shorts the receive input of the HC55185 to ground. AK2306LV operation only.
	Short 3 to 4: Connects receive output of AK2306/2306LV to VRX input of HC55185.
JP6_A/B	Connects the HC55185 transmit output VTX to the AK2306/2306LV amplifier for transhybrid balance.
JP7_A/B	Connects the GRS_0/1 output of the AK2306/2306LV to the VFTN_0/1 input of the internal transhybrid amplifier (AMPT).

Getting Started

The following steps will configure the Evaluation board for testing the AK2306/2306LV and the HC55185 with the PCM4. The operation mode selected to access the AK2306/2306LV internal function registers are the **External Clock Mode** (PCM interface operation) and the **PC Control Mode** (Serial interface operation) using AKM proprietary software. For other methods to control the PCM interface and serial interface please reference AKM's user's guide.

The circuit schematics for the AK2306 and the AK2306LV are different (reference Figures 7 and 8). The reason for the different circuits is due to the low voltage (3.3V) operation of the CODEC and the need to provide sufficient gain to the two-wire loop. The smaller signal coming from the AK2306LV (3.3V operation) needs to be gained up through the SLIC, thus the variation in the two circuits.

The evaluation board was built with either the AK2306 (5V) CODEC or the AK2306LV (3.3V) CODEC (see Figure 1 for placement of CODEC on the board). The following is a check list to verify the correct components and jumper placement for the CODEC on your board.

AK2306 (5V) Circuit Configuration:

1. Verify that resistor RIN_A/B is open (left of JP6_A/B).
2. Verify that capacitor CIN_A/B is open (left of JP6_A/B).
3. Jumper JP5_A/B has pin 3 shorted to pin 4.
4. Verify RA_A/B is 120kΩ.
5. Verify RF_A/B is 120kΩ.
6. Verify R8_A/B is 49.9kΩ.

AK2306LV (3.3V) Circuit Configuration:

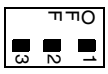
1. Verify that resistor RIN_A/B is 45.3kΩ (left of JP6_A/B).
2. Verify that capacitor CIN_A/B is 0.47µF (left of JP6_A/B).
3. Jumper JP5_A/B has pin 1shorted to pin 2.
4. Verify RA_A/B is 42.2kΩ.
5. Verify RF_A/B is 30.1kΩ.
6. Verify R8_A/B is 36.5kΩ.

The following evaluation applies for both the AK2306 (5V) or the AK2306LV (3.3V). Data presented was taken with the AK2306 (5V) evaluation board.

Configuring the board for operation:

1. Connect the IBM PC/AT (25 pin) cable between the evaluation board and your computer (Figure 1). Microsoft® Windows® 95 or higher should be installed (Microsoft® Windows NT® is not supported).
2. Connect the PCM4 to the evaluation board as shown in Figure 1.
3. Connect the power supplies to the supply jacks on the evaluation board.
4. Configure SW1, SW2, SW3, SW4, SW5 as shown in Table 4.

TABLE 4. FPGA CONTROL SWITCHES

SWITCH	POSITION
SW1 Selects PC mode	
SW2 PCM I/F data format set to Long Frame (LF)	
SW3 Sets the SYNC timing	
SW4 Selects internal BCLK frequency(2.048M)	
SW5 Selects normal operation, selects FS and BCLK from external source (BNC)	

5. Verify JUMPER positions as shown in Table 5 or 6.

TABLE 5. AK2306 (5V) JUMPER CONNECTIONS

JUMPER	FUNCTION
JP1 (CODEC side)	open
JP4 (CODEC side)	Short pin 1 to pin 2
JP4_A/B	Short pin 5 to pin 6
JP5_A/B	Short pin 3 to pin 4
JP6_A/B	Short pin 1 to pin 2
All Other Jumpers	Open

TABLE 6. AK2306LV (3.3V) JUMPER CONNECTIONS

JUMPER	FUNCTION
JP1 (CODEC side)	Open
JP4 (CODEC side)	Open
JP4_A/B	Short pin 5 to pin 6
JP5_A/B	Short pin 1 to pin 2
JP6_A/B	Short pin 1 to pin 2
All Other Jumpers	Open

6. Configure the HC55185 to be in the Forward Active mode using the SLIC Operation Mode Control Switches S1_A/B through S6_A/B. Reference Table 7 for switch positions. (Note: Switch position for logic 1 is towards the top of the board and logic 0 towards the bottom.)

TABLE 7. PROGRAMING HC55185 OPERATING MODES

HC55185 MODE	S1 (F2)	S2 (F1)	S3 (F0)	S4 (E0)	S5 ($\overline{SWC}$)	S6 (BSEL)
Low Power Standby	0	0	0	1	--	0
Forward Active	**0**	**0**	**1**	**1**	**--**	**0**
Unbalanced Ringing	0	1	0	1	--	1
Reverse Active	0	1	1	1	--	0
Ringing	1	0	0	1	--	1
Forward Loopback	1	0	1	1	--	0
Tip Open	1	1	0	1	--	0
Power Denial	1	1	1	1	--	0

7. Set the General Parameters of the PCM4 as shown in Table 12 (see Test #5).
8. Initialize the software by clicking on file 2306.exe. The internal register data of AK2306/2306LV will be initialized and the Register Map will be displayed (reference Table 8). Table 10 lists the Register functions in more detail.
9. On the computer terminal, entering a “1” will enable the user to program the AK2306/2306LVs: Receive and Transmit gains, exercise the CODECs power down controls, mute control, PCM interface select, PCM data channel select, A/μ-law select and Tone frequency select (reference Table 10).
10. Input the register address (column 1 of Table 10) in decimal form (0–7) for the function you wish to program. For example, if you wanted to change the receive gain for channel 0 you would type in ‘0’ and press return.
    NOTE: the default receive gain is 0dB.
11. To change the default values of any of the CODEC’s functions (Table 10), the user must input the corresponding number in a two-digit hexadecimal number. Table 9 can be used as a quick reference guide for programming the gains through the CODEC using hexadecimal numbers. Row one lists the available programming gains in dB, row two lists the corresponding two-digit hexadecimal number for that gain and row three lists the binary number that will appear on the computer screen after the user inputs the two-digit hexadecimal number.
12. The SLIC is now ready to be tested.

TABLE 8. REGISTER MAP

A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	TST13	TST12	-	GA0R4	GA0R3	GA0R2	GA0R1	GA0R0
0	0	1	TST11	TST10	-	GA1R4	GA1R3	GA1R2	GA1R1	GA1R0
0	1	0	TST9	TST8	-	GA0T4	GA0T3	GA0T2	GA0T1	GA0T0
0	1	1	TST7	TST6	-	GA1T4	GA1T3	GA1T2	GA1T1	GA1T0
1	0	0	TST5	TST4	MTCH1	MTCH0	PD	PDTN	PDCH1	PDCH0
1	0	1	TST3	TST2	TST1	TST0	TNFQ	ALAWN	SEL2B	PCMIF
1	1	0	Reserved							
1	1	1	Reserved							

TABLE 9. RERERENCE GUIDE TO CONVERT GAIN TO CORRESPONDING HEXADECIMAL NUMBER

Gain (dB)	6	5	4	3	2	1	0	-1	-2	-3	-4	-5	-6	-7	-8	-9	-10	-11	-12	-13	-14	-15	-16	-17	-18
Hex #	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18
Binary #	0 0 0 0 0	1 0 0 0 0	0 1 0 0 0	1 1 0 0 0	0 0 1 0 0	1 0 1 0 0	0 1 1 0 0	1 1 1 0 0	0 0 0 1 0	1 0 0 1 0	0 1 0 1 0	1 1 0 1 0	0 0 1 1 0	1 0 1 1 0	0 1 1 1 0	1 1 1 1 0	0 0 0 0 1	1 0 0 0 1	0 1 0 0 1	1 1 0 0 1	0 0 1 0 1	1 0 1 0 1	0 1 1 0 1	1 1 1 0 1	0 0 0 1 1

TABLE 10. REGISTER FUNCTIONS

Address	Bit	Name	Default	Function
000	0	GA0R0	0	**Receive gain adjustment on ch0** +6 to –18dB in 1dB steps 00000: +6dB 11xxx: -18dB
	1	GA0R1	1	
	2	GA0R2	1	
	3	GA0R3	0	
	4	GA0R4	0	
	5	-		
	6	0	0	Test mode Please write all “0”.
	7	0	0	
001	0	GA1R0	0	**Receive gain adjustment on ch1** +6 to –18dB in 1dB steps 00000: +6dB 11xxx: -18dB
	1	GA1R1	1	
	2	GA1R2	1	
	3	GA1R3	0	
	4	GA0R4	0	
	5	-		
	6	0	0	Test mode Please write all “0”.
	7	0	0	

TABLE 10. REGISTER FUNCTIONS (Continued)

Address	Bit	Name	Default	Function
010	0	GA0T0	0	**Transmit gain adjustment on ch0** +6 to -18dB in 1dB steps 00000: +6dB 11xxx: -18dB
	1	GA0T1	1	
	2	GA0T2	1	
	3	GA0T3	0	
	4	GA0T4	0	
	5	-		
	6	0	0	Test mode Please write all “0”.
	7	0	0	
011	0	GA1T0	0	**Transmit gain adjustment on ch1** +6 to -18dB in 1dB steps 00000: +6dB 11xxx: -18dB
	1	GA1T1	1	
	2	GA1T2	1	
	3	GA1T3	0	
	4	GA1T4	0	
	5	-		
	6	0	0	Test mode Please write all “0”.
	7	0	0	
100	0	PDCH0	0	**CODEC CH0,1 Power down control** 0: Power ON 1: Power OFF
	1	PDCH1	0	
	2	PDTN	1	**RING TONEGEN Power down control** 0: Power ON 1: Power OFF
	3	PD	0	**Full Power down** 0: Power ON 1: Power OFF
	4	MTDX0	0	**Mute control: VR0.VR1,DX pin** 0: Normal output 1: Mute
	5	MTDX1	0	
	6	0	0	Test mode Please write all “0”.
	7	0	0	
101	0	PCMIF	0	**PCM Interface select** 0: LF/SF 1: GCI
	1	SEL2B	0	**PCM data channel select** 0: CH0ÆB1 1: CH1ÆB1
	2	ALAWN	1	**A/μ-law select** 0: A-law 1: μ-law
	3	TNFQ	0	**Tone frequency select** 0: 16Hz 1: 20Hz
	4	0	0	Test mode Please write all “0”.
	5	0	0	
	6	0	0	
	7	0	0	
110	Reserved			
111	Reserved			

Test # 1 Normal Loop Feed Verification

This test verifies the correct tip and ring voltages in both onhook and offhook forward active and reverse active states. Loop current and ground key are also verified via on-board LEDs.

Discussion

The HC55185 is designed to have its most positive two-wire terminal (tip in the forward active state and ring in the reverse active state) fixed at a set voltage. The most negative two-wire terminal voltage is dependent upon the load across tip and ring and the programmable current limit.

Loop supervision is provided by either the switch hook or the ground key detectors. Loop status is observed by monitoring CR2_A/B LED on the board. The device may be operated from either high or low battery for on-hook transmission, during ringing and low battery for loop feed.

When operating from the high battery, the DC voltages at Tip and Ring are MTU compliant. The typical Tip voltage is -4V and the Ring voltage is a function of the battery voltage for battery voltages less than -60V as shown in Equation 1.

$$V_{RING} = V_{BH} + 4 \quad \text{(EQ. 1)}$$

Most applications will operate the device from low battery while off hook. The DC feed characteristic of the device will drive Tip and Ring towards half battery to regulate the DC loop current. For light loads, Tip will be near -4V and Ring will be near V_{VBL} + 4V. Figure 3 shows the DC feed characteristic.

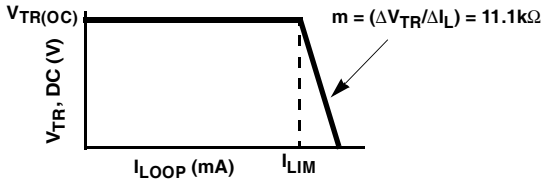


FIGURE 3. DC FEED CHARACTERISTIC

The point on the y-axis labeled $V_{TR(OC)}$ is the open circuit Tip to Ring voltage and is defined by the feed battery voltage.

$$V_{TR(OC)} = |V_{BL}| - 8 \quad \text{(EQ. 2)}$$

The Ground Key detector operation is verified by configuring the HC55185 in the tip open state and grounding the ring pin. Grounding the ring pin results in a current that triggers an internal detector that pulls the output of $\overline{DET}$ low causing current to flow through CR2_A/B, turning on the diode.

The Forward Loop Back mode provides test capability for the device. An internal signal path is enabled allowing for both DC and AC verification. The internal 600Ω terminating resistor has a tolerance of ±20%. **The HC55185 is intended to operate from only the low battery during this mode.**

When the forward loop back mode is initiated internal switches connect a 600Ω load across the outputs of the Tip and Ring amplifiers as shown in Figure 4.

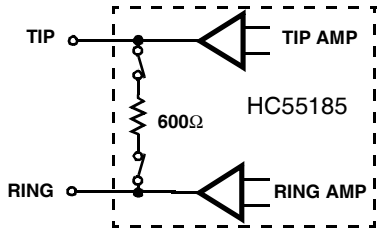


FIGURE 4. FORWARD LOOP BACK INTERNAL TERMINATION

When the internal signal path is provided, DC current will flow from Tip to Ring. The DC current will force $\overline{DET}$ low causing current to flow through CR2_A/B, turning on the diode.

Measuring Tip and Ring Voltages

1. Configure Hardware and Software as described in section titled *Getting Started*.
2. Configure the HC55185 to be in the forward active mode using the SLIC operation mode control switches S1_A/B through S6_A/B. Reference Table 7 for switch positions. (Note: Switch position for logic 1 is towards the top of the board and logic 0 towards the bottom.)
3. Measure the tip and ring voltages (reference Figure 1) and compare to those in Table 11 (onhook).
4. Terminate TIP and RING with a 600Ω load via the banana jacks or the RJ11 jack.
5. Measure tip and ring voltages with respect to ground and compare to those in Table 11 (offhook 600Ω).
6. Configure the HC55185 to be in the Reverse Active mode using the SLIC Operation Mode Control Switches S1_A/B through S6_A/B. Reference Table 7 for switch positions.
7. Disconnect the 600Ω load from across tip and ring.
8. Repeat steps 3, 4 and 5.

TABLE 11. TIP AND RING VOLTAGES

LOGIC STATE	R_L (Ω)	TIP VOLTAGE REFERENCED TO GND	RING VOLTAGE REFERENCED TO GND
Forward Active V_{BH} = -48V V_{BL} = NA V_{CC} = +5V	Onhook	-3.6 to -4.6	-17.2 to -21.1.0
	Offhook 600Ω	-4.6 to -5.6	-16.2 to -19.7
Reverse Active V_{BH} = -48V V_{BL} = NA V_{CC} = +5V	Onhook	-17.2 to -21.1.0	-3.6 to -4.6
	Offhook 600Ω	-16.2 to -19.7	-4.6 to -5.6

Test # 2 Loop Supervisory Detection

Verification of Switch Hook Detect

If previous test was Test #1, skip to step 3.

1. Configure Hardware and Software as described in section titled *Getting Started*.
2. Configure the HC55185 to be in the forward active mode using the SLIC operation mode control switches S1_A/B through S6_A/B. Reference Table 7 for switch positions.
3. With the SLIC in either the forward active state (Active F) or reverse active state (Active R), the LED CR2_A/B is on when tip and ring are terminated with 600Ω and off when tip and ring are an open circuit.
4. Disconnect the 600Ω load from across tip and ring.

Verification of Ground Key Detect

1. Configure the HC55185 to be in the Tip Open mode using the SLIC operation mode control switches S1_A/B through S6_A/B. Reference Table 7 for switch positions.
2. Grounding the ring terminal will verify ground key detect when the CR2_A/B diode turns on.

Verification of Forward Loopback

1. Configure the HC55185 to be in the forward loop back mode using the SLIC operation mode control switches S1_A/B through S6_A/B. Reference Table 7 for switch positions.
2. Verification of forward loopback operation is when both the CR2_A/B (SHD) and CR1_A/B (ALM) diodes turn on.

Test # 3 Ringing Verification

This test will demonstrate the ability of the AK2306/2306LV to ring a phone through the HC55185. A telephone is the only additional hardware required to complete this test.

Discussion

The HC55185 provides linear amplification to support a variety of ringing waveforms. A programmable ring trip function provides loop supervision and auto disconnect upon ring trip. The device is designed to operate from the high battery during this mode.

Architecture

The device provides linear amplification to the signal applied to the ringing input, V_{RS}. The differential ringing gain of the device is 80V/V. The circuit model for the ringing path is shown in Figure 5.

The voltage gain from the VRS input to the Tip output is 40V/V. The resistor ratio provides a gain of eight and the current mirror provides a gain of five. The voltage gain from the VRS input to the Ring output is -40V/V. The equations for the Tip and Ring outputs during ringing are given in Equations 3 and 4.

$$V_T = \frac{V_{BH}}{2} + (40 \times VRS) \quad \text{(EQ. 3)}$$

$$V_R = \frac{V_{BH}}{2} - (40 \times VRS) \quad \text{(EQ. 4)}$$

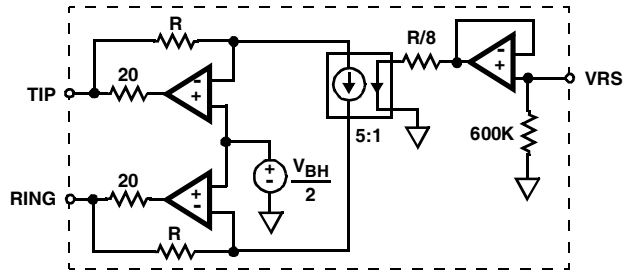


FIGURE 5. LINEAR RINGING MODEL

When the input signal at VRS is zero, the Tip and Ring amplifier outputs are centered at half battery. The device provides auto centering for easy implementation of sinusoidal ringing waveforms. Both AC and DC control of the Tip and Ring outputs are available during ringing. This feature allows for DC offsets as part of the ringing waveform.

Ringing Input

The ringing input, V_{RS}, is a high impedance input. The high impedance allows the use of low value capacitors for AC coupling the ring signal. The V_{RS} input is enabled only during the ringing mode, therefore a free running oscillator may be connected to VRS at all times.

When operating from a battery of -100V, each amplifier, Tip and Ring, will swing a maximum of $95V_{P-P}$. Hence, the maximum signal swing at VRS to achieve full scale ringing is approximately $2.4V_{P-P}$. The low signal levels are compatible with the output voltage range of the CODEC. The digital nature of the CODEC ideally suits it for the function of programmable ringing generator.

Ringing the Phone

If previous test was either Test #1 or #2, skip to Step 2.

1. Configure hardware and software as described in section titled *Getting Started*.
2. Configure the HC55185 to be in the Ringing mode using the SLIC Operation Mode Control Switches S1_A/B through S6_A/B. Reference Table 7 for switch positions. *Keep BSEL LOW at this point.*
3. Press '1' to write to the CODEC resisters. Then decimal 4 followed by Hex 00. This will power up the ring tone generator.
4. Press '1' to write to the CODEC resisters. Then decimal 5 followed by Hex 06. This will set the ring tone generator to 20Hz.
5. Connect a phone to Channel A/B using the RJ11 jack on the board.
6. Toggle the BSEL switch S6_A/B from low battery to high battery and the phone will start to ring.

7. When the test is completed, set the BSEL switch S6_A/B low. You also need to power down the ring generator. Press '1' to write to the CODEC resisters. Then decimal 4 followed by Hex 04.This will prevent the tone from interfering with subsequent tests.
8. Configure the HC55185 to be in the forward active mode using the SLIC operation mode control switches S1_A/B through S6_A/B. Reference Table 7 for switch positions.

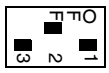
Test # 4 Emulation of Phone Conversation

This test will demonstrate an end to end phone conversation between Channel A and Channel B. Setting up an end to end phone conversation is accomplished configuring the AK2306/2306LV for the swap mode and connecting the DX and DR terminals together (Figure 1).

If previous test was either Test #1, #2 or #3, skip to step 3.

1. Configure hardware and software as described in section titled *Getting Started*.
2. Configure both HC55185s in the forward active mode using the SLIC operation mode control switches S1_A/B through S6_A/B. Reference Table 7 for switch positions.
3. Configure DIP switch SW5 for the swap mode by toggling 2 in the off position as shown.

SW5



4. Connect the DX terminal (connected to port 20 of PCM4) to the DR terminal (connected to port 21 of PCM4).
5. Verify that the Ring tone generator is turned off. Press '1' to write to the CODEC resisters. Then decimal 4 followed by Hex 04.

Verification of Phone Conversation

1. Verify phone connection between both channels by picking up the receivers and talking.
2. Return dip switch SW5 to initial position (Table 4).
3. Reconnect DX and RX to PCM4.

Test # 5 Gain Verification

This test will verify the gains through the AK2306/2306LV and the HC55185 are operating properly. The test will show, with the receive and transmit gains programmed to 0dB, the Digital to Analog gain across both the CODEC and the SLIC is equal to -1.0 (0dB), and the Analog to Digital gain across both the SLIC and the CODEC is also equal to 1.0 (0dB). Both D/A and A/D gains will be verified by performing a Digital to Digital gain using the PCM4.

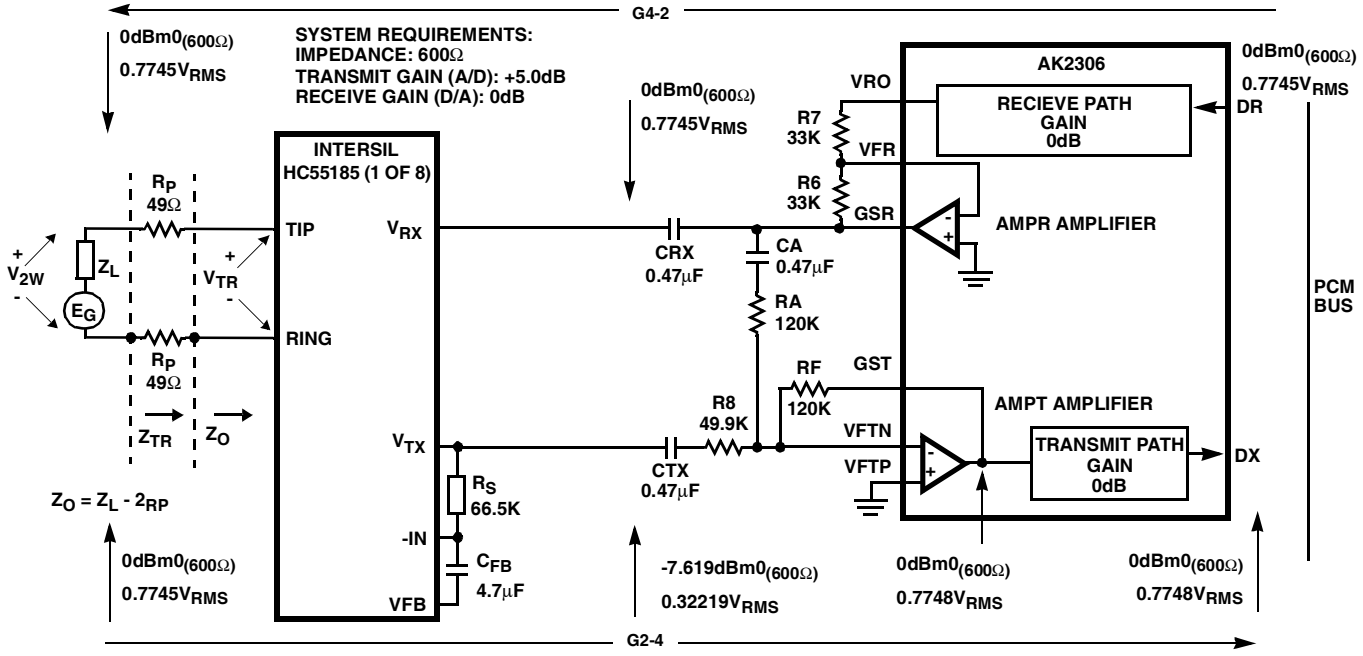


FIGURE 6. REFERENCE DESIGN OF THE HC55185 AND THE AK2306 WITH A 600Ω LOAD IMPEDANCE

Figure 6 shows the reference design of the HC55185 and the AK2306 with a 600Ω load impedance. Reference *Application Note AN9991* for a detailed engineering analysis of the reference design.

Total System Gain (D/D)

If previous test was Test #1, #2, #3, or #4, skip to Step 3.

1. Configure hardware and software as described in section titled *Getting Started*.
2. Configure the HC55185 to be in the forward active mode using the SLIC operation mode control switches S1_A/B through S6_A/B. Reference Table 7 for switch positions.
3. Terminate tip and ring with a 600Ω load.
4. Set the general parameters of the PCM4 as shown in Table 12. Set the PCM4 Interface (port 14) to TX/RX. Set the RX-Impedance/Ω (port 13) to 600Ω. Set the TX-Impedance/Ω (port 15) to 600Ω.
5. Set the PCM4 transmit and receive channels to channel 0. This will enable the PCM4 to receive and transmit data to the Channel A PCM time slot. To test channel B, set the PCM4 to channel 1.
6. Configure the PCM4 for the MODE A 11 test. Set PCM4 to D-D, SWP/S (single sweep). Press start to test network.

Verification

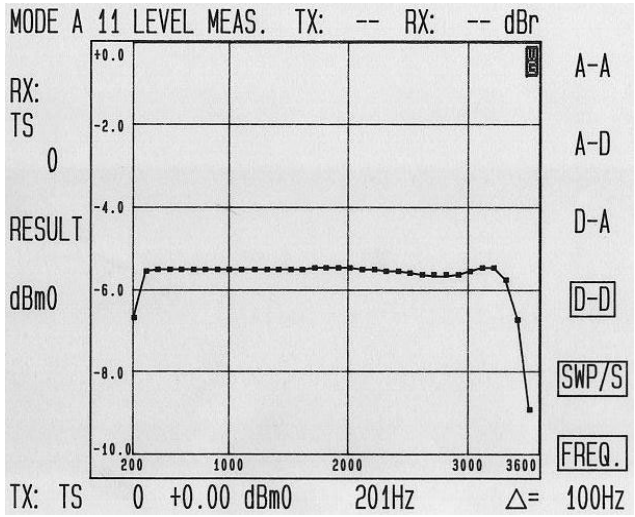
Compare results to the Graph 1.

TABLE 12. PCM4 GENERAL PARAMETERS SETTINGS

General Parameter	Setting	Parm
(1) Digital Configuration:		
General configuration	TX/RX 2M/2Mbps selected	11
Digital Loop (A - A)	OPEN/AUX.SIGN.	23
(2) Frame Selection:		
TX frame type	All 32 TS teleph	14
RX frame type	All 32 TS teleph	24
CRC-4 Multiframe	Off	31
(3) Digital TX Interface:		
Line Code	NRZ	13
Output Impedance	75Ω unbalanced	22
Clock	Int. 2048kHz	31
(4) Digital RX I nterface:		
Line Code	NRZ	13
Input Impedance	> 3kΩ	22
(5) Digital Words in TX Frame:	Reset to standard values	11
Frame Words	ALL CHAN.	22
Send Signal		
(6) TX Error Insertion	Off	11
(7) PCM Coding:		
TX Encoding Law	Must match address 101 Table 10. Default setting is μ-law	11
RX Encoding Law	Must match encoding law	21
(8) Scanner Parameter:		
VF-Input no.	1	11
VF-Output no.	1	21

TABLE 12. PCM4 GENERAL PARAMETERS SETTINGS (Continued)

General Parameter	Setting	Parm
(9) Special Parameter:		
Level Display	dBm0	11
Two wire Term.	Infinite	13
Digital Channel no.	Time Slot	16
	Mark and cont.	22
Tolerance mask set 2		23
	Mark and cont.	27
Clock display	OFF	33
OFF		35



GRAPH 1. TOTAL SYSTEM GAIN (D/D)

Test # 6 Variable Gain / Frequency

This test will configure the HC55185 in the loopback mode and evaluate the AK2306/2306LV and the HC55185's AC performance across frequency.

Discussion

Most of the SLICs in the HC55185 family feature two-wire loopback testing. During the two-wire loopback test, a 600Ω internal resistor is switched across the tip and ring terminals of the SLIC. This allows the $\overline{DET}$ function and the four-wire to four-wire AC transmission, right up to the subscriber loop, to be tested.

Variable Gain / Frequency (D/A) Test #6a

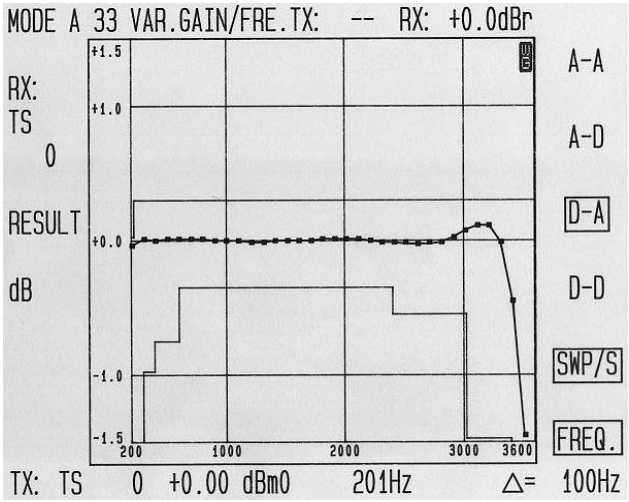
If previous test was Test #1, #2, #3, or #4, skip to Step 3. If previous test was Test # 5 skip to Step 5.

1. Configure hardware and software as described in section titled *Getting Started*.
2. Configure the HC55185 to be in the forward loop back mode using the SLIC operation mode control switches S1_A/B through S6_A/B. Reference Table 7 for switch positions.

3. Set the general parameters of the PCM4 as shown in Table 12. Set the PCM4 Interface (port 14) to TX/RX. Set the RX-Impedance/Ω (port 13) to 600Ω. Set the TX-Impedance/Ω (port 15) to 600Ω.
4. Set the PCM4 transmit and receive channels to channel 0. This will enable the PCM4 to receive and transmit data to the Channel A PCM time slot. To test channel B, set the PCM4 to channel 1.
5. Remove the 600Ω load from across tip and ring.
6. Configure the PCM4 for the MODE A 33 test. Set PCM4 to D-A, SWP/S (single sweep). Press start to test network.

Verification

Compare results to the Graph 2.



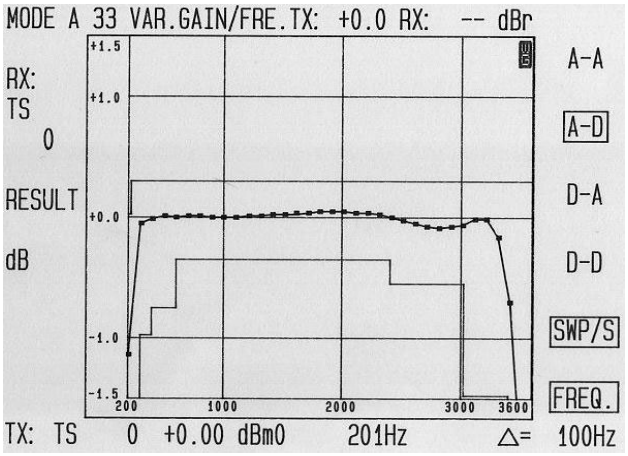
GRAPH 2. (D/A) VARIABLE GAIN vs. FREQUENCY

Variable Gain / Frequency (A/D) Test #6b

1. Configure the PCM4 for the MODE A 33 test. Set PCM4 to A-D, SWP/S (single sweep). Press start to test network.

Verification

Compare results to the Graph 3.



GRAPH 3. (A/D) VARIABLE GAIN vs. FREQUENCY

Test # 7 Total Distortion

This test will configure the HC55185 in the loopback mode and evaluate the AK2306/2306LV and the HC55185's total distortion.

Total Distortion (D/A) Test #7

If previous test was Test # 1, #2, #3, or #4, skip to Step 3.
If previous test was Test # 5 skip to Step 4.
If previous test was Test #76a/b skip to Step 6.

1. Configure hardware and software as described in section titled *Getting Started*
2. Set the general parameters of the PCM4 as shown in Table 12. Set the PCM4 Interface (port 14) to TX/RX. Set the RX-Impedance/Ω (port 13) to 600Ω. Set the TX-Impedance/Ω (port 15) to 600Ω.
3. Set the PCM4 transmit and receive channels to channel 0. This will enable the PCM4 to receive and transmit data to the Channel A PCM time slot. To test channel B, set the PCM4 to channel 1.
4. Configure the HC55185 to be in the forward loop back mode using the SLIC operation mode control switches S1_A/B through S6_A/B. Reference Table 7 for switch positions.
5. Remove the 600Ω load from across tip and ring.
6. Configure the PCM4 for the MODE A 55 test. Set PCM4 to D-A, SWP/S (single sweep). Press start to test network.

Verification

Compare results to the Graph 4.

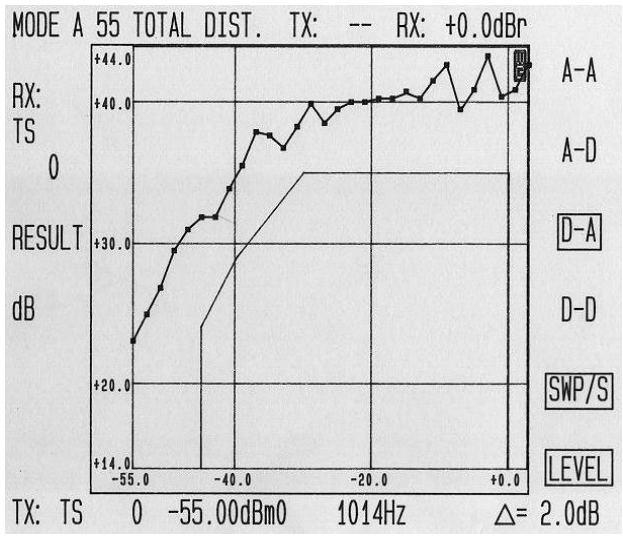


FIGURE 4. (D/A) TOTAL DISTORTION

Board Schematic

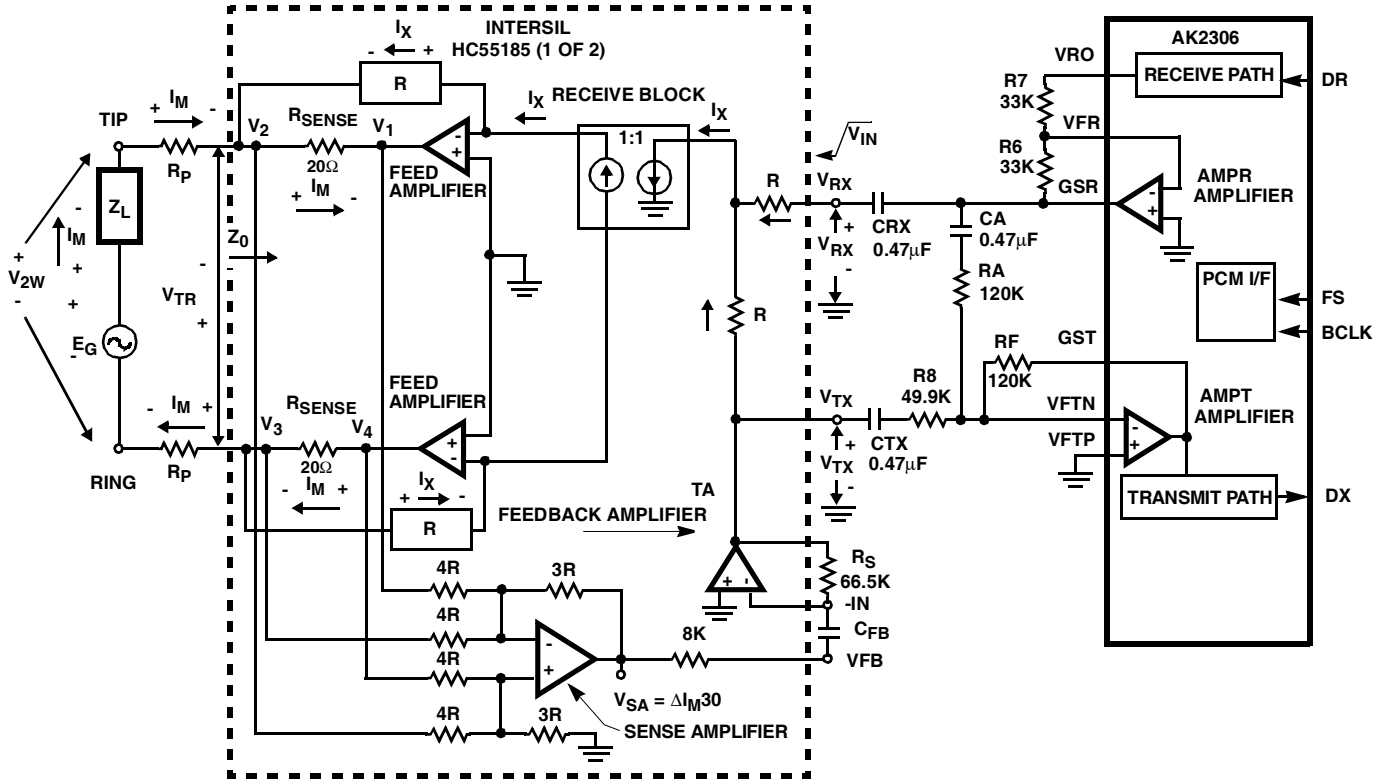


FIGURE 7. HC55185 SIMPLIFIED AC TRANSMISSION CIRCUIT AND AK2306

Board Schematic (continued)

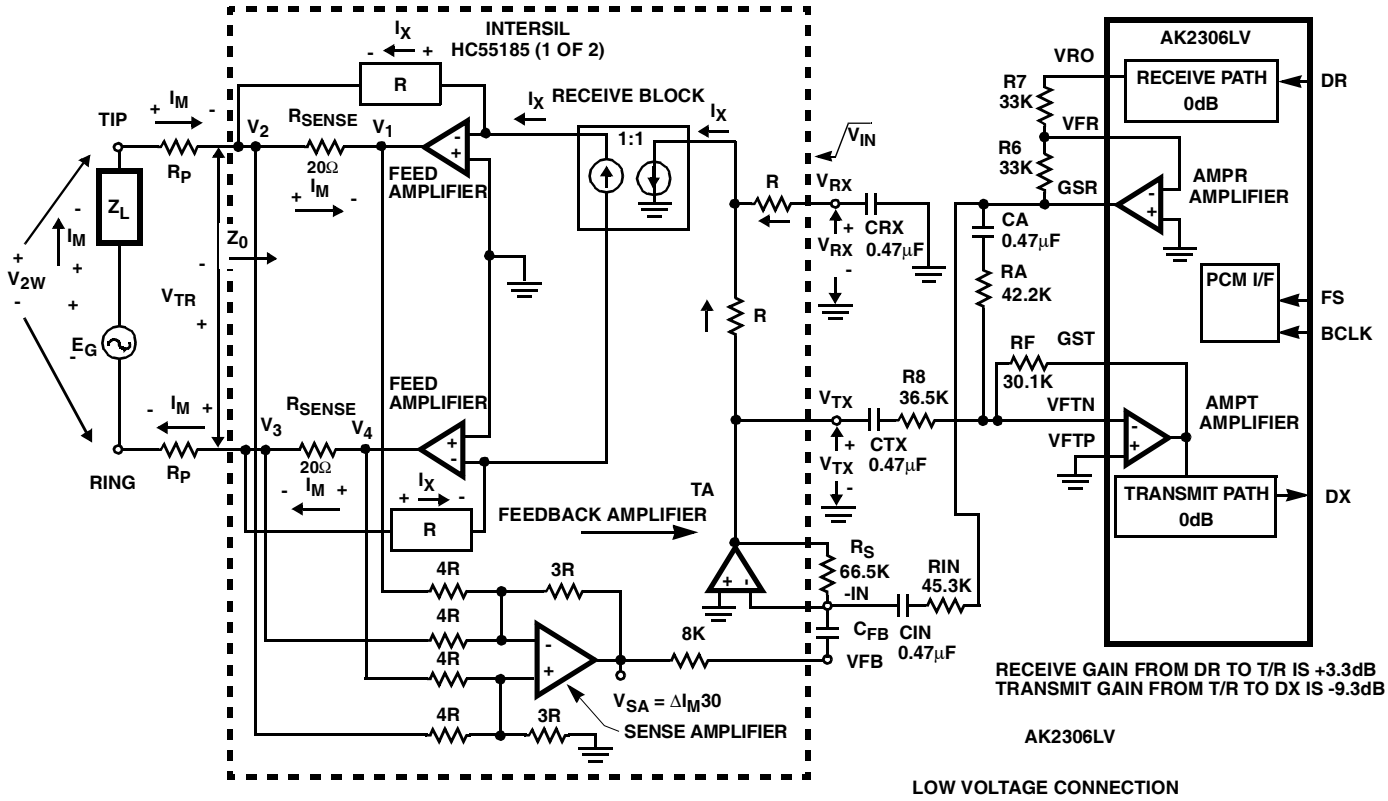


FIGURE 8. HC55185 DEMO DAUGHTER BOARD SCHEMATIC

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
7585 Irvine Center Drive
Suite 100
Irvine, CA 92618
TEL: (949) 341-7000
FAX: (949) 341-7123

Intersil Corporation
2401 Palm Bay Rd.
Palm Bay, FL 32905
TEL: (321) 724-7000
FAX: (321) 724-7946

EUROPE
Intersil Europe Sarl
Ave. William Graisse, 3
1006 Lausanne
Switzerland
TEL: +41 21 6140560
FAX: +41 21 6140579

ASIA
Intersil Corporation
Unit 1804 18/F Guangdong Water Building
83 Austin Road
TST, Kowloon Hong Kong
TEL: +852 2723 6339
FAX: +852 2730 1433