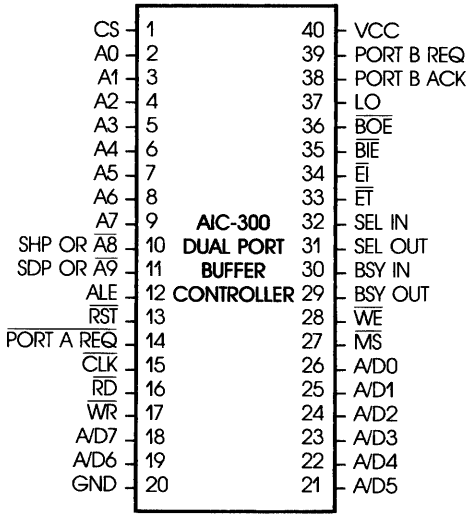
Dual Port Buffer Controller

PRELIMINARY

- 16-bit Buffer Addressing
- DMA Handshake Logic
- Overrun Control
- Dual Port Circular FIFO Buffer Control
- Buffer Sizes from 256 to 64K Locations
- Port Priority Resolver
- 2-wire Arbitration Logic
- Optimized for Use with AIC-100 Winchester Disk Controller Chip
- Single +5V Power



DESCRIPTION

The Adaptec AIC-300 Dual Port Buffer Controller is specifically designed to simplify the buffering and increase throughput of block-oriented high-performance peripheral controllers. Its primary functions are to: allow low cost static RAM to be utilized as a dual port circular FIFO, supervise data transfers to the buffer, reduce the possibility of host overruns of the peripheral, and allow for high speed DMA transfers. The device contains logic for resolving peripheral/host requests by giving priority to the peripheral and placing effectively a hold request to the host. The AIC-300 also implements a two wire arbitration circuit and provides DMA handshaking. This device represents a significant savings in component count for high performance, block oriented device controllers and provides performance capabilities that previously had not been cost effective for microcomputers.

The AIC-300 is intended for use in intelligent controllers utilizing a low cost microprocessor for supervision of the controller function. The device is software configurable via a multiplexed microprocessor I/O bus as provided by the Intel 8085 family of microprocessors and is adaptable to other microprocessor I/O techniques. The AIC-300 is optimized for use with the Adaptec AIC-100 Winchester disk controller chip in the design of a low-cost high-performance disk controller.

AIC-300 PIN DESCRIPTION

SYMBOL	PIN	TYPE	NAME AND FUNCTION
CS	1	IN	CHIP SELECT: Asserting CS allows the microprocessor to access the registers of the AIC-300.
A0-A7	2-9	OUT	BUFFER ADDRESS LINES: Bits 0-7 for addressing low-order address of buffer in applications with less than 10-bits of addressing. In applications with more than 10-bit addressing these lines are multiplexed low and high order addresses.
SHP Or $\overline{A8}$	10	OUT	STROBE HOST POINTER: Buffer address bit 8 in applications with buffer size of 10 or less bit addressing. This is the clocking signal for loading high-order address bits into an external host address register in applcations using more than 10-bit addressing.
SDP Or $\overline{A9}$	11	OUT	STROBE DEVICE POINTER: Buffer address bit 9 in application with buffer size of 10 or less bit addressing. This is the clocking signal for loading high-order address bits into external disk address register in applications using more than 10-bit addressing.
ALE	12	IN	ADDRESS LATCH ENABLE: This control signal latches the address on the A/D0-A/D7 lines and identifies the bits as register address.
$\overline{RST}$	13	IN	RESET: This line, when asserted, resets all registers in the AIC-300 and sets bit 0 of Register 59.
$\overline{Port\ A\ Req}$	14	IN	PORT A REQUEST: Requests a Port A data transfer into or out of the buffer.
$\overline{CLK}$	15	IN	CLOCK: This is the primary clock for the part. Its period should be greater than RAM access time + 250 ns.
$\overline{RD}$	16	IN	READ: $\overline{RD}$ and CS active causes the data on the A/D lines to be read from the specified register.
$\overline{WR}$	17	IN	WRITE: $\overline{WR}$ and CS active causes the data on the A/D lines to be written into the specified register.
A/D0-7	18-19 21-26	I/O	MULTIPLEXED ADDRESS/DATA: These are 3-state Address/Data lines which interface with a multiplexed microprocessor Address/Data bus.
GND	20		GROUND.
$\overline{MS}$	27	OUT	MEMORY SELECT: Chip select for the buffer memory RAM chips.
$\overline{WE}$	28	OUT	WRITE ENABLE: $\overline{WE}$ enables data to be written into the RAM buffer and deasserting WE enables data to be read from the RAM buffer.
BSY OUT	29	OUT	BUSY OUT: Either set directly by the microprocessor or in an arbitration request mode the Busy Out will be activated when Busy In and Select In are inactive. The arbitration mode assures an arbitration phase.
BSY IN	30	IN	BUSY IN: Active when other devices are actively accessing the bus.
SEL OUT	31	OUT	SELECT OUT: Set by the microprocessor as bit 6, Register 52 (Channel Control).
SEL IN	32	IN	SELECT IN: Active indicates a bus select status. Sel In will reset the arbitration latch.
$\overline{ET}$	33	OUT	ENABLE TARGET: A microprocessor settable signal to identify slave status.
$\overline{EI}$	34	OUT	ENABLE INITIATOR: A microprocessor settable signal to identify master status.
$\overline{BIE}$	35	OUT	BUS IN ENABLE: Used to clock data into external latches from the bus for writing into the buffer.

AIC-300 PIN DESCRIPTION (Continued)

SYMBOL	PIN	TYPE	NAME AND FUNCTION
$\overline{BOE}$	36	OUT	BUS OUT ENABLE: Used to clock data out of external latches for transfer onto the bus. Asserted when arbitration latch is set.
LO	37	OUT	LATCH OUT: Used to gate data into external latches after reading from buffer via Port B.
PORT B ACK	38	IN	PORT B ACKNOWLEDGE: Used to acknowledge data has been received or sent from the buffer via Port B (DMA Handshake).
PORT B REQ	39	OUT	PORT B REQUEST: The request for a data transfer via Port B (DMA Handshake).
V_{CC}	40		+5 Volt Supply.

FUNCTIONAL DESCRIPTION

The AIC-300 is divided into four basic sub-functions:

- Buffer Control
- Priority Resolver
- DMA Control
- Arbitration

The AIC-300 when used in a CPU environment will work well with the DMA control devices available to provide host processor memory addressing or it may be used in an external I/O bus system such as SCSI.

BUFFER CONTROL: The buffer control function provides read and write address registers as well as Memory Select (MS) and Read/Write (WE) signaling. These signals are used to read or write data from the RAM buffer.

PRIORITY RESOLVER: The priority resolver allows the typically synchronous peripheral to have priority over the host requests. This is fairly crucial in disk controller applications, where in a 10 MB/sec system, a data byte has to be transferred exactly once every 800 nsecs.

DMA CONTROL: The DMA control generates a request to the host (Port B Req) gates into or out of the buffer the appropriate data, and waits for a correctly timed acknowledge (Port B ACK).

ARBITRATION: The arbitration logic of the AIC-300 provides for a two-wire arbitration scheme where either Select In or Busy In indicate a bus busy state. The device allows for stacking a request for arbitration when the bus is in the bus busy state. The arbitration logic will request the bus for arbitration when both Select In and Busy In are inactive for a period of 100 ns.

FUNCTIONAL OPERATION

The AIC-300 is capable of handling buffer sizes from 256 bytes to 64K bytes. The chip provides up to 16 buffer address signals necessary for this, along with a Memory Select (MS) signal and a Read/Write (WE) signal. All of the buffer addressing is done by eight lines (A0-A7) and two dual purpose lines (A8/SHP and A9/SDP).

In the 10 bit or less addressing mode, the two special lines supply the A8 and A9 address lines. An example is shown in Figure 1.

In the 16 bit addressing mode, the higher order lines (A8-A15) and the lower order lines (A0-A7) are multiplexed coming out of the chip, on pins A0-A7. Two external TRI-STATE registers are required for the high order address lines A8-A15. These registers hold a copy of the internal counters, Registers 5B and 5D. These registers are updated on the CLK cycle following an increment of the internal counters (5B or 5D), if a Port A cycle is not required or on the CLK cycle following a write of 5B or 5D by the microprocessor. A word of caution: The microprocessor update of these external registers is not prioritized and therefore should only be done when Port A and B operations have quiesced. The AIC-300 updates the external registers by emitting the appropriate A8 through A15 on address lines A0 through A7 and then pulses either SHP or SDP appropriately. In normal operation these updates will occur after every 256 bytes transferred by either port.

Note that an "AND" gate of SHP and CLK is required for proper operation of microprocessor updates of the host pointer. When slow microprocessors are used, double pulsing of SHP and SDP will occur because of the internal syncronization circuit; however, the address for both pulses is valid.

The CLK cycle determines the access time requirement for the buffer RAMs, along with the address valid time for the AIC-300. For a 400 ns CLK period 150 ns access-time RAM is needed for proper operation.

For proper interleaved Port A-Port B operation, the maximum rate at which Port A requests should occur is once for every two CLK cycles. This will allow Port B REQ/ACK cycles to occur at one-half the CLK rate. Note that Port A cycles always have priority over Port B and high order address register updates. With a very fast DMA interface and a CLK period of 333 ns and 85 ns access buffer rams a 1.5 Mbyte transfer rate is possible in this mode.

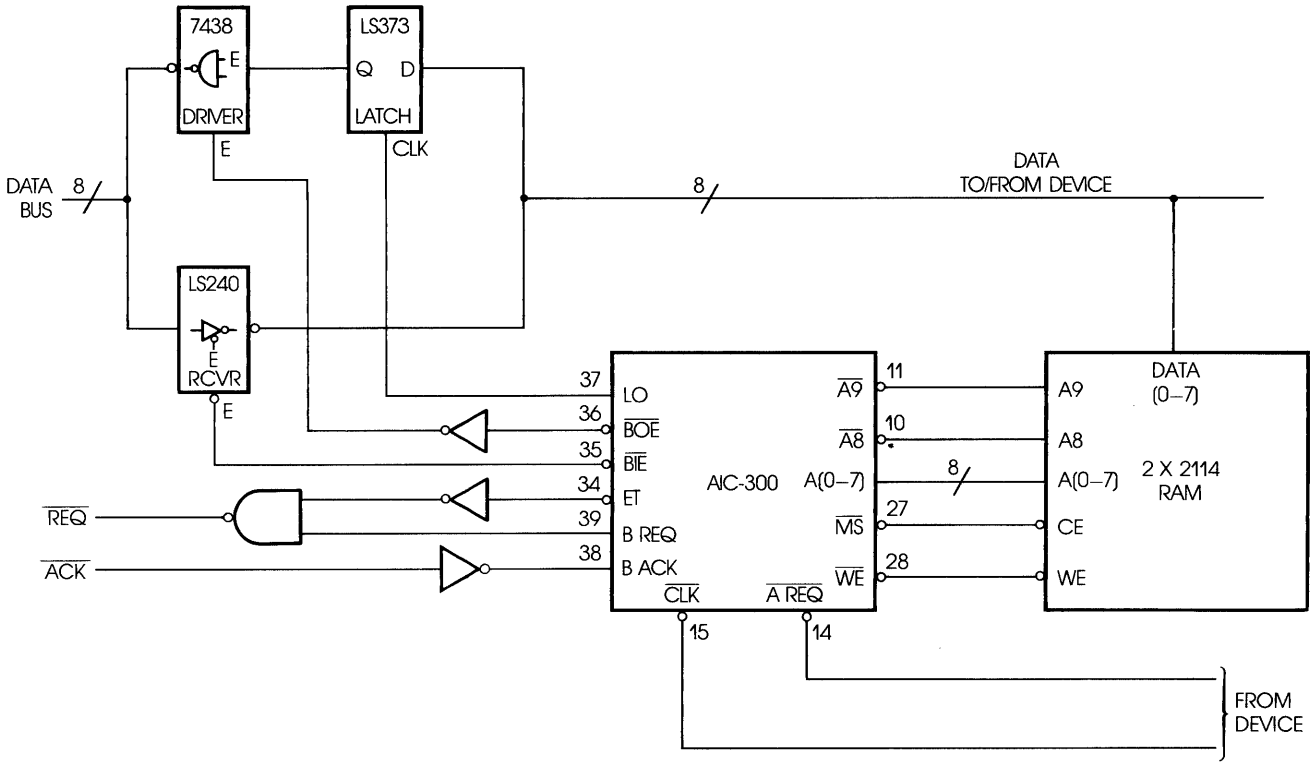


FIGURE 1. 10-BIT ADDRESSING APPLICATION EXAMPLE

An example of the 16-bit addressing mode is shown in Figure 2. Figure 3 shows an internal block diagram of the AIC-300 buffer addressing section.

The AIC-300 buffer controller chip is viewed as 10 internal registers and 3 external registers by the support processor. The table shows each register and their function. A more detailed graphical breakdown of the registers follows.

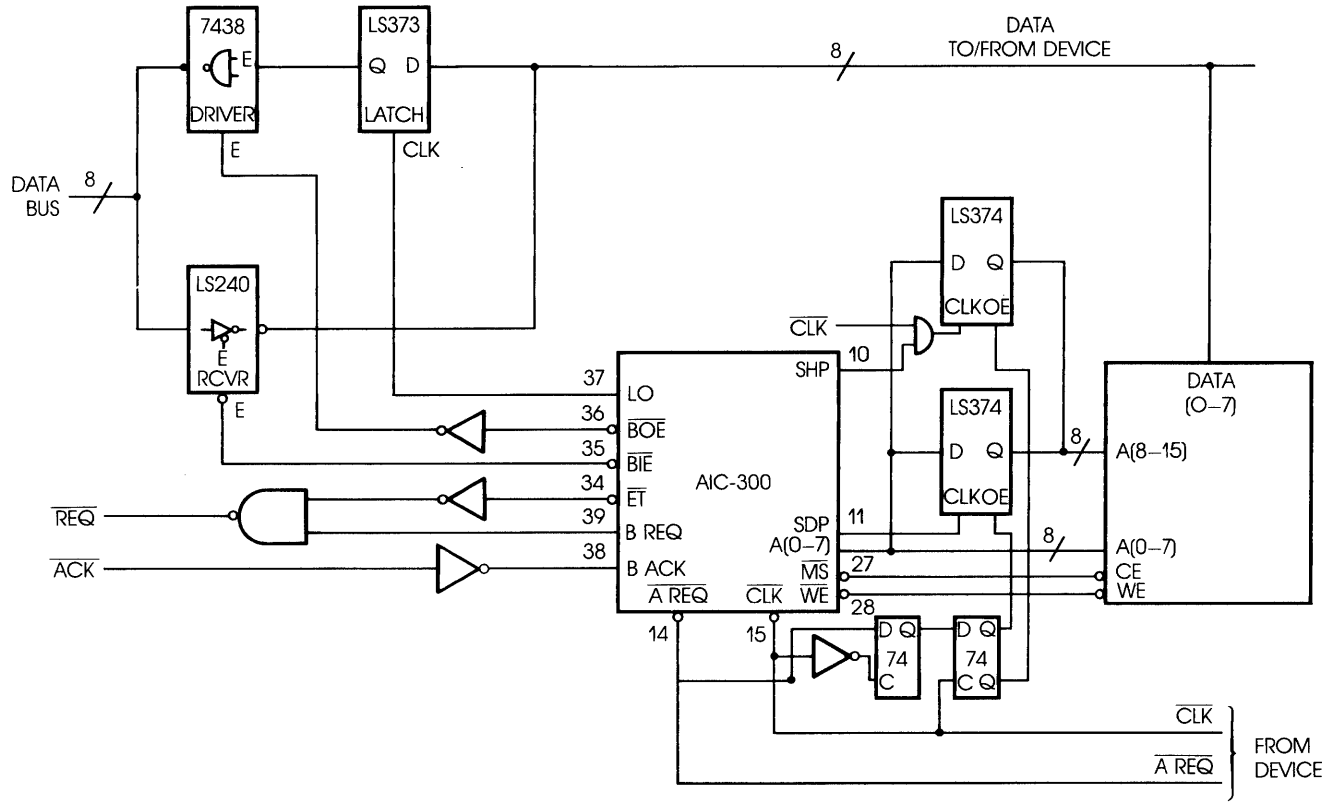


FIGURE 2. 16-BIT ADDRESSING APPLICATION EXAMPLE

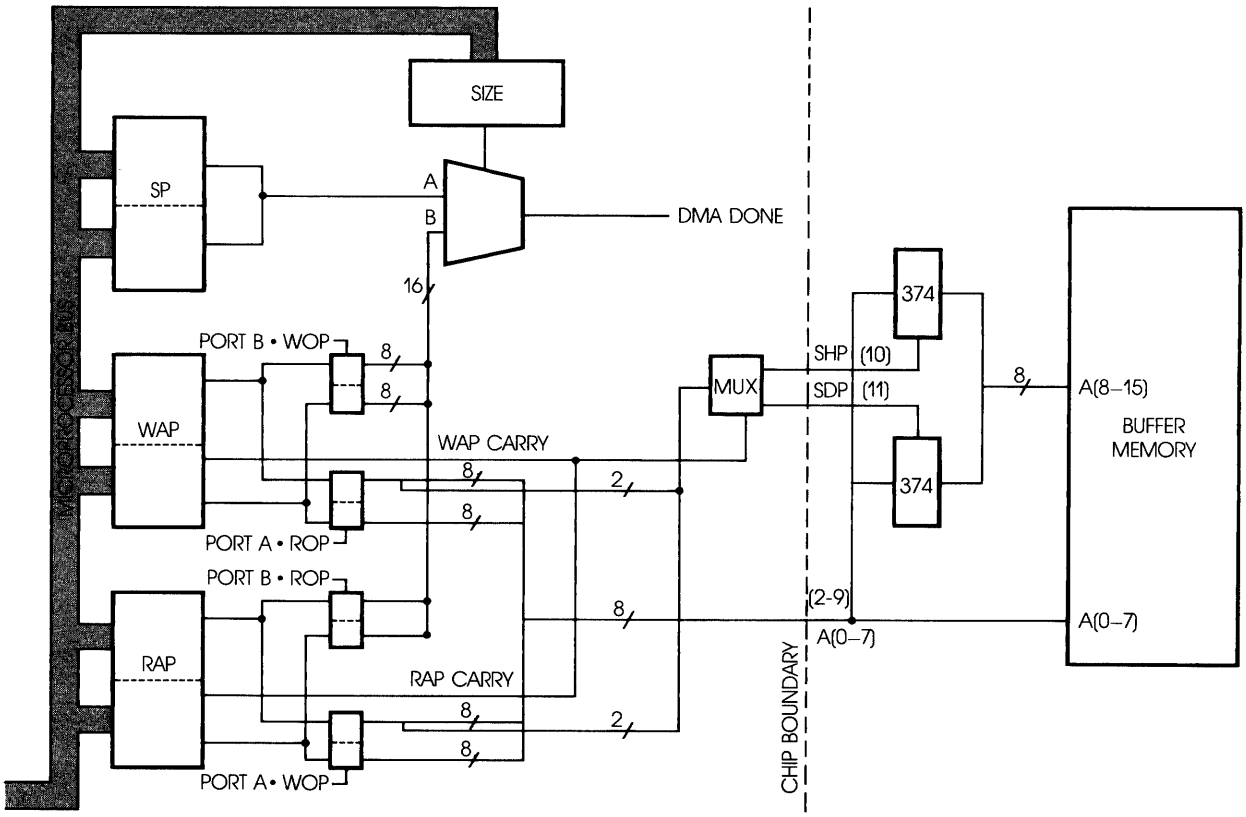


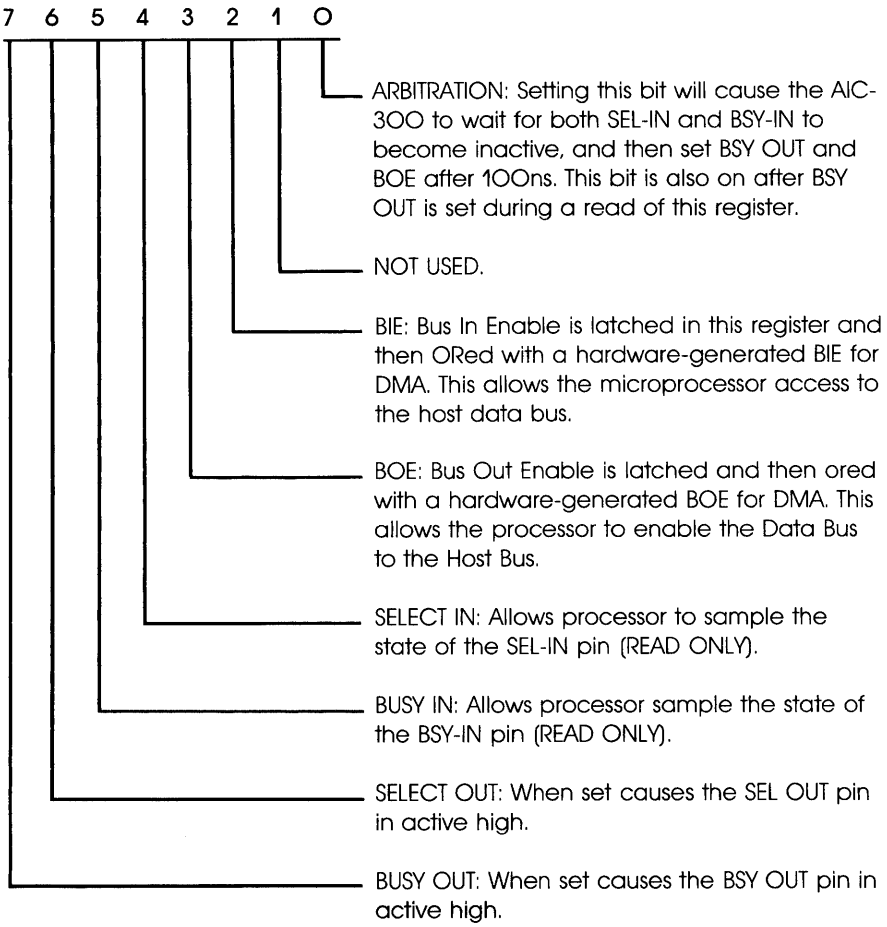
FIGURE 3. AIC-300 BUFFER ADDRESSING BLOCK DIAGRAM

AIC-3OO REGISTER TABLE

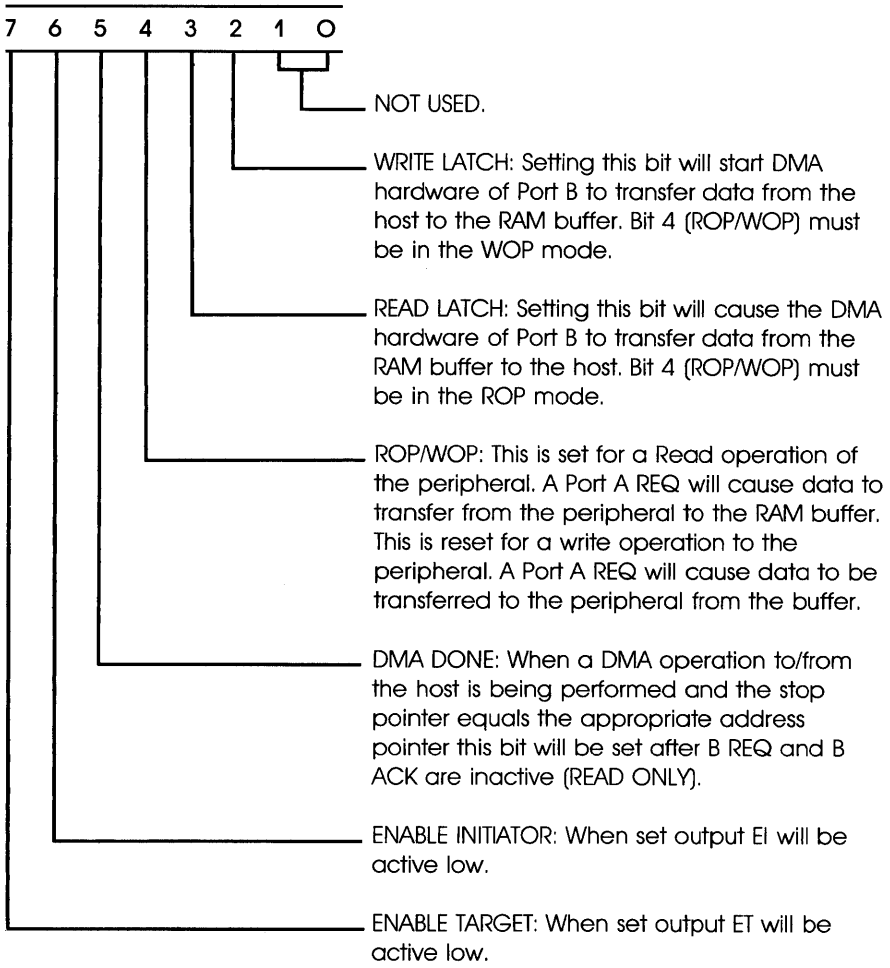
INTERNAL REGISTERS	DESCRIPTION/FUNCTION
Register 52	Control register for the host bus, for arbitration control.
Register 53	DMA control register, starts DMA operations, and defines data direction for bus and device data transfers.
Register 54	Buffer size register defines the size of the buffer to determine the roll over point, creating a circular buffer.
Register 59	Only bit O is used. When bit O is set, all registers in AIC-3OO will be reset. Any write to this Register will reset WAP, RAP, and SP.
Register 5A & 5B	16 bit Read Address Pointer, used to address the buffer on read cycles.
Register 5C & 5D	16 bit Write Address Pointer, used to address the buffer on write cycles.
Register 5E & 5F	16 bit Stop Pointer used to prevent the host from overrunning the peripheral device. The Stop Pointer is compared with the Host Pointer by a comparator whose high-order bits are enabled by the contents of Register 54. When the two pointers are equal, DMA REQ/ACK cycles are halted and the done bit is set. If a new high-order stop point is set, DMA REQ/ACK cycles will begin again if the appropriate READ latch or WRITE latch is still on.
EXTERNAL REGISTERS	**DESCRIPTION/FUNCTION**
Register 5O	Register 5O decode is used to allow the support processor access to the host data bus. Register 5O decode and WR asserts LO.
Register 51	Register 51 decode is used to allow the support processor to access the high order byte of the data bus in 16 bit applications. RD and WR operates the same as Register 5O.
Register 7O	Register 7O decode is used to allow the support processor to access the buffer. A read will cause MS to be active. A write will cause MS and WE to be active.

Internal Register Description

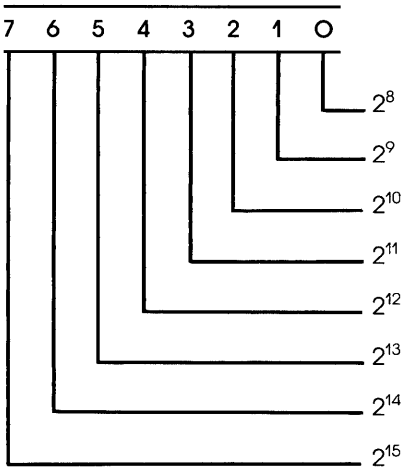
52 HOST INTERFACE CONTROL
(READ/WRITE)



53 DMA CONTROL (READ/WRITE)

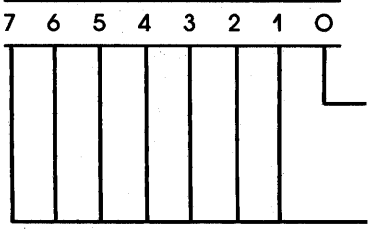


54 BUFFER SIZE (WRITE)



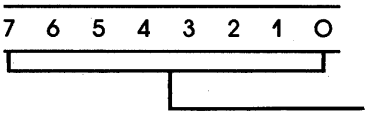
(Example: Set Register 54 to O3 for a 1 Kbyte buffer.)

59 RESET CONTROL (WRITE)

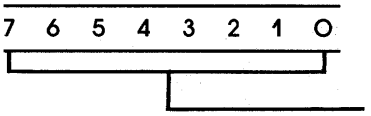


NOTE: Any write to this register will reset WAP, RAP and SP. If external high order address register are used, they will not be reset.

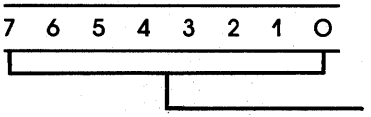
5A RAP (O-7) (READ/WRITE)



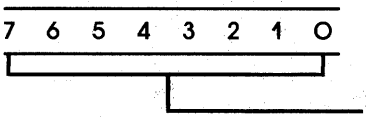
5B RAP (8-15) (READ/WRITE)



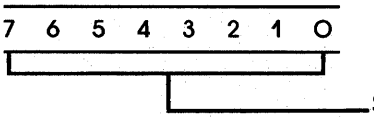
5C WAP (O-7) (READ/WRITE)



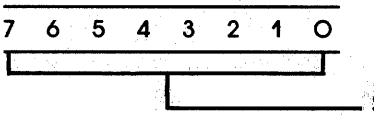
5D WAP (8-15) (READ/WRITE)



5E STOP (O-7) (READ/WRITE)



5F STOP (8-15) (READ/WRITE)



Data Transfer Description

In the AIC-300 dual port buffer controller, data transfer can take place in two possible ways: (1) synchronously with the peripheral (Port A transfer) or (2) asynchronously with the host (Port B transfer).

In the case of Port A transfers, a byte is transferred after every time pin 14 (Port A Req) is asserted. This line is sampled on the trailing edge of the signal on pin 15 (CLK), and the data transfer takes place on the next cycle after Port A Req is asserted.

The direction of the transfer is determined by the value of bit 4 in Register 53. If it is set, then a Read Operation is performed from the peripheral. The contents of the WAP Registers (5C and 5D) are used to select a buffer address, and Memory Select (MS) and Write Enable (WE) are used to write the information into the buffer.

If Register 53, bit 4, is reset, a write operation to the peripheral is performed. The RAP Registers (5A and 5B) are used to generate a buffer address, and the data is read when Memory Select (MS) is active. The ideal time for the peripheral to sample the data from the buffer RAM in this case is at the falling edge of CLK following the Port A REQ.

In the case of Port B transfers, data is transferred under the control of the AIC-300 chip. Again the direction of the transfer is controlled by the contents of the ROP/WOP bit (Reg 53, bit 4), and either Write Latch or Read Latch (Reg 53, bit 1 or bit 2).

If the ROP/WOP bit is set, and Read Latch is on then data is transferred from the buffer to host. The contents of the RAP Registers (5A and 5B) are used to generate the addresses. The data is latched into an external latch using the output signal on pin 37 (LO). Bus Out Enable (BOE) is also asserted and the data is made available to the host. A Port B request is sent to the host, and the data is placed on the bus. After an acknowledge is received, BOE is deasserted.

If bit 4 in Register 53 is reset, and Write Latch is on then data is transferred from the host bus to the buffer. The contents of the WAP Registers (5C and 5D) are used to generate the buffer address. BIE is asserted to enable the external receiver.

A point to note here: During a host data transfer, the top buffer address that can be accessed is controlled by the stop pointer (Registers 5E and 5F).

OP COMMAND SEQUENCES

A detailed description of the data transfers in two fundamental AIC-300 operations follows:

Read — Single Block and Multiple Block
Write — Single Block and Multiple Block

Initialization

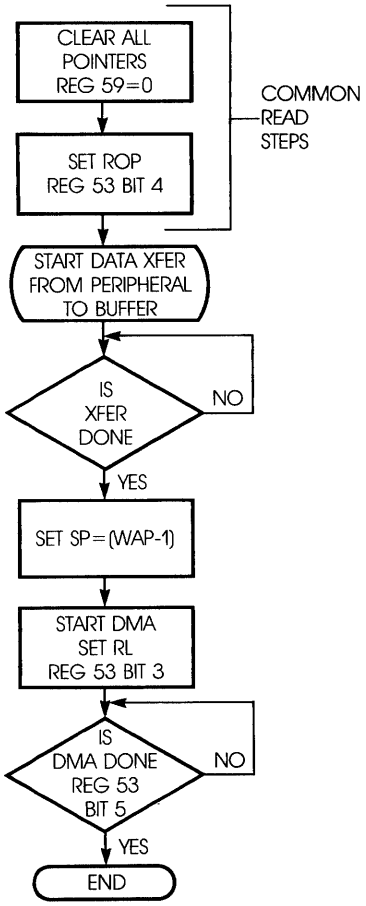
Initialization is done after power on reset. It is not required thereafter:

1. Reset chip by strobing pin 13 and set Register 59 to 00 (clear Reset).
2. Set maximum size of RAM buffer by loading Register 54 with buffer size.

Single Block Read

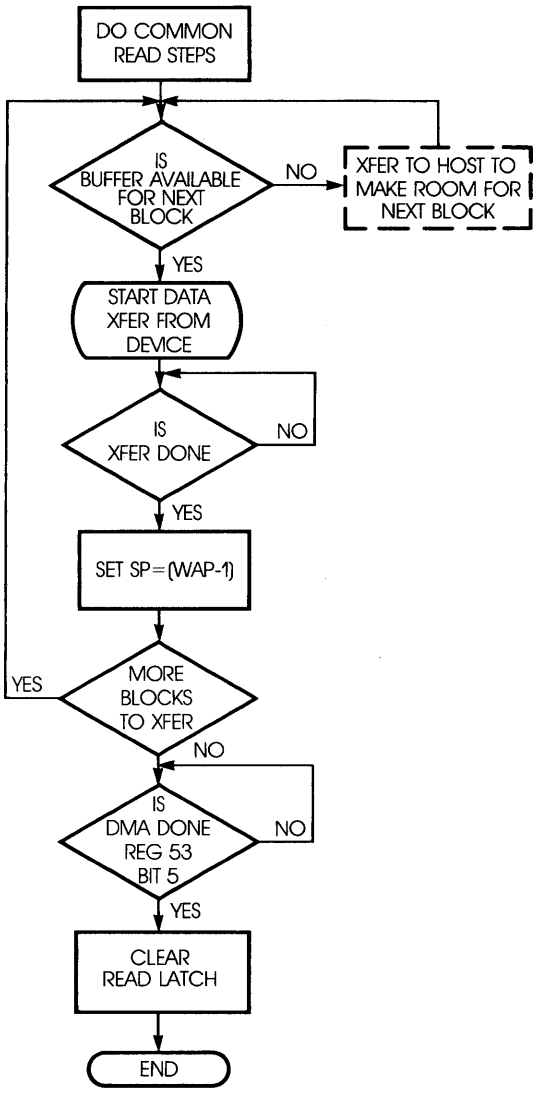
1. Clear all pointers (set Register 59 to O).*
2. Set-up for read operation (set Register 53, bit 4).
3. Transfer data to buffer (WAP will increment on each transfer).
4. At completion of transfer from device, set SP to (WAP-1) and set read latch for DMA read operation (Register 53, bit 3). RAP will increment for each Request Acknowledge cycle.
5. Monitor DMA Done bit (Register 53, bit 5) to determine when the DMA transfer is complete (RAP equals SP).

*In the 16-bit addressing mode, after setting Register 59 to O, also set RAPH (Register 5B) and WAPH (Register 5D) to O.



Multiple Block Read

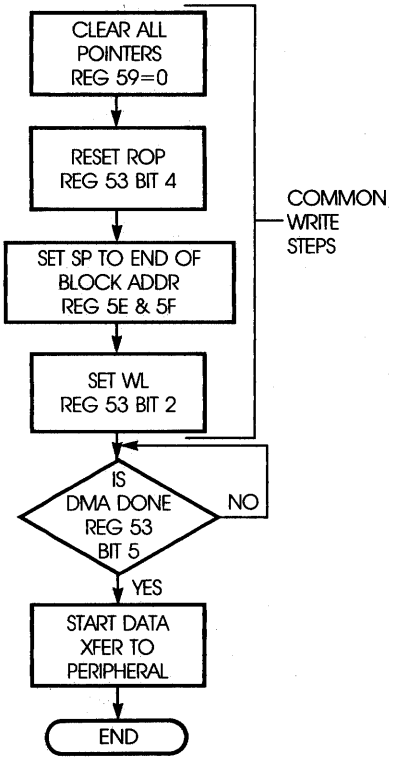
1. Do the same first four operations as single block read.
2. Read RAP to ensure that next block may be transferred from the device without overrunning the RAP.
3. Begin transfer of next block to buffer (WAP will increment on each transfer).
4. At end of transfer, set SP to new (WAP-1) address.
5. If DMA Done occurred, a restart of the DMA transfer will occur when the new SP address is set.
6. Return to step two if more blocks are to be transferred.
7. Wait for DMA Done and clear Read Latch.



Single Block Write

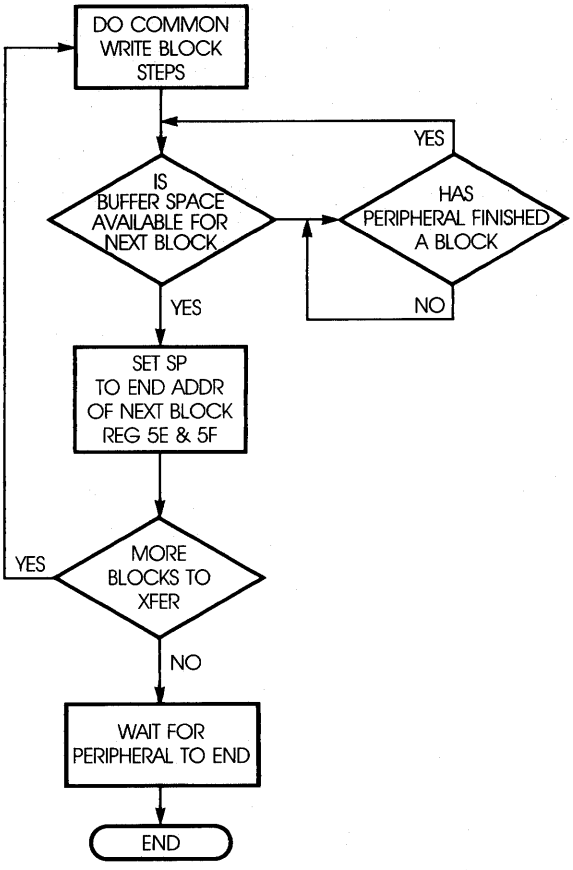
1. Clear all pointers (set Register 59 to O).*
2. Reset Read OP in DMA control (Register 53, bit 4).
3. Set SP to the address at the end of the block to be transferred.
4. Set the Write Latch (Register 53, bit 2). This causes the DMA cycles to begin.
5. Monitor DMA Done bit (Register 53, bit 5) to determine when DMA transfer is complete (WAP equals SP).
6. Transfer to the peripheral may now begin.

*In the 16-bit addressing mode, after setting Register 59 to O, also set RAPH (Register 5B) and WAPH (Register 5D) to O.



Multiple Block Write

1. Do the same first five operations as single block write.
2. Begin block transfer to peripheral.
3. Check that there is enough buffer for the next block without overrunning the RAP. If buffer space is available, set SP to end of next block.
4. If DMA Done was on, setting the new SP address will clear it and renew DMA transfers.



External Registers

In addition to these data transfer operations, certain data transfers are possible that happen external to the AIC-300 chip. These have to do with accesses to external Register 50, 51, and 70.

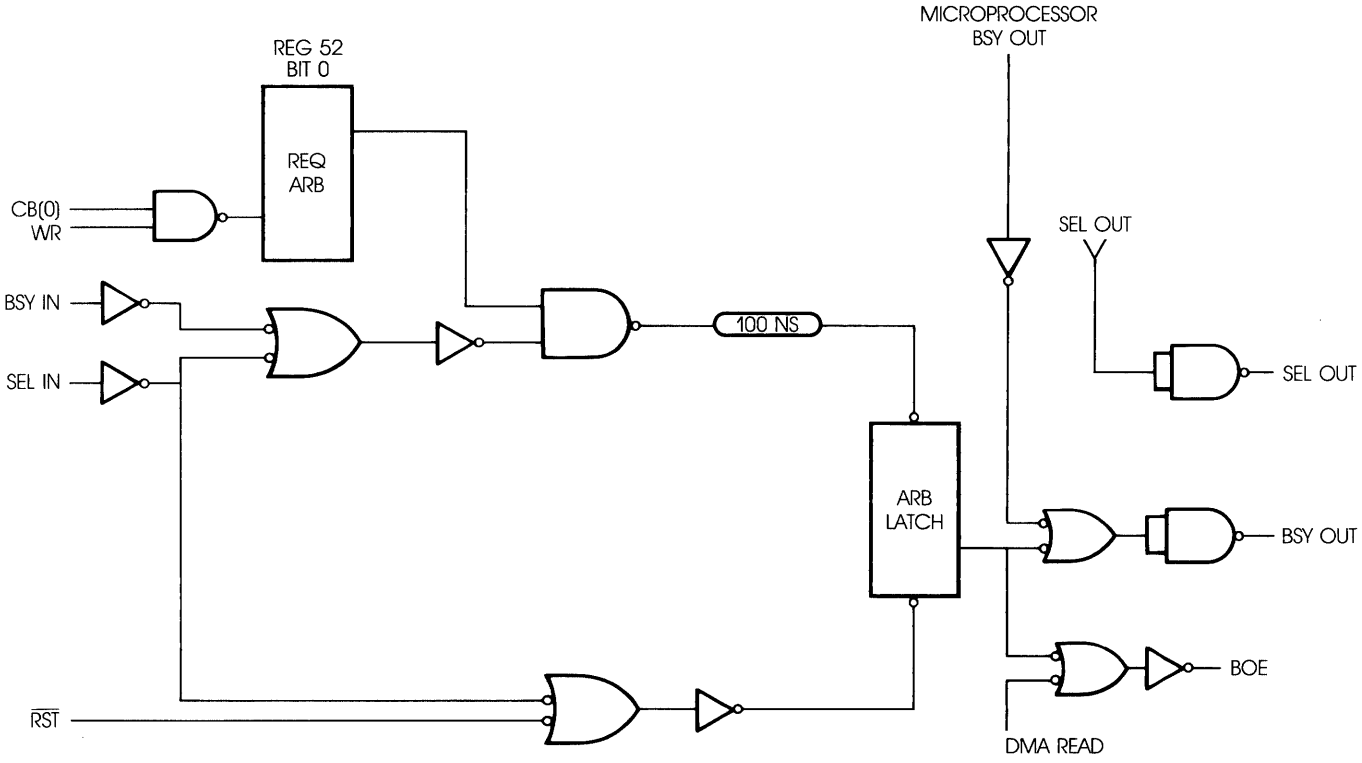
A Read/Write to Register 50 by the support processor is used to directly access the host data bus. During a read to Register 50, if bit 2 of Register 52 (BIE) was previously set, the BIE line (pin 35) will be asserted. The host data latch contents will then be placed on the data bus. During a write to Register 50, if bit 3 of Register 52 (BOE) was previously set, the LO line (pin 37) will first be asserted allowing the support processor data to be latched. This will be followed by BOE (pin 36) being asserted, allowing the latched data to become available on the host data bus. Typical configurations were shown in Figures 1 and 2.

An access to Register 70 is used by the support processor to access the data in the buffer. The address is generated by the AIC-300 chip, and is based on the contents of RAP (Registers 5A and 5B) if Register 53, bit 4, is reset (WOP); and on the contents of WAP (Registers 5C and 5D) if Register 53, bit 4, is set (ROP). The address pointer (RAP or WAP) is not incremented by a Register 70 access.

In the 16-bit addressing mode, to ensure proper operation during a Register 70 access, both RAP Registers (5A and 5B) and both WAP Registers (5C and 5D) must be loaded with the same value.

USE OF ARBITRATION

The Arbitration circuit is designed to allow rapid arbitration in two-wire arbitration systems. Setting Register 52, bit 0, sets a request for arbitration. The circuit monitors the Busy In and Select In pins, waiting for both to be deactivated. After a 100 ns bus-free condition, the circuit will begin arbitration support. The Bsy Out signal will be activated until Sel Out, Sel In, or Bsy In is active, or Bsy Out is reset by the microprocessor. External circuitry must be used to set or determine priority (for SCSI applications).



ABSOLUTE MAXIMUM RATINGS

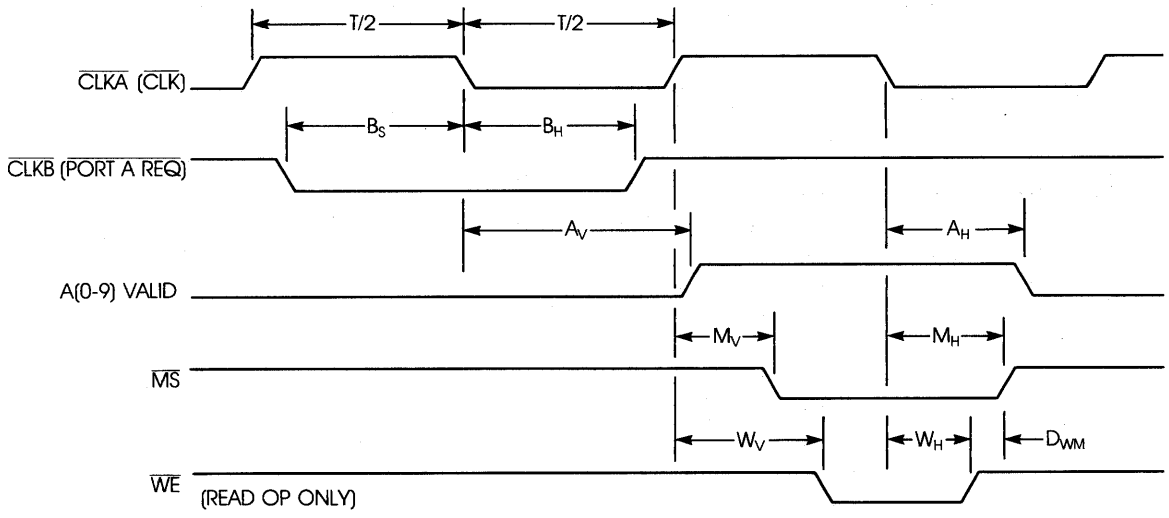
Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to 150°C
Voltage on Any Pin with Respect to Ground ..... −0.5 to 7 volts
Power Dissipation ..... 0.475 watt
Power Supply Voltage ..... 4.75 to 5.25 volts

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

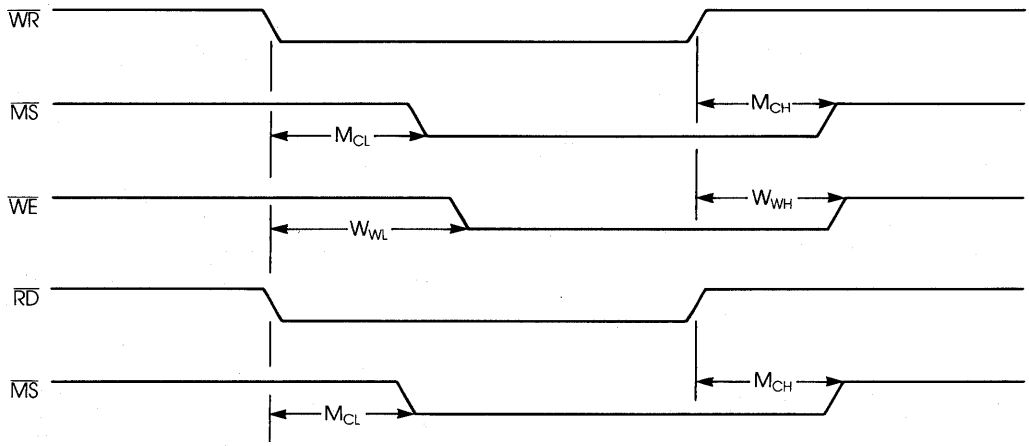
SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.40	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4			I_{OH} = −400 µA
I_{CC}	Supply Current		85	mA	
I_{IL}	Input Leakage	−10	10	µA	$0 < V_{IN} < V_{CC}$
I_{OL}	Output Leakage	−100	100	µA	$0.45 < V_{OUT} < V_{CC}$
C_{IN}	Input Capacitance		10	pF	
C_{OUT}	Output Capacitance		5	pF	

BUFFER RAM INTERFACE



SYMBOL	PARAMETER	MIN	MAX	UNITS
T/2	CLK Half Cycle	165		ns
B_S	$\overline{CLKB}$ ↓ to $\overline{CLKA}$ ↓ (Setup)	150		ns
B_H	$\overline{CLKA}$ ↓ to $\overline{CLKB}$ ↑ (Hold)	50		ns
A_V	$\overline{CLKA}$ ↓ to ADRS Valid		235	ns
A_H	$\overline{CLKA}$ ↓ to ADRS Valid	90		ns
M_V	$\overline{CLKA}$ ↑ to $\overline{MS}$ ↓		50	ns
M_H	$\overline{CLKA}$ ↓ to $\overline{MS}$ ↑	70	120	ns
W_V	$\overline{CLKA}$ ↑ to $\overline{WE}$ ↓		130	ns
W_H	$\overline{CLKA}$ ↓ to $\overline{WE}$ ↑	40	80	ns
D_{WM}	$\overline{WE}$ ↑ to $\overline{MS}$ ↑	20		ns

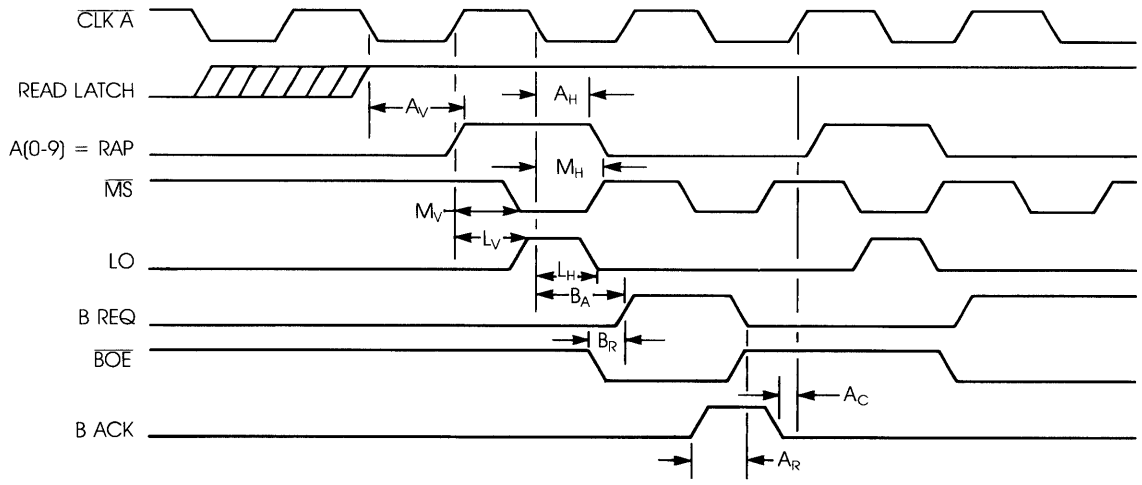
READ/WRITE REGISTER 70



SYMBOL	PARAMETER	MIN	MAX	UNITS
M_{CL}	$\overline{WR}$ or $\overline{RD}$ ↓ to $\overline{MS}$ ↓		105	ns
M_C	$\overline{WR}$ or $\overline{RD}$ ↑ to $\overline{MS}$ ↑		110	ns
W_W	$\overline{WR}$ ↓ to $\overline{WE}$ ↓		110	ns
W_{WH}	$\overline{WR}$ ↑ to $\overline{WE}$ ↑		115	ns

BUFFER TO HOST INTERFACE

READ OPERATION

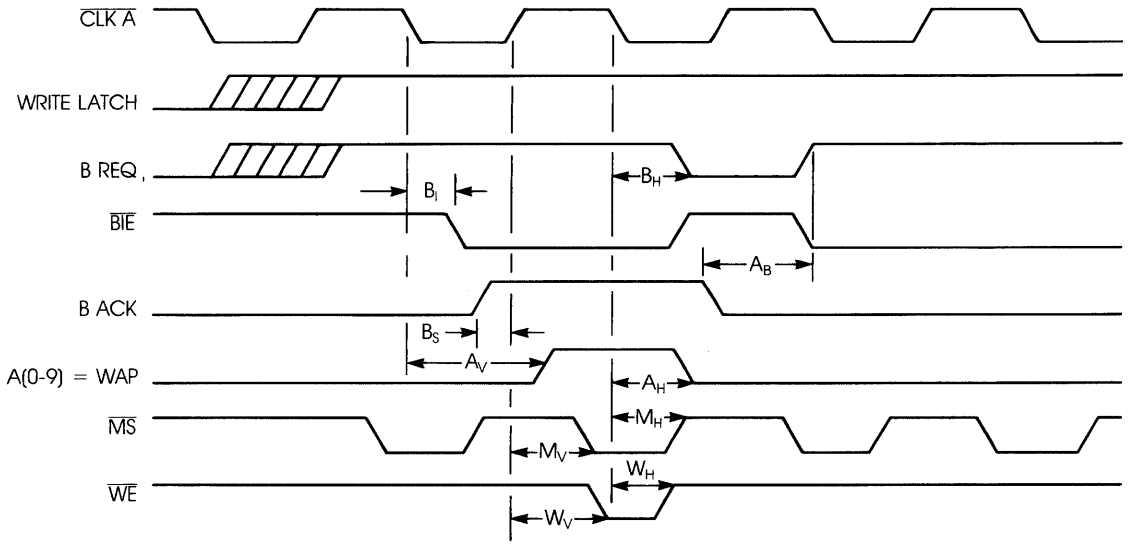


SYMBOL	PARAMETER	MIN	MAX	UNITS
A_V	$\overline{CLKA}$ ↓ to ADRS Valid		235	ns
A_H	$\overline{CLKA}$ ↓ to ADRS $\overline{Valid}$	90		ns
M_V	$\overline{CLKA}$ ↑ to $\overline{MS}$ ↓		50	ns
M_H	$\overline{CLKA}$ ↓ to $\overline{MS}$ ↑	70	120	ns
L_V	$\overline{CLKA}$ ↑ to LO ↑		130	ns
L_H	$\overline{CLKA}$ ↓ to LO ↓	40	80	ns
B_A	$\overline{CLKA}$ ↓ to BREQ ↑	90	200	ns
B_R	$\overline{BOE}$ ↓ to BREQ ↑	45		ns
A_C	BACK ↓ to $\overline{CLKA}$ ↑		70	ns
A_R	BACK ↑ to BREQ ↓		225	ns

NOTE: A Port A Req cycle has priority over a DMA cycle; i.e., if Port A Req is not active during the falling edge of $\overline{CLK}$, the following cycle is available for DMA. If Port A Req is active, $\overline{BIE}$ will be disabled for one CLK cycle.

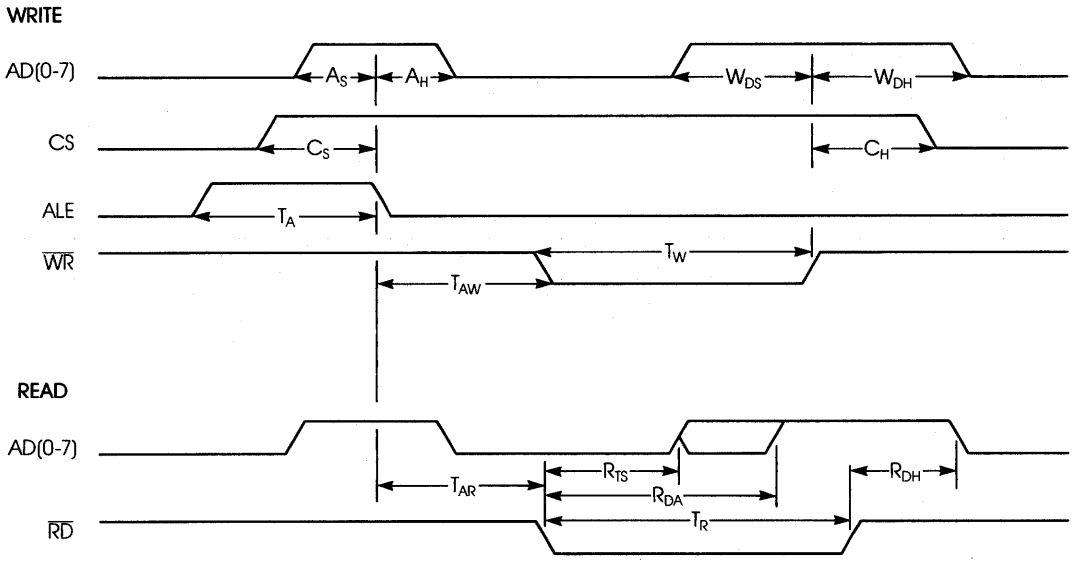
HOST TO BUFFER INTERFACE

WRITE OPERATION



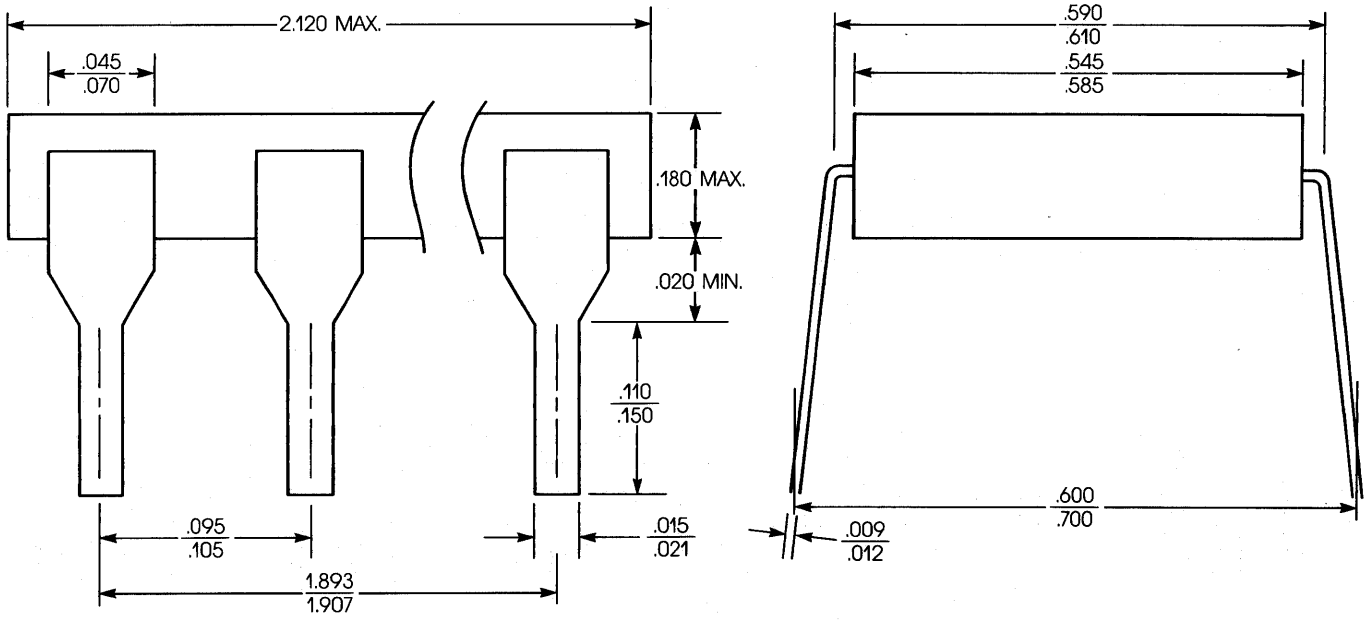
SYMBOL	PARAMETER	MIN	MAX	UNITS
B_I	$\overline{CLKA}$ ↓ to $\overline{BIE}$ ↓	25	60	ns
B_H	$\overline{CLKA}$ ↓ to BREQ ↓		225	ns
B_S	BACK ↑ to $\overline{CLKA}$ ↑	80		ns
A_V	$\overline{CLKA}$ ↓ to ADRS Valid		235	ns
A_H	$\overline{CLKA}$ ↓ to ADRS $\overline{Valid}$	90		ns
M_V	$\overline{CLKA}$ ↑ to $\overline{MS}$ ↓		50	ns
M_H	$\overline{CLKA}$ ↓ to $\overline{MS}$ ↑	70	120	ns
W_V	$\overline{CLKA}$ ↑ to $\overline{WE}$ ↓		130	ns
W_H	$\overline{CLKA}$ ↓ to $\overline{WE}$ ↑	40	80	ns
A_B	BACK ↓ to BREQ ↑		125	ns

MICRO-PROCESSOR INTERFACE



SYMBOL	PARAMETER	MIN	MAX	UNITS
T_A	ALE Width	150		ns
T_A	ALE ↓ to $\overline{WR}$ ↓	90		ns
T_{AR}	ALE ↓ to $\overline{RD}$ ↓	90		ns
T_W	$\overline{WR}$ Width	160		ns
T_R	$\overline{RD}$ Width	215		ns
A_S	ADRS Valid to ALE ↓	90		ns
A_H	ALE ↓ to ADRS $\overline{Valid}$	10		ns
C_S	CS Valid to ALE ↓	15		ns
C_H	$\overline{RD}$ or $\overline{WR}$ ↑ to CS ↓	10		ns
W_{DS}	Write Data Valid to $\overline{WR}$ ↑	70		ns
W_{DH}	$\overline{WR}$ ↑ to Write Data $\overline{Valid}$	60		ns
R_{TS}	$\overline{RD}$ ↓ to AD(0-7) Out Active	50		ns
R_{DH}	$\overline{RD}$ ↓ to Read Data Valid		275	ns
R_{DH}	$\overline{RD}$ ↑ to Read Data $\overline{Valid}$		110	ns

PACKAGING INFORMATION



40-Lead Plastic Dual-in-line Package

adaptec, inc.
580 Cottonwood Drive, Milpitas, CA 95035 • (408) 946-8600

STOCK NO: 500002-00
ASB/SB/CBM