CAL DATA 135
EMULATE BOARD
(P/N C81080210)

TECHNICAL MANUAL
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TABLES

ILLUSTRATIONS

SECTION 1
INTRODUCTION

1.1   SCOPE

This manual provides the information needed to understand and maintain the Cal Data 135 Emulate Board (part number C81080210) when used with the drawing package provided. The information in this manual is for the use of a skilled technician familiar with standard test equipment, solid-state logic theory, common maintenance practices and standard troubleshooting techniques. A basic knowledge of design principles and circuits used in small computers is assumed, hence no tutuorial material of this kind is included.

As a stand-alone publication, this manual has a good functional and physical description of the Emulate Board, providing the information needed to understand the capabilities and features of the board. The maintenance coverage of this manual is commensurate with the pre-requisite skills and knowledge of the defined user, characteristics of the product and maintainability requirements established by Cal Data.

1.2   DOCUMENTATION

This manual describes the 135 Emulate Board of a Cal Data 1 Computer system that is equipped with a Cal Data 100 Engine (CPU) and a MACROBUS Channel Adapter (MCA).

The following paragraphs define publications and conventions that support this manual.

1.2.1   Publications

Figure 1-1 shows the relationship of system documentation to hardware elements. Controlled copies of publications, provided in accordance with the terms of the purchase contract, are kept current for the life of the product.

1.2.2   Engineering Drawings

For maintenance purposes, this manual is supported by a theory of operation and a drawing package that contains schematic diagrams, assembly drawings and other required engineering drawings. The drawing package is updated with the latest revision of each drawing.

1.2.3   Abbreviations and Conventions

Table 1-1 lists the abbreviations found in this manual.

Conventions used in the text of this manual include:

    a.   Equipment panel nomenclature is reproduced in all upper-case characters.

PUBLICATIONS						SYSTEM HARDWARE	
TM	TO	DP	IM	UM	①		
X	X	X				POWER SUPPLY	
					18	SMALL I/O BOARD	*
					17	MEMORY OR I/O BOARD	
					16	I/O BOARD	
					15	MEMORY OR I/O BOARD	
					14	MEMORY OR I/O BOARD	
X	X	X	X		13	MEMORY OR I/O BOARD	
					12	MEMORY OR I/O BOARD	
					11	MEMORY OR I/O BOARD	
X	X	X			10	MEMORY OR I/O BOARD	
					9	MEMORY OR I/O BOARD	
					8	MEMORY OR I/O BOARD OR OPTION	
					7	MEMORY OR I/O BOARD OR OPTION	
					6	OPTION	
X	X	X			5	EMULATE BOARD	
X	X	X			4	ENGINE BOARD 1	
					3	ENGINE BOARD 2	
X	X	X			2	MACROBUS CHANNEL ADAPTER	
X	X	X			1	MACROPANEL	
		X	X	X		Computer System	
				X		Engine Microprogramming	

MEMORY

I/O BOARD OR OPTION

NOTES:
  A Standard 18-Slot Backplane is Shown

* = MACROBUS Terminator or Extension Cable

① TM = Technical Manual
  TO = Theory of Operation
  DP = Engineering Drawing Package
  IM = Installation Manual
  UM = User Manual

Figure 1-1. Relationship of Publications to Cal Data 1 System Elements

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b. The proper names of instructions, microcommands and signals are capitalized.

c. ZERO and ONE are used to express binary logic "0" and "1" states, respectively.

d. Hexadecimal numbers are preceded by a dollar sign for easy identification.

e. A colon (:) is used to indicate a range of bits. For example the range of Address bits A12 to A04 is written A12:A04.

Table 1-1. Abbreviations

Abbreviation	Meaning
Cal Data	California Data Processors
CPU	central processing unit (Engine)
MCA	MACROBUS Channel Adapter
ROM	read-only memory
K	1,024 (addresses or memory locations)
EIA	emulate instruction address
PSW	processor status word
I/O	input/output
PC	program counter
FR	file register
IR	instruction register
PS	processor (macro)status register
MS	microstatus register
CC	microcommand location counter
MB	M bus
AB	A-operand bus
cm	centimeter
Vdc	volts, direct current
psi	pounds per square inch
kg/cm^2	kilograms per square centimeter
cfm	cubic feet per minute
lps	liters per second
$^{\circ}C$	degrees, Celsius
µA	microampere
mA	milliampere
ns	nanosecond
TTL	transistor-transistor logic
V	volts
max	maximum
min	minimum

2.1 GENERAL

Emulate Boards are "language conentrators" that allow the Cal Data 100 Engine to emulate the functions performed by a variety of computers at average speeds comparable to the machines being emulated. To the user, the Cal Data 1 system with an Emulate Board (Figure 2-1) is transparent to all applicable software of the machine being emulated.

Because of differences in system architecture, some emulated instructions are executed faster and some slower in the Cal Data system with the Emulate Board. For this reason, and due to the asynchronous operation of the MACROBUS (whereby direct-memory-access devices can come on-line at any time), time-dependent program loops should be avoided to ensure complete program interchangability between the Cal Data 135 and the machine being emulated.

The Cal Data 100 Engine has all the elements of a very fast and versatile CPU, but without an I/O structure. An I/O capability is provided by an I/O channel adapter and associated I/O channel structure. For the Cal Data 135 system, a MACROBUS Channel Adapter is used. These are all the basic elements required for a successful emulation; however, such an emulation can be slow due to the distribution of data and control bits that must be analyzed in different emulated instructions. This makes decoding and arithmetic comparisons difficult. The Emulate Board works with the Engine to provide custom, high-speed instruction-decoding logic to perform the emulation at comparable average program speed.

2.2 EMULATE INSTRUCTION ADDRESS

To emulate instructions, the CPU executes appropriate firmware microcommand sequences from control memory. Depending on the instruction being emulated, different sequences are executed in a specific order. To save time, Emulate Board logic (Figure 2-2) sufficiently decodes each instruction to determine the microcommand sequence(s) to execute. Furthermore, the Emulate Board generates (by table lookup) the starting address within control memory of each required microcommand sequence. This address is called the emulate instruction address (EIA).

Three kinds of EIA are generated by the Emulate Board, according to the sequence being processed:

    a. Operand-sequence addresses from the emulate operand table

    b. Execution-sequence addresses from the emulate execute table

    c. CPU-interrupt vector addresses from the interrupt entry table

Table 2-1 shows the relationship between operand and execution sequences within the complete emulation for double-operand, single-operand and
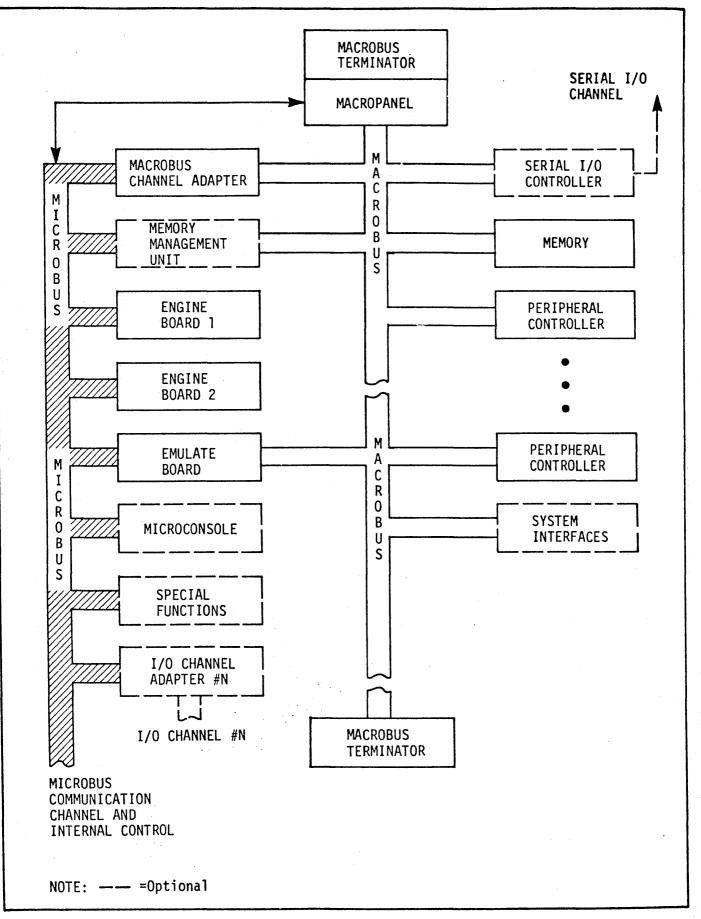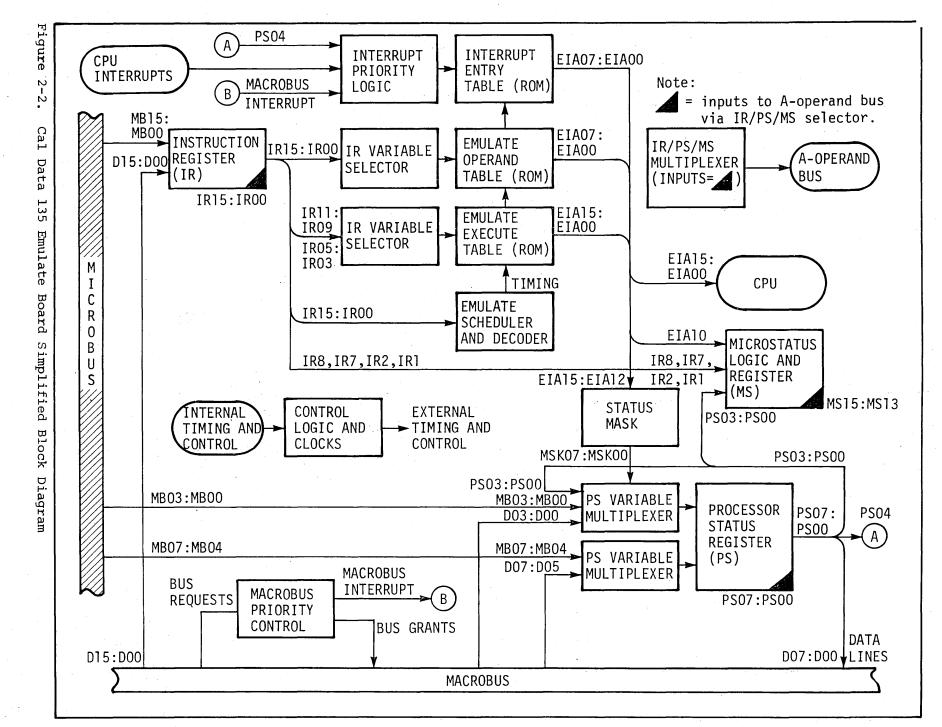
Figure 2-1. Cal Data 1 Computer System Organization

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Figure 2-2. Cal Data 135 Emulate Board Simplified Block Diagram

control instructions. CPU-interrupt vector addresses are enabled when needed by the interrupt priority logic.

One or two operand sequences are required for each single- or double-operand programmed instruction, respectively. Each operand sequence fetches one operand from the appropriate location.

An execution sequence is required for the emulation of any instruction, with or without operands. The execution sequence performs the function specified by the emulated instruction. Although different instructions often call for execution of the same operand sequences, each instruction generally has a separate execution sequence. Firmware associated with the execution sequence indicates the end of a complete emulation and enables the beginning of the next programmed instruction, if any.

An interrupt vector address is generated for each recognized interrupt.

Table 2-1. Emulation Sequences

Step	Double-Operand Instruction	Single-Operand Instruction	Control Instruction
1	Operand sequence	Operand sequence	Execution sequence
2	Operand sequence	Execution sequence	--
3	Execution sequence	--	--

2.3   EMULATE EXECUTE TABLE

The emulate execute table is an ROM addressed by selected control bits of the instruction being emulated. For each possible combination of bits selected by the variable selector and the decoder, and applied to the table, a 16-bit control word is output.

Eight bits of the output control word comprise the execution-sequence EIA sent to the CPU microcommand location counter (CC). Four bits are used for special control functions within the emulation logic.

The most-significant four bits output from the emulate execute table control the modification of bits 03:00 of the processor status word (PSW). This modification is under firmware control. These PSW bits are the status flags required by the program (03 = negative, 02 = zero, 01 = overflow and 00 = carry). The emulate execute table provides rapid and specific updating of these bits in the single cycle following the execution of the instruction (i.e., just after the fetch for the next instruction is issued). The updated PSW can be read from the Emulate Board at either the macrolevel via the MACROBUS, or the microlevel via the A-operand bus (AB; part of the Microbus). The instruction register (IR) or the micro-status register (MS) can also be read via AB by execution of an appropriate microcommand. The information placed on AB is determined by the emulate IR/PS/MS multiplexer, which is controlled by the address generated in the A-operand field of the microcommand.

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2.4   SPECIFICATIONS

General specifications for the Emulate Board are given in Table 2-2.

Table 2-2.   Cal Data 135 Emulate Board Specifications

Characteristic	Specification	
Interface	Two connectors (A and B) interface with the standard MACROBUS. Six connectors (C, D, E, F, J1 and J2) interface with the Microbus.	
Power	Operating Amperes	Voltage Tolerance
+5 Vdc	3.5 ±10%	±5%
Configuration	Hex-width printed-circuit board	
Dimensions	15.7 by 8.9 inches (39.9 by 22.7 cm)	
Mounting Centers	0.75 inch (1.91 cm) recommended minimum	
Ambient Temperature	0 to +50° C	
Airflow	115 cfm (54 lps)	
Ambient Humidity	10 to 90% relative, without condensation	

SECTION 3
PHYSICAL DESCRIPTION

3.1 GENERAL

The Emulate Board (Figure 3-1) is a hex-width board 15.7 by 8.9 inches (39.9 by 22.7 cm) that normally plugs into slot 5 of the Cal Data computer chassis.* The right-hand edge of the board has a 1.0 by 5.5 inch (2.5 by 14.0 cm) cutout as clearance for the side-mounted cooling fans in the chassis.

There are no controls or adjustable elements on the 135 Emulate Board.

3.2 CONNECTORS

There are six printed-circuit connectors (A to F) on the bottom edge of the board, and two (J1 and J2) on the top edge. Connectors A and B interface with the MACROBUS. Connectors C to F, and J1 and J2 interface with the main computer Microbus. Connectors A to F are standard backplane connectors. Connectors J1 and J2 plug into two small processor-interconnection boards.

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*Because of the universal connections in the CPU area of the chassis, the Emulate Board can operate in any slot from 1 to 6.

15.69"

0.99"

A1 A30 ② A1 A30

J2 J1

COMPONENT SIDE

5.55" 8.94"

F E D C B A

FV1 FA1 EV1 EA1 DV1 DA1 CV1 CA1 BV1 BA1 AV1 ① AA1

② Solder Side = B1 to B30. Likewise with connector J2.

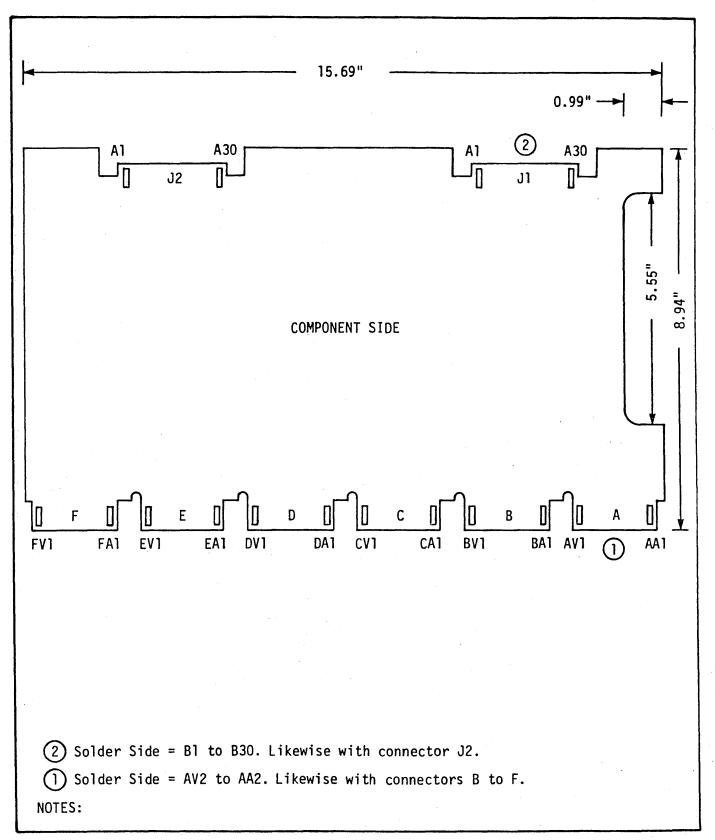① Solder Side = AV2 to AA2. Likewise with connectors B to F.

NOTES:

Figure 3-1. Cal Data 135 Emulate Board

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4.1   GENERAL

The Emulate Board interfaces with the other computer boards via the chassis backplane, which includes the MACROBUS, and via two small interconnection boards spanning the tops of the computer boards.

The interface with the MACROBUS (connectors A and B) conforms to the standard interfacing rules for I/O compatibility, described in the MACROBUS Channel Adapter Technical Manual, C21518013.

4.2   SIGNALS

Backplane connectors are labeled A to F. A and B carry the MACROBUS, and C to F interface with the main computer Microbus. Connectors on the small processor-interconnection board are labeled J1 and J2. Pin assignments for all interface connectors are listed in Appendix A.

4.3   CIRCUITS

Because the Emulate Board is attached to the MACROBUS along with peripheral devices and memory, the MACROBUS loading introduced by the board is an important system consideration for configurations with a large amount of memory or numerous peripheral devices. The Emulate Board minimizes the loading of receivers and the leakage current of drivers in the high state (these being the critical bus-loading parameters). This is accomplished in two ways:

    a. The driver leakage load is limited to that of one gate instead of two (as is common in some logic designs).

    b. A Cal Data proprietary bus receiver circuit improves speed and reduces drive requirements.

4.3.1   Line Driver

The line driver is a TTL buffer. The critical MACROBUS specifications for the device are:

Output low voltage at 50 mA sink (V_{OL})	+0.5 V max
Output high leakage current at 2.5 V (I_{OH})	+60 µA max

4.3.2   Line Receiver

The Emulate Board uses a Cal Data line receiver. The critical MACROBUS specifications for this device are:

Input high threshold (V_{IH})	+2.5 V min
Input low threshold (V_{IL})	+1.4 V max
Input current at +2.5 V (I_{IH})	+60 µA max
Input current at 0.0 V (I_{IL})	+25 µA max

4.3.3   MACROBUS Loading

The limiting MACROBUS loading occurs on the bidirectional data lines that have one receiver and one driver for each I/O module. Worst-case MACROBUS load specifications are:

V_{IH}	+2.5 V min
V_{IL}	+1.4 V max
I_{IH}	+120 µA max at +2.5 V
I_{IL}	+25 µA max at 0.0 V

SECTION 5
MAINTENANCE

5.1 GENERAL

This section describes preventive and corrective maintenance procedures that apply to the Cal Data 135 Emulate Board. In general, corrective maintenance is limited to the isolation of a fault to the Emulate Board followed by replacement of the board. Troubleshooting can then be used to verify that the suspected module is malfunctioning and to help diagnose the specific problem. Repair should be conducted at the factory or by an authorized representative.

5.2 PREVENTIVE MAINTENANCE

The Emulate Board is a reliable solid-state device designed to perform continuously for many years. Preventive maintenance consists of performing the following tasks every six months:

    a.   Inspect the board for damaged wires, components or other obvious defects.

    b.   Using a low-pressure source of air (75 psi one foot from the board or 5 kg/cm^2 30 cm from the board), blow off accumulated dust and foreign matter.

Another aspect of preventive maintenance is proper handling of the board. The following points should be observed:

    a.   Always be sure that system power is OFF before installing or removing any board.

    b.   Install each board with the component side toward the front of the chassis. Check each board for proper orientation before attempting to install it. Because the connectors are keyed, excessive force applied to a reversed board can result in connector damage. Make sure that the board is completely and evenly seated.

    c.   Insert and remove each board slowly and carefully so that it does not make contact with adjacent boards.

    d.   Never use components as finger grips; use the grip areas at the corners of the board.

    e.   To prevent oxides from forming on the gold plating, do not touch connectors.

5.3   CORRECTIVE MAINTENANCE

Repair or adjustment of the Emulate Board in the field is not recommended. If a malfunction is detected, replace the board with a spare known to be operating properly and return the malfunctioning board for repair to California Data Processors or an authorized representative.

Name	Signal	Pin	Pin	Signal	Name
Initialize	* BUS INIT-L	A1	A2	+5V	+5 Vdc
Interrupt	* BUS INTR-L	B1	B2	GND	Ground
Data 00	BUS D00-L	C1	C2	GND	Ground
Data 02	BUS D02-L	D1	D2	BUS D01-L	Data 01
Data 04	BUS D04-L	E1	E2	BUS D03-L	Data 03
Data 06	BUS D06-L	F1	F2	BUS D05-L	Data 05
Data 08	BUS D08-L	G1	H2	BUS D07-L	Data 07
Data 10	BUS D10-L	J1	J2	BUS D09-L	Data 09
Data 12	BUS D12-L	K1	K2	BUS D11-L	Data 11
Data 14	BUS D14-L	L1	L2	BUS D13-L	Data 13
Parity Bit Low	* BUS PA-L	M1	M2	BUS D15-L	Data 15
Ground	GND	N1	N2	*BUS PB-L	Parity Bit High
Ground	GND	P1	P2	*BUS BBSY-L	Bus Busy
Ground	GND	R1	R2	*BUS SACK-L	Selection Acknowledgement
Ground	GND	S1	S2	*BUS NPR-L	Nonprocessor Request
Ground	GND	T1	T2	BUS BR7-L	Bus Request 7
Nonprocessor Grant	* BUS NPG-H	U1	U2	BUS BR6-L	Bus Request 6
Bus Grant 7	* BUS BG7-H	V1	V2	GND	Ground

* These signals are assigned on the backplane but are not used on this assembly.

Name	Signal	Pin	Pin	Signal	Name
Bus Grant 6	* BUS BG6-H	A1	A2	+5V	+5 Vdc
Bus Grant 5	* BUS BG5-H	B1	B2	GND	Ground
Bus Request 5	BUS BR5-L	C1	C2	GND	Ground
Ground	GND	D1	D2	BUS BR4-L	Bus Request 4
Ground	GND	E1	E2	* BUS BG4-H	Bus Grant 4
AC Low	* BUS ACLO-L	F1	F2	* BUS DCLO-L	DC Low
Address 01	BUS A01-L	H1	H2	* BUS A00-L	Address 00
Address 03	BUS A03-L	J1	J2	BUS A02-L	Address 02
Address 05	BUS A05-L	K1	K2	BUS A04-L	Address 04
Address 07	BUS A07-L	L1	L2	BUS A06-L	Address 06
Address 09	BUS A09-L	M1	M2	BUS A08-L	Address 08
Address 11	BUS A11-L	N1	N2	BUS A10-L	Address 10
Address 13	BUS A13-L	P1	P2	BUS A12-L	Address 12
Address 15	BUS A15-L	R1	R2	BUS A14-L	Address 14
Address 17	BUS A17-L	S1	S2	BUS A16-L	Address 16
Ground	GND	T1	T2	BUS C1-L	Control 1
Slave Synchronization	BUS SSYN-L	U1	U2	* BUS C0-L	Control 0
Master Synchronization	BUS MSYN-L	V1	V2	GND	Ground

* These signals are assigned on the backplane but are not used on this assembly.

Name	Signal	Pin	Pin	Signal	Name
M Bus 00	MB000-L	A1	A2	+5V	+5 Vdc
M Bus 01	MB001-L	B2	B2	-15V	-15 Vdc
M Bus 02	MB002-L	C1	C2	GND	Ground
M Bus 03	MB003-L	D1	D2	MB004-L	M Bus 04
M Bus 05	MB005-L	E1	E2	MB006-L	M Bus 06
M Bus 07	MB007-L	F1	F2	MB008-L	M Bus 08
M Bus 09	MB009-L	H1	H2	MB010-L	M Bus 10
M Bus 11	MB011-L	J1	J2	MB012-L	M Bus 12
M Bus 13	MB013-L	K1	K2	MB014-L	M Bus 14
M Bus 15	MB015-L	L1	L2	AB000-H	A Bus 00
A Bus 01	AB001-H	M1	M2	AB002-H	A Bus 02
A Bus 03	AB003-H	N1	N2	AB004-H	A Bus 04
A Bus 05	AB005-H	P1	P2	AB006-H	A Bus 06
A Bus 07	AB007-H	R1	R2	AB008-H	A Bus 08
A Bus 09	AB009-H	S1	S2	AB010-H	A Bus 10
Ground	GND	T1	T2	AB011-H	A Bus 11
A Bus 13	AB013-H	U1	U2	AB012-H	A Bus 12
A Bus 15	AB015-H	V1	V2	AB014-H	A Bus 14

Name	Signal	Pin	Pin	Signal	Name
Power Failure Interrupt	PFINT-H	A1	A2	+5V	+5 Vdc
Halt Interrupt	HLINT-H	B1	B2	*-15V	-15 Vdc
Data Switch 16	* DS16-H	C1	C2	GND	Ground
Data Switch 17	* DS17-H	D1	D2	* LTCL-L	Line-Frequency Clock
Virtual Address	* VIRTAD-H	E1	E2	* PBBSY-L	Processor Bus Busy
Control Count 00	* CC000-L	F1	F2	HALTP-L	Panel Halt
Control Count 01	* CC001-L	H1	H2	*MSR15-L	Microstatus Register 15
Control Count 02	* CC002-L	J1	J2	RESET-L	Reset
Control Count 03	* CC003-L	K1	K2	*BUS BG7-IN	Bus Grant 7 In
Control Count 04	* CC004-L	L1	L2	BUS BG7-OUT	Bus Grant 7 Out
Control Count 05	* CC005-L	M1	M2	*BUS BG6-IN	Bus Grant 6 In
Control Count 06	* CC006-L	N1	N2	BUS BG6-OUT	Bus Grant 6 Out
Control Count 07	* CC007-L	P1	P2	*BUS BG5-IN	Bus Grant 5 In
Control Count 08	* CC008-L	R1	R2	BUS BG5-OUT	Bus Grant 5 Out
Control Count 09	* CC009-L	S1	S2	*BUS BG4-IN	Bus Grant 4 In
Ground	GND	T1	T2	BUS BG4-OUT	Bus Grant 4 Out
Control Count 10	* CC010-L	U1	U2	*BUS NPG-IN	Nonprocessor Grant In
Control Count 11	* CC011-L	V1	V2	*BUS NPG-OUT	Nonprocessor Grant Out

* These signals are assigned on the backplane but are not used on this assembly.

Name	Signal	Pin	Pin	Signal	Name
Control Memory 00	CM000-H	A1	A2	+5V	+5 Vdc
Control Memory 01	* CM001-H	B1	B2	* -15V	-15 Vdc
Control Memory 02	* CM002-H	C1	C2	GND	Ground
Control Memory 03	* CM003-H	D1	D2	* CM004-H	Control Memory 04
Control Memory 05	* CM005-H	E1	E2	CM006-H	Control Memory 06
Control Memory 07	* CM007-H	F1	F2	* EMINH-L	Emulate Inhibit
Control Memory 09	* CM009-H	H1	H2	* CM008-H	Control Memory 08
Control Memory 11	* CM011-H	J1	J2	* CM010-H	Control Memory 10
Decode Address 00	* DAD00-H	K1	K2	* CM012-H	Control Memory 12
Control Memory 13	* CM013-H	L1	L2	* CM014-H	Control Memory 14
Control Memory 15	* CM015-H	M1	M2	* DAD01-H	Decode Address 01
Control Memory 17	* CM017-H	N1	N2	* CM016-H	Control Memory 16
Control Memory 19	* CM019-H	P1	P2	* CM018-H	Control Memory 18
Switch Register 0	* SR0-L	R1	R2	* CM020-H	Control Memory 20
Control Memory 21	* CM021-H	S1	S2	* CM022-H	Control Memory 22
Ground	GND	T1	T2	CM024-H	Control Memory 24
Control Memory 23	* CM023-H	U1	U2	CM026-H	Control Memory 26
Control Memory 25	CM025-H	V1	V2	CM027-H	Control Memory 27

* These signals are assigned on the backplane but are not used on this assembly.

Name	Signal	Pin	Pin	Signal	Name
Control Memory 28	CM028-H	A1	A2	+5V	+5 Vdc
Control Memory 29	* CM029-H	B1	B2	* -15V	-15 Vdc
Control Memory 31	* CM031-H	C1	C2	GND	Ground
Control Memory 31	* CM030-H	D1	D2	* CM032-H	Control Memory 32
Control Memory 33	* CM033-H	E1	E2	* CM034-H	Control Memory 34
Control Memory 35	* CM035-H	F1	F2	* DAD02-H	Decode Address 02
Control Memory 37	* CM037-H	H1	H2	* CM036-H	Control Memory 36
Control Memory 39	* CM039-H	J1	J2	* CM038-H	Control Memory 38
Instruction Repeat	IRPTE-L	K1	K2	* CM040-H	Control Memory 40
Control Memory 41	* CM041-H	L1	L2	* CM042-H	Control Memory 42
Control Memory 43	* CM043-H	M1	M2	* CPEN-L	Control Panel Enable
Control Memory 45	* CM045-H	N1	N2	* CM044-H	Control Memory 44
Control Memory 47	* CM047-H	P1	P2	* CM046-H	Control Memory 46
Decode Address 03	* DAD03-H	R1	R2	* ACMSL-L	Alterable Control Memory Select
	Reserved	S1	S2	* AUXRM-L	Auxiliary ROM Select
Ground	GND	T1	T2	IRINH-L	Instruction Inhibit
	Reserved	U1	U2	IWAIT-L	Instruction Wait
System Clock	SYSCK-L	V1	V2	GND	Ground

*These signals are assigned on the backplane but are not used on this assembly

Name	Signal	Pin	Pin	Signal	Name
Skip	* SKIPP-L	1A	1B	EMA00-H	Emulate Address 00
AR Write Enable	ARWEN-L	2A	2B	EMA01-H	Emulate Address 01
Stack Limit Write Enable	* SLWEN-L	3A	3B	EMA02-H	Emulate Address 02
Slave Synchronization Error	SSYER-H	4A	4B	EMA03-H	Emulate Address 03
Double Slave Synchronization Error	DSYER-H	5A	5B	EMA04-H	Emulate Address 04
Load Special Function	LDSPF-H	6A	6B	EMA05-H	Emulate Address 05
Fatal Interrupt	* FINTP-L	7A	7B	EMA06-H	Emulate Address 06
Special Function	SPFNC-H	8A	8B	EMA07-H	Emulate Address 07
Panel Halt	HALTP-L	9A	9B	Reserved	
	Reserved	10A	10B	* PSSEL-L	Program Status Select
Carry	* CARRY-H	11A	11B	Reserved	
	Reserved	12A	12B	Reserved	
Address Error	ADERR-H	13A	13B	Reserved	
Program Status 03	PS003-L	14A	14B	Reserved	
	Reserved	15A	15B	* XD007-L	Inhibit Destination File 0 to 7
	Reserved	16A	16B	* XD815-L	Inhibit Destination File 8 to 15
	Reserved	17A	17B	* XB815-L	Inhibit B-Field File 8 to 15
Control Count Write Enable	* CCWEN-H	18A	18B	* XB007-L	Inhibit B-Field File 0 to 7
Static Condition	* STATIC-L	19A	19B	* LITRL-L	Literal
Master Synchronization	MSYN-H	20A	20B	* PLUS1-L	Plus 1
Special Function 04	SPF04-L	21A	21B	PSWEN-L	Processor Status Write Enable
B Bus Inhibit	* BBINH-L	22A	22B	IRWEN-L	IR Write Enable
B Bus 01	* BB001-H	23A	23B	* BB000-H	B Bus 00
B Bus 03	* BB003-H	24A	24B	* BB002-H	B Bus 02
B Bus 05	* BB005-H	25A	25B	* BB004-H	B Bus 04
B Bus 07	* BB007-H	26A	26B	* BB006-H	B Bus 06
B Bus 09	* BB009-H	27A	27B	* BB008-H	B Bus 08
B Bus 11	* BB011-H	28A	28B	* BB010-H	B Bus 10
B Bus 13	* BB013-H	29A	29B	* BB012-H	B Bus 12
B Bus 15	* BB015-H	30A	30B	* BB014-H	B Bus 14

*These signals are assigned on the small processor interconnection board but are not used on this assembly.

Name	Signal	Pin	Pin	Signal	Name
Load CC Register	* LOADC-L	1A	1B	Reserved	
Bus Request	* BREQ-H	2A	2B	MINTP-L	Microinterrupt
Bus Grant	BGRNT-L	3A	3B	* BYTDA-L	Byte Data
Bus Grant Enable	BGEN-H	4A	4B	Reserved	
Memory Management Inhibit	MMINH-L	5A	5B	* MARLD-H	Management Address Load
Data Inhibit	* DAINH-L	6A	6B	* CCCEN-H	CC Count Enable
Special Function 7	* SPF07-L	7A	7B	* SPR1A-L	Special Register 1A
Special Function 5	* SPF05-L	8A	8B	* SPR19-L	Special Register 19
Special Function 6	* SPF06-L	9A	9B	* SPR1B-L	Special Register 1B
Special Function Decode	* SPFNC-H	10A	10B	* MLTPY-L	Multiply
Inhibit B Field	INHBF-L	11A	11B	* ENSPF-H	Enable Special Function
Emulate	EMLAT-H	12A	12B	CR008-H	Microcommand Register 08
Power Failure	PFAIL-L	13A	13B	Reserved	
AU Carry In	* AUCIN-L	14A	14B	Reserved	
Write	WRITE-L	15A	15B	FILE6-H	File 6
IR Read	IRERD-H	16A	16B	* XA815-L	Inhibit A-Field File 8 to 15
Interrupt	INTR-H	17A	17B	* XA007-L	Inhibit A-Field File 0 to 7
Memory Management C0	* MMC0-L	18A	18B	* RSTRA-L	Restore A
Memory Management C1	* MMC1-L	19A	19B	YELLW-L	Yellow
Microcommand Register 07	CR007-H	20A	20B	BYTMD-L	Byte Mode
Stack Limit Interrupt	SLINT-H	21A	21B	* MS006-H	Microstatus Register 06
DR Write Enable	* DRWEN-L	22A	22B	* RRWEN-L	RR Write Enable
Emulate Instruction Address 01	EIA001-H	23A	23B	EIA000-H	Emulate Instruction Address 00
Emulate Instruction Address 03	EIA003-H	24A	24B	. EIA002-H	Emulate Instruction Address 02
Emulate Instruction Address 05	EIA005-H	25A	25B	EIA004-H	Emulate Instruction Address 04
Emulate Instruction Address 07	EIA007-H	26A	26B	EIA006-H	Emulate Instruction Address 06
Emulate Instruction Address 09	EIA009-H	27A	27B	EIA008-H	Emulate Instruction Address 08
Emulate Instruction Address 11	EIA011-H	28A	28B	EIA010-H	Emulate Instruction Address 10
Emulate Instruction Address 13	EIA013-H	29A	29B	EIA012-H	Emulate Instruction Address 12
Emulate Instruction Address 15	EIA015-H	30A	30B	EIA014-H	Emulate Instruction Address 14

*These signals are assigned on the small processor interconnection board but are not used on this assembly.

The tables in this appendix give approximate instruction execution
times for the Cal Data 135. The values given have a tolerance of
ten percent and are calculated assuming a 165-ns clock and one Cal Data
8KX16 memory module as the main storage element.

Table B-1. Single-Operand Instruction Timing (Microseconds)

Instruction	Address Mode							
	0	1	2	3	4	5	6	7
JMP	–	1.5	1.8	2.1	2.0	2.3	2.1	2.8
JSR	–	2.8	3.0	3.3	3.0	3.4	3.3	4.0
TST(B)	1.6	2.0	2.6	3.0	2.6	3.1	3.0	3.8
CLR(B)	1.6	2.1	2.5	2.6	2.5	2.8	2.6	3.5
COM(B)	1.6	2.8	3.1	3.3	3.1	3.5	3.3	4.0
INC(B)	1.6	2.8	3.1	3.3	3.1	3.5	3.3	4.0
DEC(B)	1.6	2.8	3.1	3.3	3.1	3.5	3.3	4.0
NEG(B)	1.6	2.8	3.1	3.3	3.1	3.5	3.3	4.0
ASL(B)	1.6	2.8	3.1	3.3	3.1	3.5	3.3	4.0
ADC(B)	1.6	2.8	3.1	3.3	3.1	3.5	3.3	4.0
SBC(B)	1.6	2.8	3.1	3.3	3.1	3.5	3.3	4.0
ASR(B)	1.6	2.8	3.1	3.3	3.1	3.5	3.3	4.0
ROR(B)	1.6	2.8	3.1	3.3	3.1	3.5	3.3	4.0

Table B-2. MOV(B) Instruction Timing (Microseconds)

Destination Mode	Source Mode							
	0	1	2	3	4	5	6	7
0	2.0	2.6	2.6	3.3	2.6	3.3	3.3	4.1
1	2.5	3.1	3.1	3.8	3.1	3.8	3.8	4.6
2	2.8	3.6	3.6	4.3	3.6	4.3	4.3	5.1
3	3.0	3.8	3.8	4.5	3.8	4.5	4.5	5.6
4	2.8	3.6	3.6	4.3	3.6	4.3	4.3	5.1
5	3.1	4.0	4.0	4.6	4.0	4.6	4.6	5.4
6	3.0	3.8	3.8	4.5	3.8	4.5	4.5	5.3
7	3.6	4.5	4.5	5.1	4.5	5.1	5.1	5.9

Table B-3. Typical Double-Operand Instruction Timing (Microseconds): BIS(B), BIC(B), ADD, SUB

Destination Mode	Source Mode							
	0	1	2	3	4	5	6	7
0	2.0	2.6	2.6	3.3	2.6	3.3	3.3	4.1
1	3.1	3.8	3.8	4.5	3.8	4.5	4.5	5.3
2	3.5	4.1	4.1	4.8	4.1	4.8	4.8	5.6
3	3.6	4.3	4.3	4.9	4.3	4.9	4.9	6.1
4	3.5	4.1	4.1	4.8	4.1	4.8	4.8	5.6
5	3.8	4.5	4.5	5.1	4.5	5.1	5.1	5.9
6	3.6	4.3	4.3	5.0	4.3	5.0	5.0	5.6
7	4.9	4.9	4.9	5.6	4.9	5.6	5.6	6.4

Table B-4. Control, Branch and Miscellaneous Instruction Timing

Instruction	Time (Microseconds)
Conditional Branch	1.5 for branch 2.0 for no branch
RTS	2.1
RTI	3.0
RTT	3.1
Traps	5.6
Branch (BR)	1.7
SCC	1.5
CCC	1.5
HALT	1.5
MARK	2.3
SOB	1.6 for branch 1.5 for no branch
WAIT	1.3 (interrupts checked every 0.33 microsecond)