6639 DISK CONTROLLER TRAINING MANUAL

TEST EDITION

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FOR TRAINING PURPOSES ONLY

This manual was compiled and written by members of the instructional staff of

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CHAPTER I

INTRODUCTION

INTRODUCTION

Controllers, or Synchronizers as they are sometimes called, are responsible for transfering the commands of the computer to peripheral equipment. In most cases there is a great time differential in the operating speed of the computer and I/O, therefore the controller must be the go-between for these two very different devices. It was decided early in the 6000 program (after the first five 6600's were built) that the most economical way to handle 6000 peripheral equipment was to use the already built 3000 I/O equipment and associated controllers. This entails the use of some type of adapter because the communication from a 6000 data channel is much different than that of a 3000 channel. This adapter, called a Data Channel Converter, was constructed and designated a 6681. At that time however there was no controller available in the 3000 line for handling the Display Console or the Bryant Disk so special 6000 controllers were developed for these two devices. These last two controllers are built into the computer main frame while the 6681 is in an external air-cooled low boy cabinet. The 3000 controllers and equipments are not modified.

CHANNEL OPERATION

A review of data channel operation might aid in the understanding of controller operation. A channel can have many controllers tied to it, however more than two per channel is seldom required due to the number of channels available. Controllers are connected in serial, that is the first controller on the channel receives everything and must pass it on to the second controller, etc. Data or control signals coming from the last controller must pass thru all preceding units to get back to the channel. All signals are retimed as they pass thru the controller by use of a pass on or pass back circuit.

See Figure 1 for a typical example. The timing involved in either of these circuits is such that exactly 100 ns are consumed. This means that the third equipment on a channel would receive information 200 ns late and lose 200ns in its returned response. Obviously this could have a detrimental effect in time utilization if a great deal of information is involved. Therefore the last equipment on a channel should be one used only rarely.

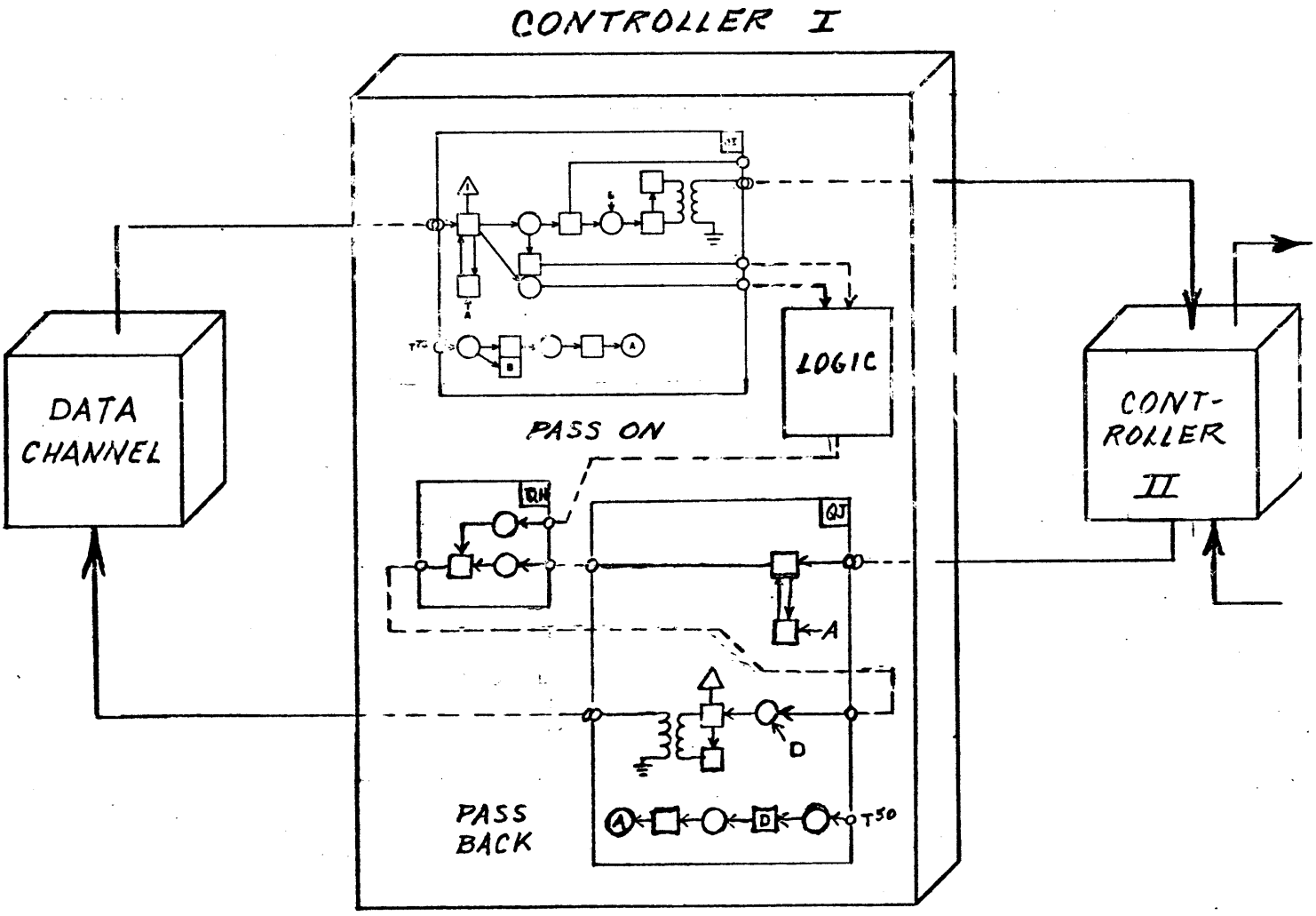


FIGURE 1-1 SERIAL CONTROLLER CONNECTION

SIGNAL FLOW

The channel exists in two states, Active or Inactive, which it passes on to the controller. The Inactive state will allow functions to be processed. When the channel generates a FUNCTION SIGNAL (76 or 77 instruction) and sends it to the controller it expects an INACTIVE response. When data is to be transfered the channel must be active. A FULL signal accompanies each 12-bit data word and a EMPTY response is made no matter which direction the data is flowing. For an output operation the channel brings up its data and FULL to start the operation, the controller always sends back an EMPTY. On input operations the controller does not receive an EMPTY until it has sent the first data and FULL. It does however receive an extra EMPTY in response to the last data word. Provision is made within the controller so that an END OF RECORD will cause an INACTIVE response instead of a FULL, and the read operation will be terminated. Additional information can be found in the PPU Training Manual. The controllers on a designated channel are selected by the upper three bits of the function sent to them. The select code for each controller is given in the 6400/6600 Code Book, however this code can be changed for individual sites by minor revisions. In most cases an equipment is deselected by sending a function with a different select code.

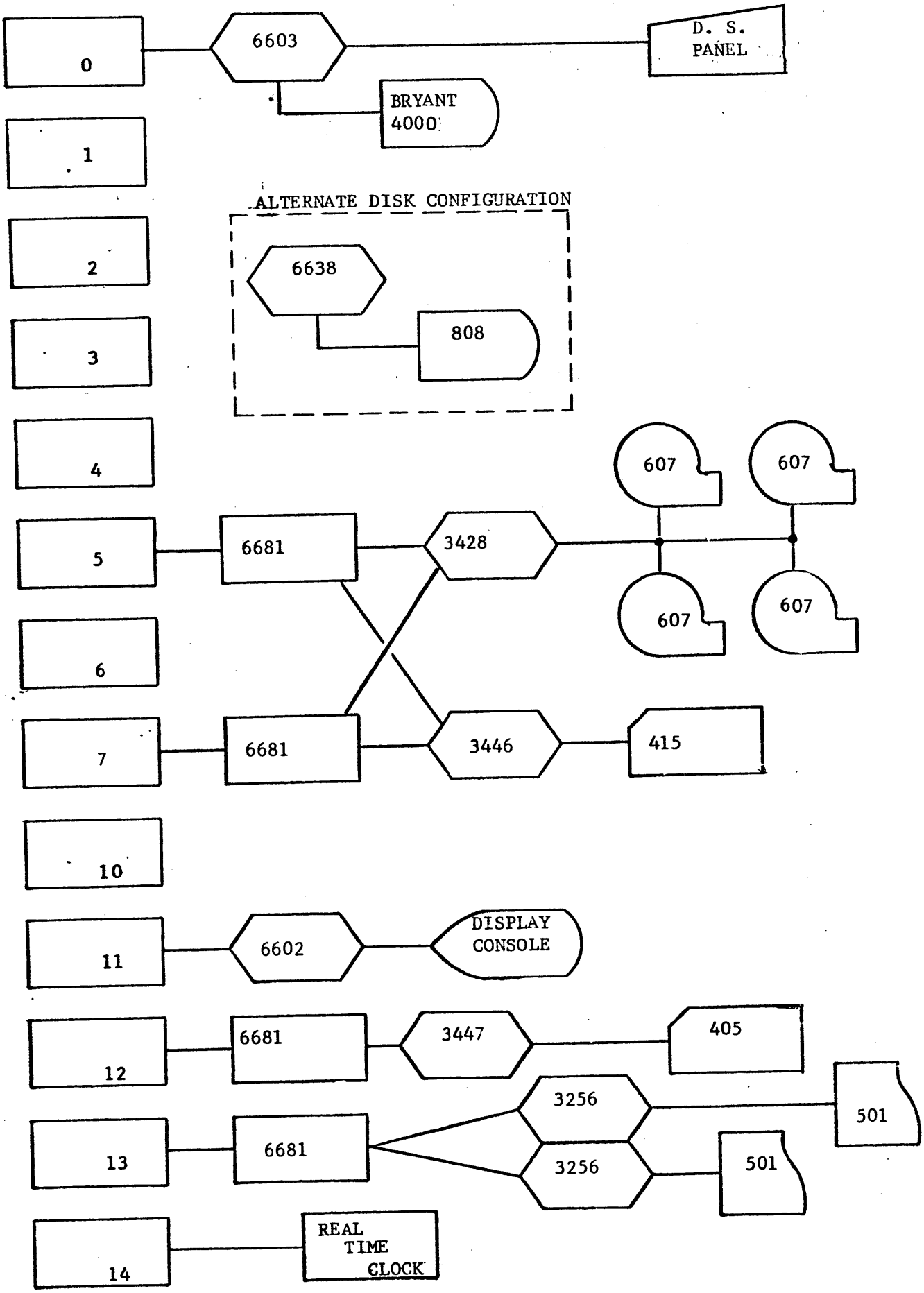


Figure 1-2. 6000 Peripheral Equipment Usage

CHAPTER II

6639/808

INTRODUCTION

The disk, along with the display console, is one of the most important pieces of peripheral equipment in the 6000 system. The operating system relys on the disk for storage of operating routines, incoming jobs, object programs, terminated jobs for printing, and many other miscellaneous purposes. The overall speed of the computer is pretty much limited to the speed and programming capabilities of the disk. An understanding of disk operation is essential to the maintenance of the system and is helpful to the programmer and operator as well. The basic configuration is shown in Fig. 2-1.

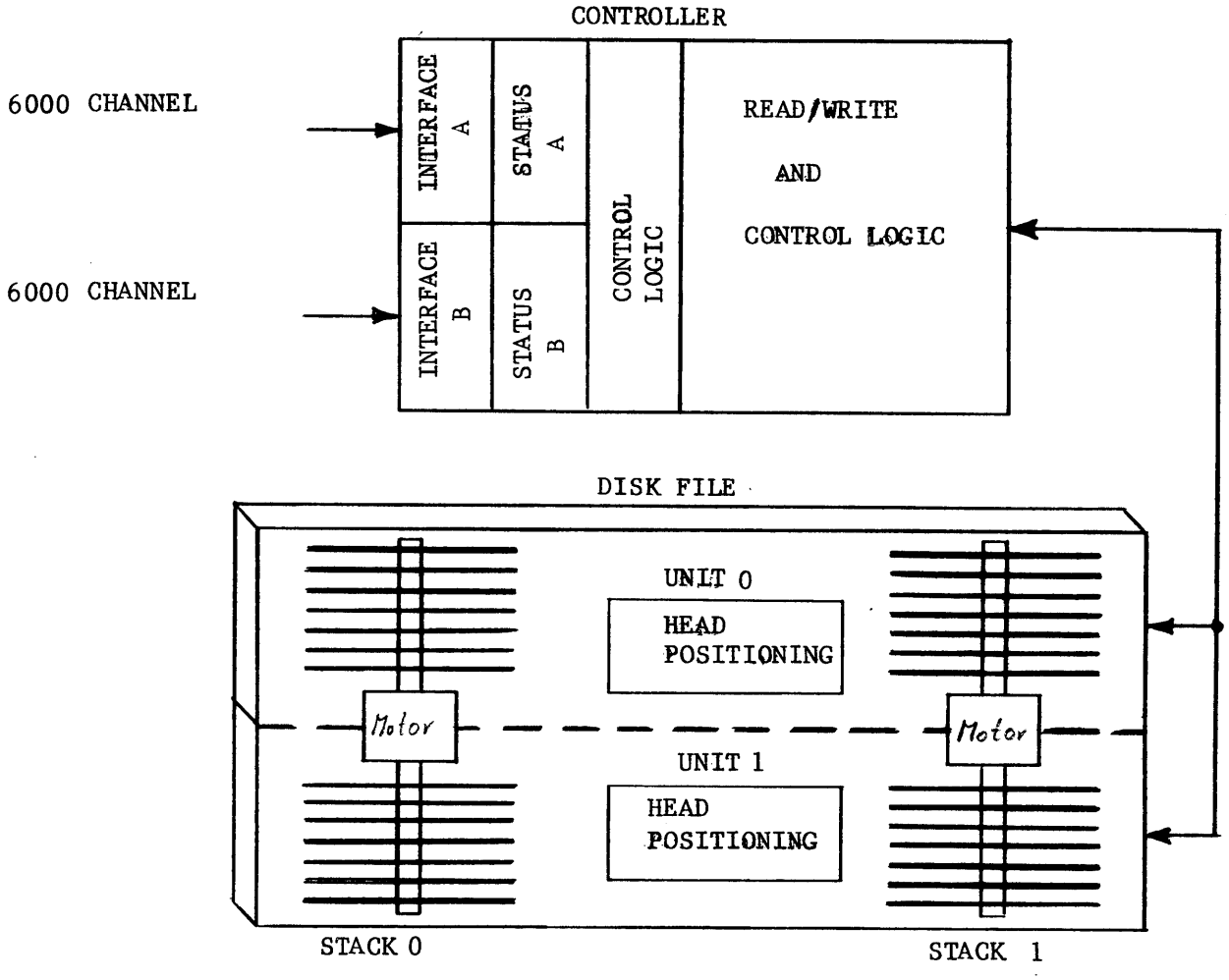
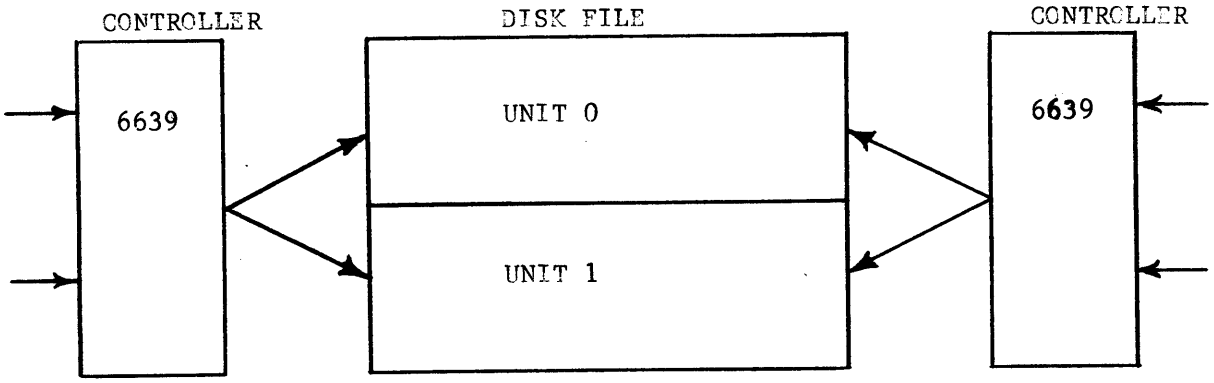


Figure 2-1. Basic System Block Diagram

Note that the 6639 is a two channel controller. It is housed in a separate air-cooled chasis and can be as far as 75 ft. from the computer. If desired a different computer could be tied to each channel giving a path for data flow from computer to computer or to simply give the disk maximum utilization of time. An even greater time saving is realized by using two controllers as shown in Figure 2. Since the disk file is essentially two separate independently operating units, a number of different operations can occur simultaneously.



igure 2-2. System for Maximum Time Utilization

As previously stated the 808 disk is made up of two units. Each unit contains two stacks of 18 disks each. For the most part all surfaces are used for data storage, 128 surfaces for the complete file. Two surfaces, one on each stack, are used for clock signals and 4 surfaces (total) are used for track verification information. Total capacity of the file is 84 million 12-bit words, however this is not normally achieved due to the method the computer uses for organizing information on the file. Figure 3 illustrates the use of disk surfaces on one stack, both stacks have the same configuration.

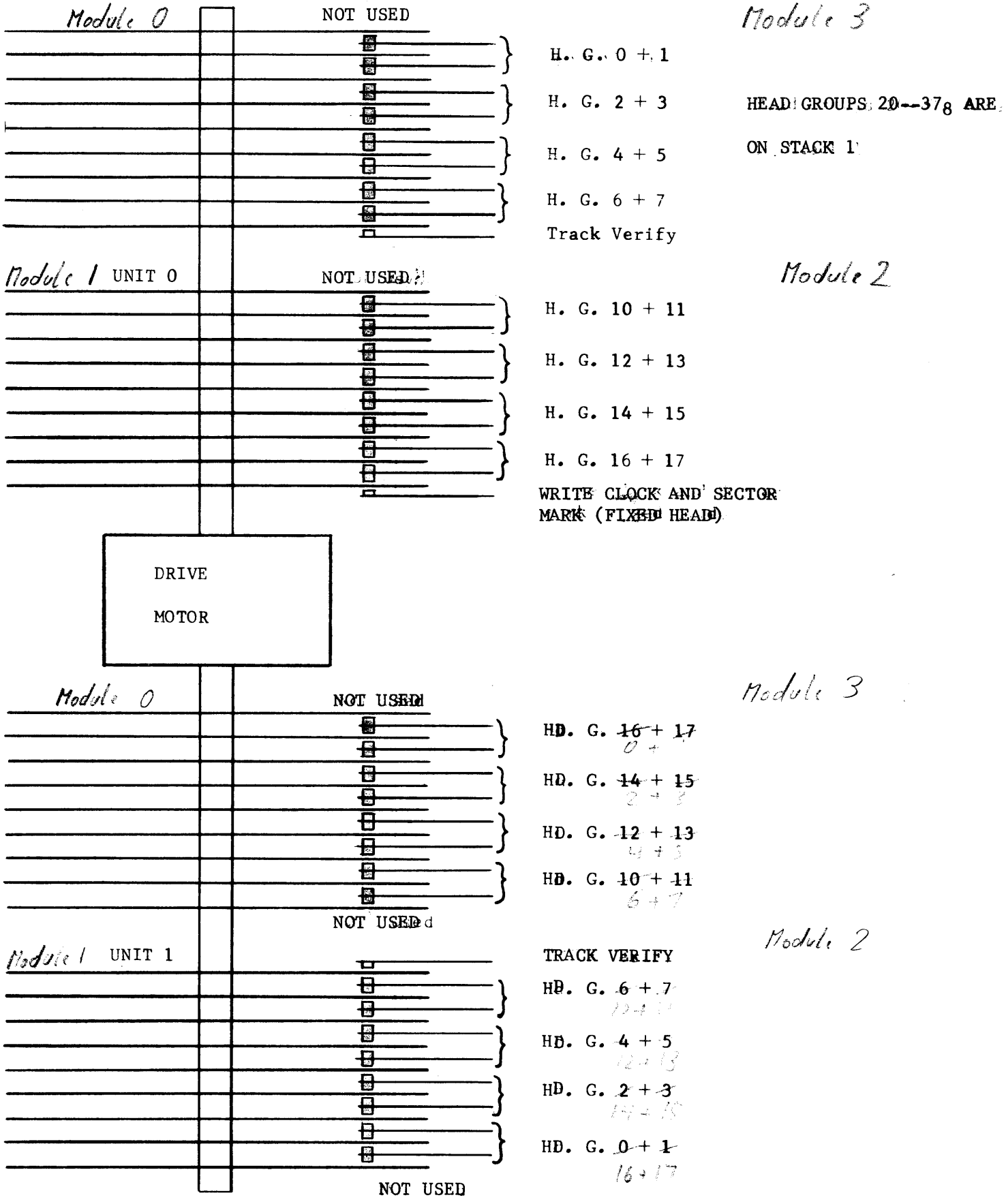


Figure 2-3. Disk Usage (Stack 0)

Data is organized on the disk surface by track and sector. Each surface is divided into 100 pie shaped sectors which are addressable by program operations. Sector number is determined from the clock track which has a sector pulse at the beginning of each sector. An index is used as the starting point for counting sectors. By making the read/write heads moveable, a series of tracks are established on the disk surface. The head positioning system of each unit is independant so that each unit can operate on a separate track, however the head positioning system works in a horizontally opposed manner causing each stack within a unit to be at the same track position. Figure 4 shows the data format within a sector. Each sector contains 430 words, but only 322 of these are data. A preamble of 80 words consisting of alternate ones and zeros terminated by two ones is written to overcome the gap between the erase and the write heads. (All data is written erase before write.) The 322 data words consist of 100$_8$ central memory words plus a file mark. After data is written, the postamble of 3 guard words and the parity is automatically recorded. The rest of the postamble consists of garbage. 12-bit words are recorded in parallel on four disk surfaces. The surfaces used are determined by a programmed head group select. There are 32 possible head groups on each unit. Each head pad has 6 heads, 3 being used at a time.

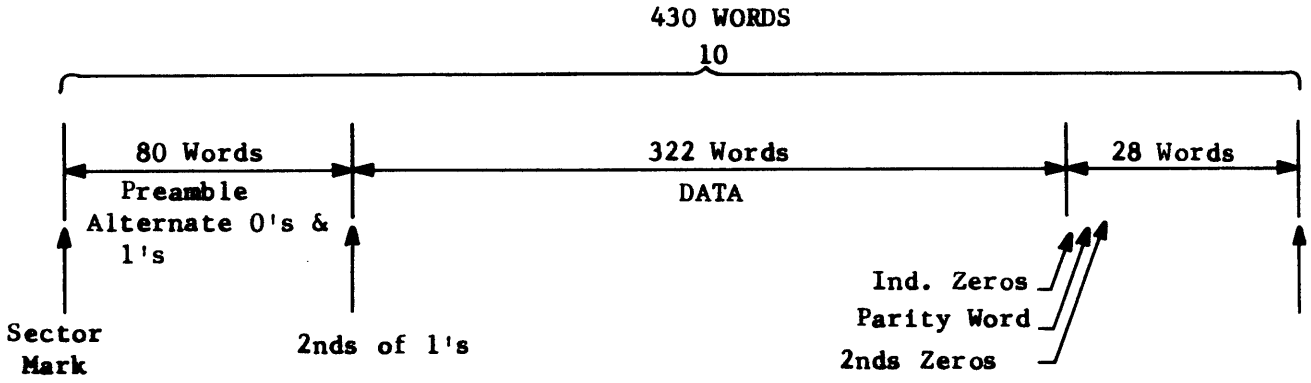


Figure 2-4. Sector Format

Phased modulation is used for writing data. Data is compared with the write clock from the clock disk, and written in phase or out of phase dependant on a one or a zero. Data is read using a read clock developed by an oscillator synchronized by the preamble of the sector. This eliminates any possible errors due to a paralax. While reading, the same parity generator develops a parity word which is compared against the parity word on the disk to determine if a parity error exists.

CLOCK SYSTEM

In order to be an adapter between the computer and the disk, the 6638 must use of the clocks of both units. The computer clock area is no different than any other controller with the exception that each interface must have its own system, since two different computers might be involved. When a channel is connected, its clock becomes the controller clock. The disk file feeds three different clock signals to the controller. Only one of these is used at any one time and they are all very close to a square wave with a 1.2 usec period. There is a write clock derived from the clock track of each unit. This is normally used, the last unit selection determining which one. The read clock is used only during read operations. The selected clock is broken down into 4 timing pulses of 50 nsec duration as shown in Figure 5. These timing pulses control all operations where the disk file is involved.

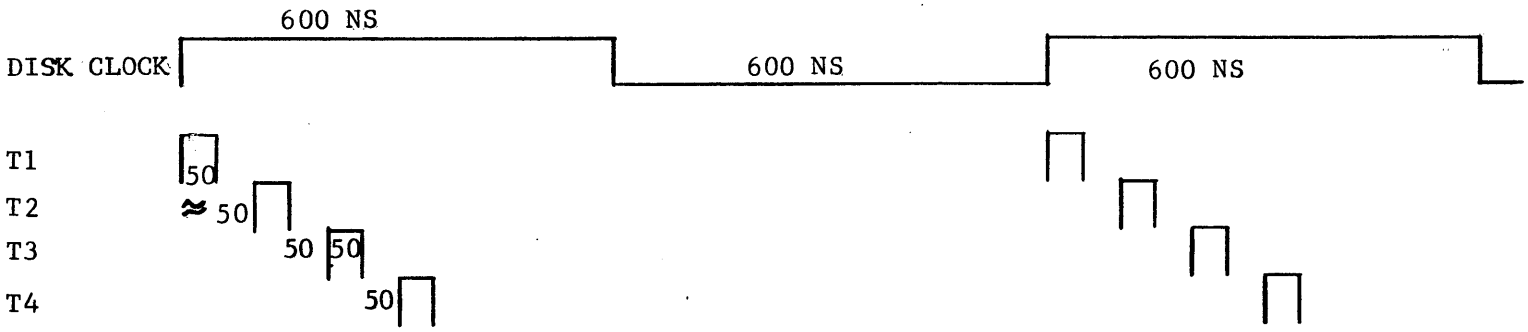
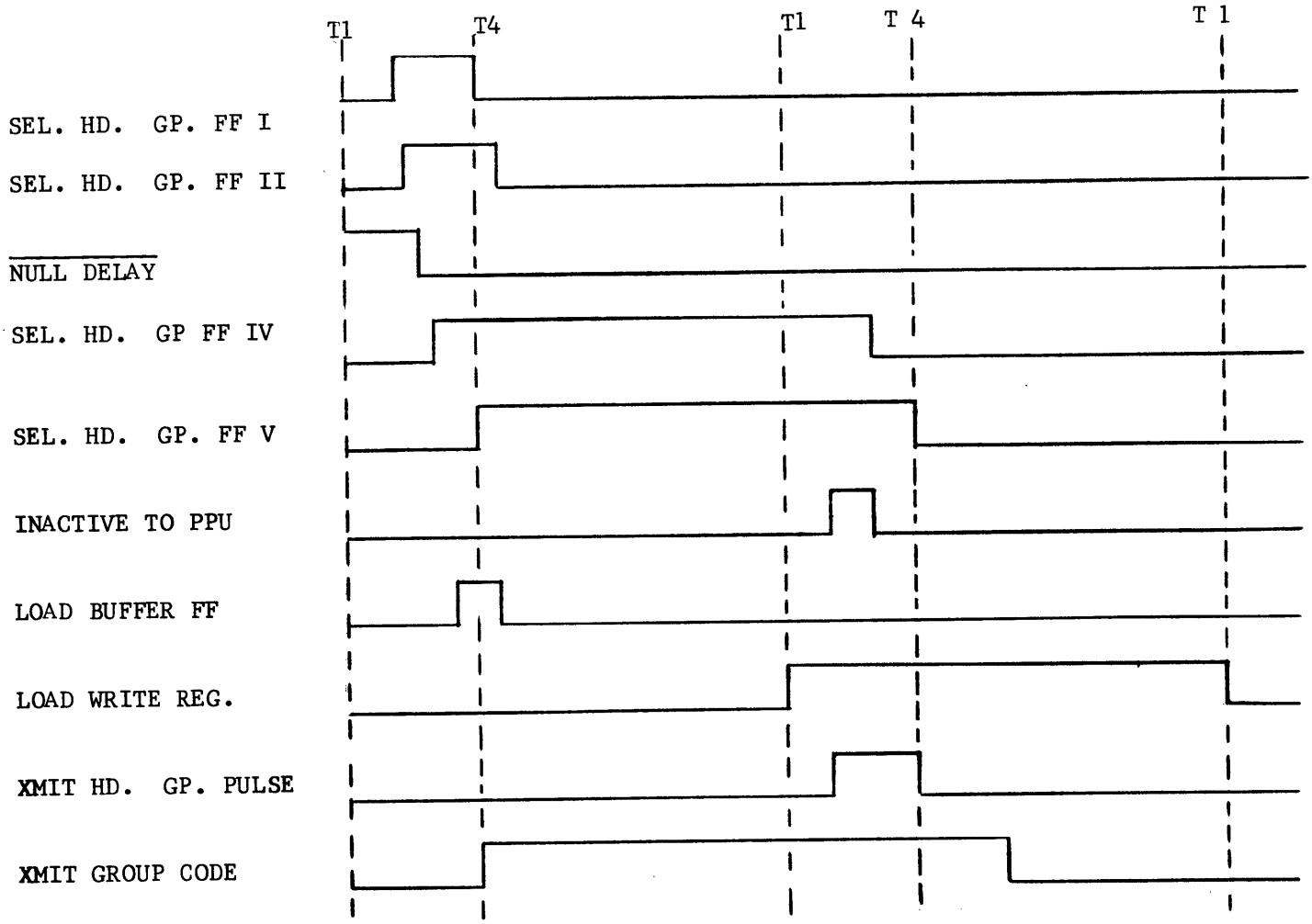


Figure 2-5. Disk Clocking

CONNECT AND STATUS

Since the 6639 has inputs for 2 channels, there are 2 identical interfaces for connecting and obtaining status. The status operation (17XX) must always be performed to determine if the other channel is using the common area of the controller. Any function other than connect and status sent from a channel while the other channel is using the 6639 will cause the requesting channel to hang up. If the controller is free when the request is made it will hold a connection until other functions are initiated. The controller must be disconnected by a 1740 or 1540 code. There is a built in delay in interface B which will allow A to connect in case of simultaneous requests. The status word is gated to the channel upon activating after the status function is performed. See 6400/6600 code book for status responses. Unit selection is performed with the lowest bit of the connect and status function.



Fi re 2-6. Head Group Sel. Timing

HEAD GROUP SELECT

The head group selection is accomplished within the disk file. It is the responsibility of the controller to generate a HEAD GROUP PULSE and pass the head group code on to the file. The controller initiates 2 delays while executing a head group selection. A 30 usec head switch delay prevents sending a read or write enable signal to the disk, and a 4 ms null delay if the stack is changed which disables beginning a read or write by droping the ready condition of the system. The amplitude of the head group selection determines the stack selected, $0\text{-}17_8$ = stack 0, $20\text{-}37_8$ = stack 1. See Figure 2-6 for timing of the head group select.

POSITION SELECT

The position select function causes the position servo system of the disk file to select a new track on the disk. The controller must generate a POSITION PAUSE and pass the selected track on to the file. See Figure 2-7. The position select also initiates the null delay, however in addition a track verification is made before a ready condition is established. Repositioning the heads causes the track verify head to move in conjunction with the data heads. (Figure 2-3)

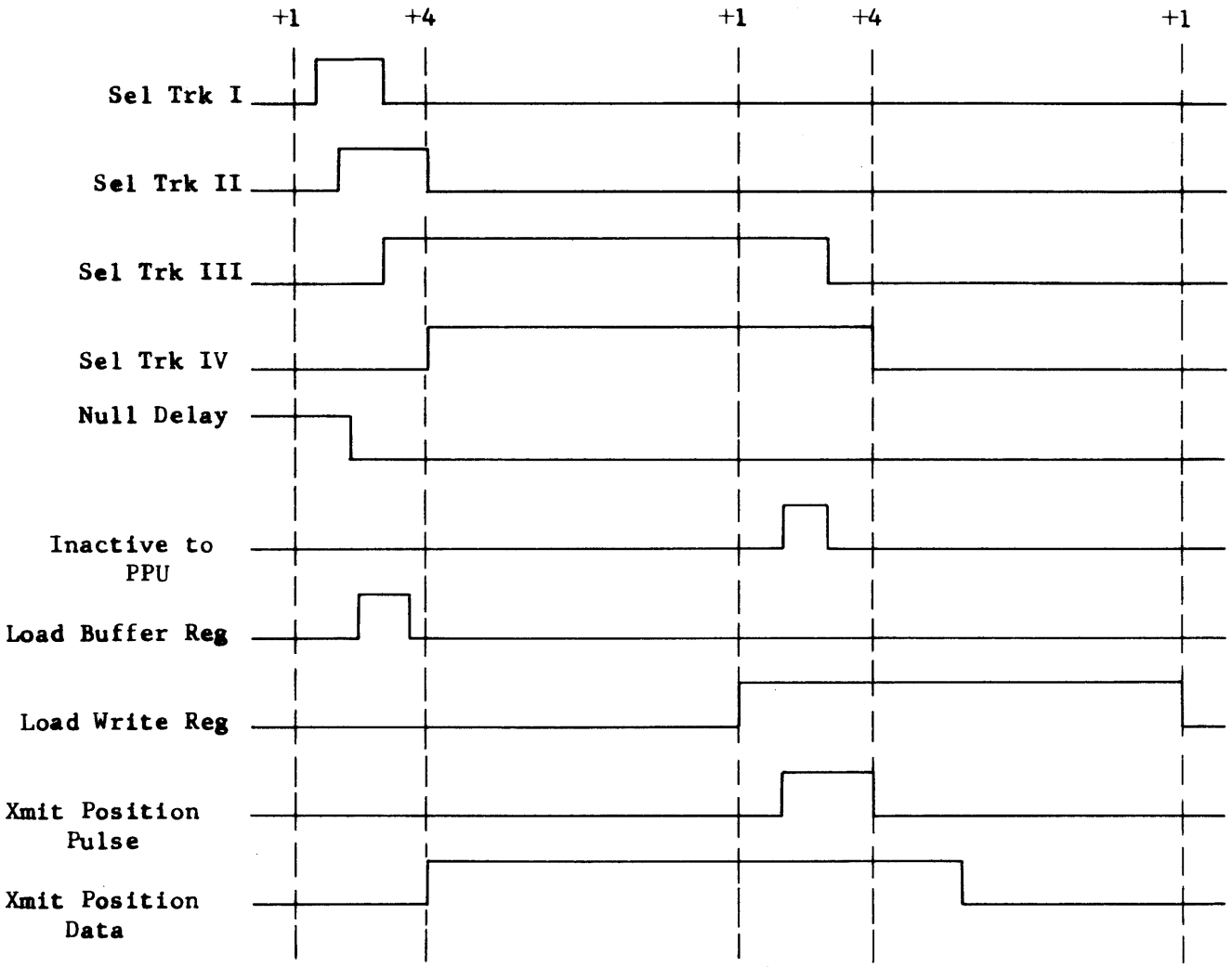


Figure 2-7. Position Select Timing

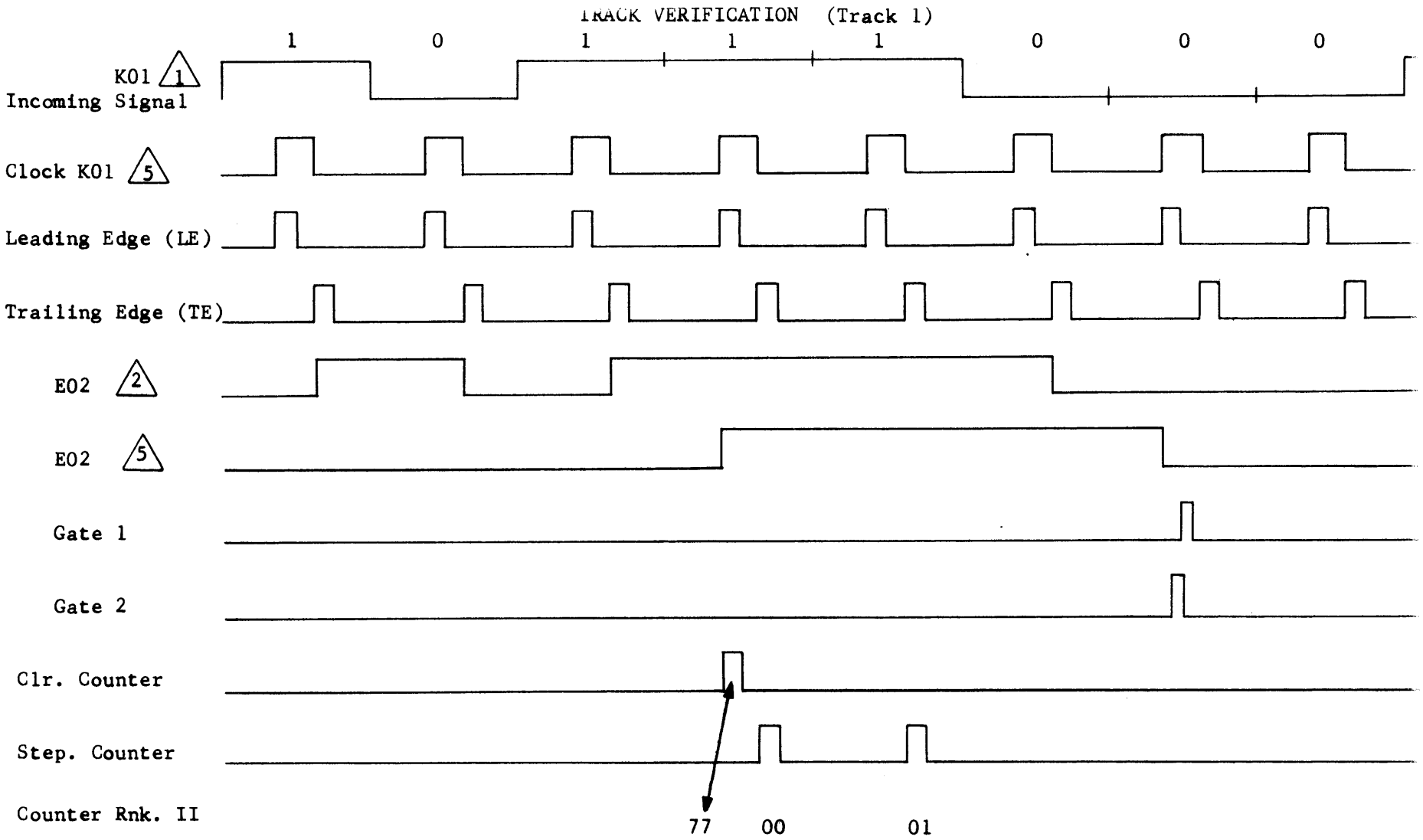
The Verify head picks up a coded signal representing the current track at that location. The code consists of a series of ones followed by a series of zeros repeated every 64 bits as shown in the following table.

Position 0	010101100101010101010
Position 1	010101110001010101010
Position 2	010101111001010101010
Position 12	010101111111111111111001010

The 6639 receives the Verify data and a verify clock generated by the 0/1 pattern which is used for a counter. The counter is started by a series of two ones and terminated by two zeros so that for position 1, the counter would equal 1, etc. (See Figure 2-8) Track verification exists when the output of the counter is equal to the selection made by the function plus an additional ON POINT signal which the disk servo system generates when the system nulls. Two consecutive counter-code compares are necessary to produce verification due to a laping problem at the starting and stopping point when the verify tracks are written. Likewise 2 consective non-verifies will constitute a position error.

WRITE DATA

After previously establishing a head group and a track, the write function selects a sector and initiates a write operation. Although the disk is laid out for sectors of 500_8 12-bit words, the amount of data written is determined by the program and is only limited to the 4K size of PPU memory.



Need "On Point" and two verifies to set Verify 2 FF

Figure 2-8

The write operation is initiated in the controller as soon as the disk reaches the sector specified, providing the system is ready. The current location of the disk is determined by a sector counter. There must be a sector counter for each stack since they are not on a common shaft. The sector counters use their respective index marks and sector marks from the clock disks (index clears, sector mark advances). The count of the selected counter is beat against the desired sector to develop a sector verify signal which starts the writing by sending a WRITE ENABLE to the file. A cell counter which is controlled by the file clock is cleared at the same time. It is the responsibility of this cell counter to determine when the preamble is completed. - The 2^0 bit of the cell counter is used to write the preamble because it will toggle at a clock rate and therefore write a 0/1 pattern for all twelve bits. Data is written continuously as long as the WRITE ENABLE signal is present and is the WRITE CLOCK DELAYED that causes the data to be in phase or out of phase with the clock. The complement of data is sent from the controller. At the cell count of 80 a double word of ones is written and the first word of data is brought in to the write register. Figure 2-9 shows the timing involved in writing the preamble.

The first data word is caught in a holding register and can be received any time during the writing of the preamble. Receipt of the FULL signal accompanying the data will cause the holding register contents to be transfered to the buffer register and an empty returned, unless the buffer register is already loaded. Once data transfers are underway, they must proceed at a 1.2 usec rate due to the speed at which the disk writes the information.

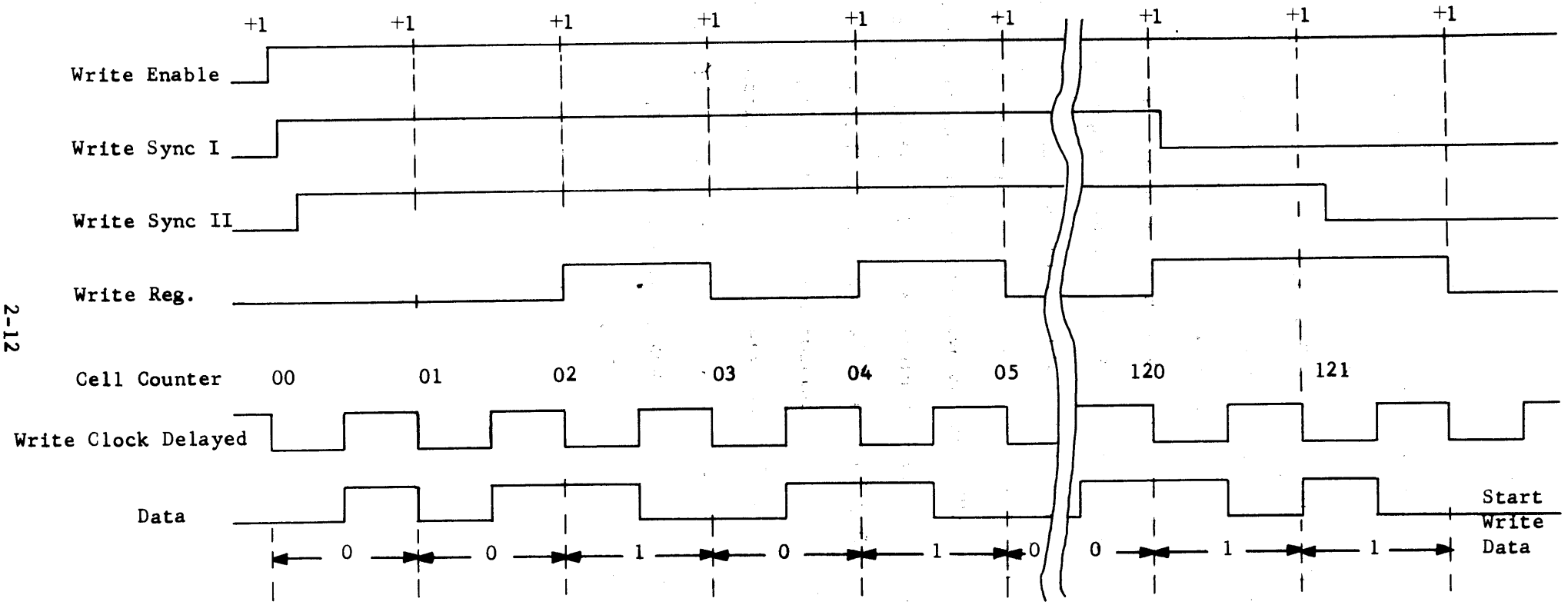


Figure 2-9. Write Preamble Timing

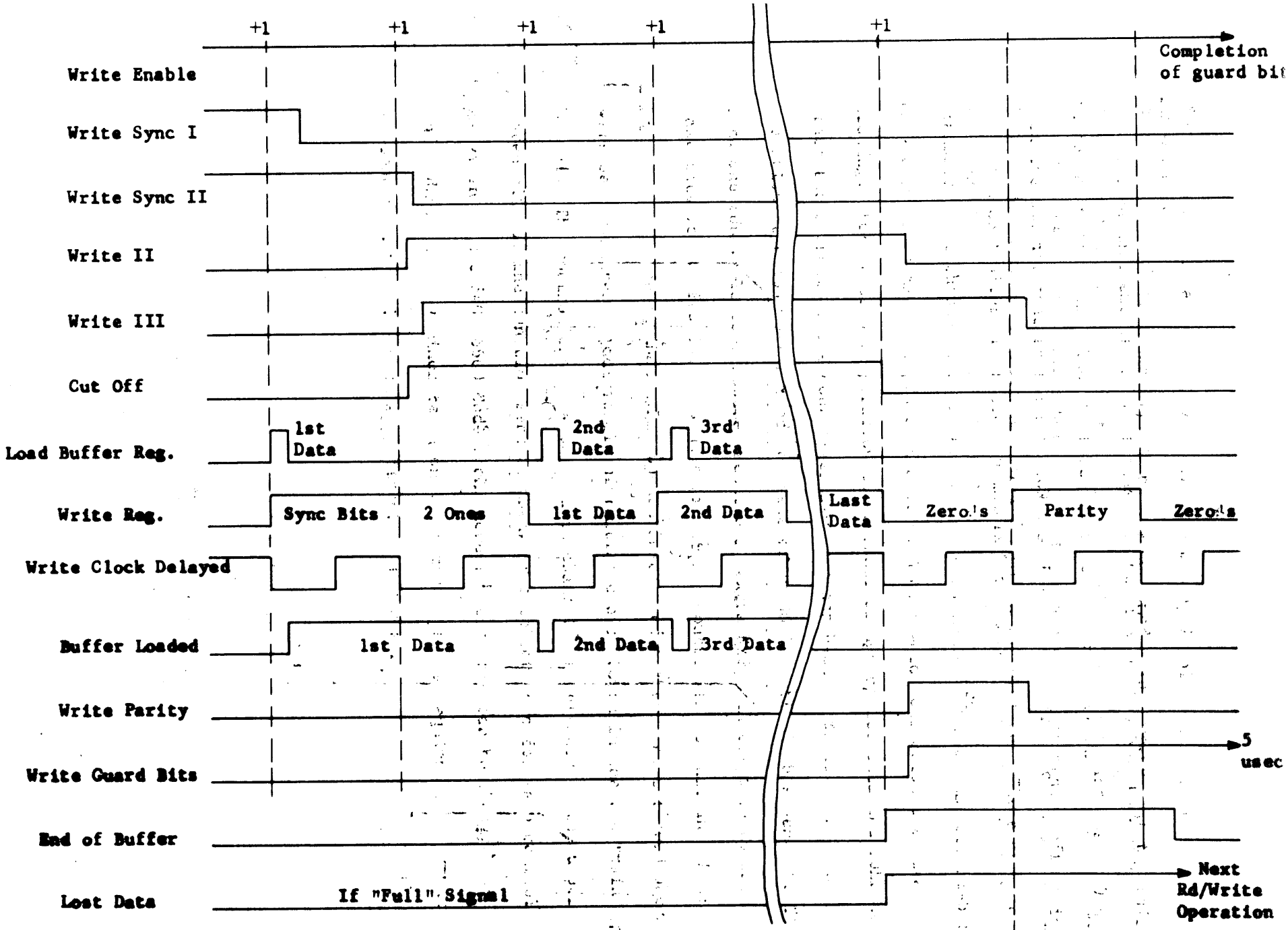


Figure 2-10. Write Data Timing

If new data has not been received when it is time to reload the write register, a Cutoff FF is cleared. Clearing this FF, which was set at the beginning of data writing, will cause the termination of the disk write. See Figure 2-10 for detailed timing. In terminating a write operation a word of zeros is written, then a parity word followed by two words of zeros. A check is made to determine if the termination was due to the program or some unaccountable delay by noting if a FULL came in after termination was begun. If so a Lost Data FF is set to give this status indication.

PARITY GENERATION

The parity word developed during data transfers and eventually written on the disk is a modified form of cyclic coding. Each new input word is checked for equivalence with the current contents and the result left shifted. When the write operation terminates the resultant word is sent to the Write register with the odd bits complimented. Figure 2-11 shows an example of parity word generation for a 2 word transfer.

ON DISK			
1st Word	4102	000 000 000 000	Original Contents
2nd Word	6670	100 001 000 010	1st Word
Guard	0000	011 110 111 101	Equivalence
Parity	0642	111 101 111 010	Left Shift 1
		110 110 111 000	2nd Word
		110 100 111 101	Equivalence
		101 001 111 011	Left Shift 1
		000 000 000 000	Guard
		010 110 000 100	Equivalence
		101 100 001 000	Left Shift 1
		000 110 100 010	To Disk

FIGURE 2-11. WRITE PARITY GENERATION

During the read operation the parity circuits operate in the same maner. The data read from the disk,. including the parity word, develop a check word which should have a 5252 pattern. If the pattern does not exist a parity error status is set up. Figure 12 shows the same data as was written in Figure 2-11 being read. Note that a valid parity check can only be made if the exact number of words written are read.

FROM DISK			
1st Word	4102	000 000 000 000	Original Contents
2nd Word	6670	100 001 000 010	1st Word
Guard	0000	011 110 111 101	Equivalence
Parity	0642	111 101 111 010	Left Shift 1
		110 110 111 000	2nd Word
		110 100 111 101	Equivalence
		101 001 111 011	Left Shift 1
		000 000 000 000	Guard
		010 110 000 100	Equivalence
		101 100 001 000	Left Shift 1
		000 110 100 010	Parity
		010 101 010 101	Equivalence
		101 010 101 010	Left Shift 1

FIGURE 2-12. READ PARITY GENERATION

READ DATA

The read function, like the write, specifies a sector, and the operation is initiated by identifing this sector as it comes under the heads. The cell counter is started when the sector is verified so that the controller can be gated at the count of 70 to look for the double ones signifying the beginning of data. When the sync is received the data transfer begins by setting Read III FF. If, through malfunction, the double ones is not detected a forced read is initiated at a cell count of 112 and a parity error is set. This prevents a hang up of the channel. See Figure 2-13 for read timing.

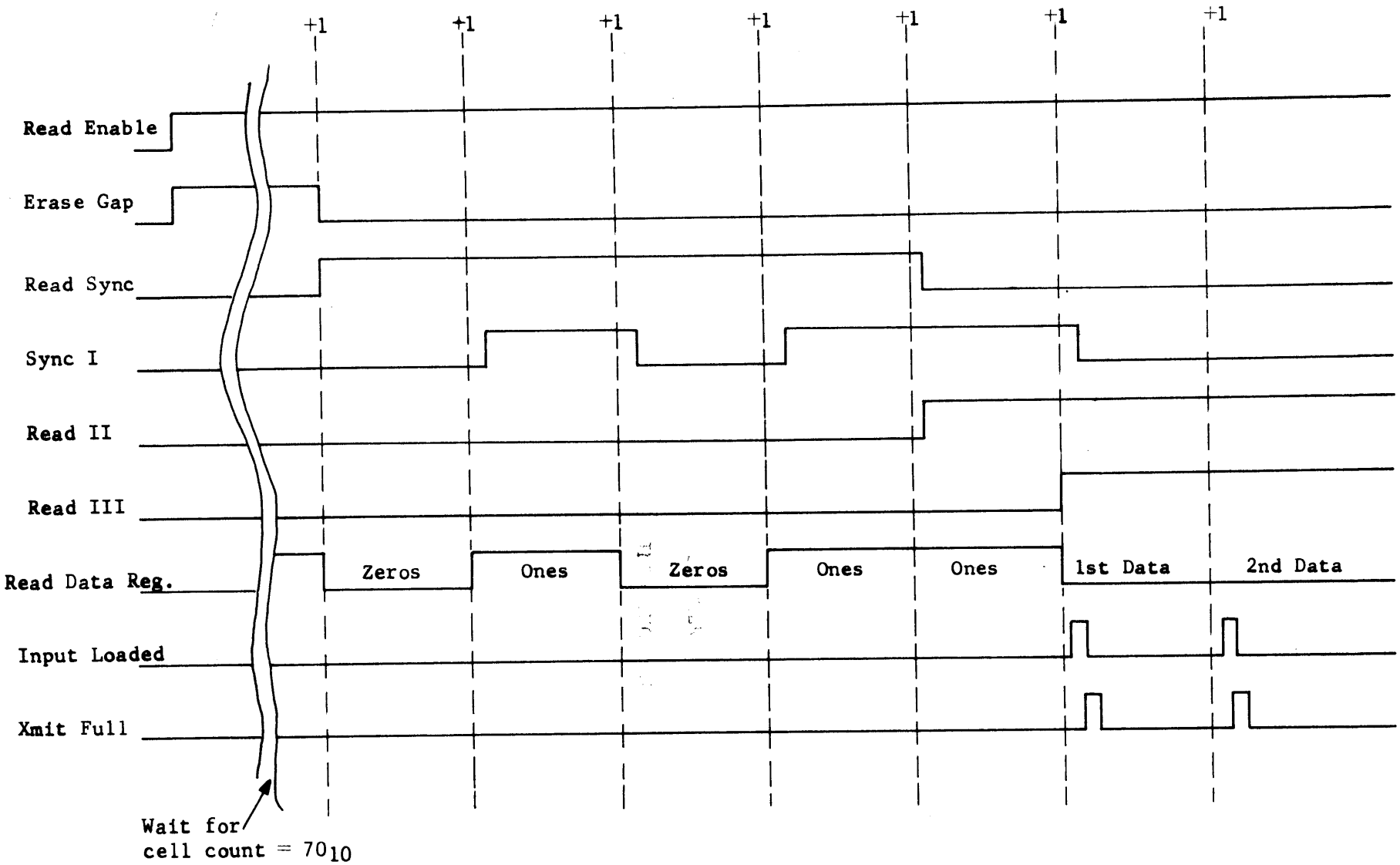


Figure 2-13. Read Timing, Begin Data Xfer

It is a characteristic of the data channel to respond with an EMPTY at the end of the last data word even though it desires no more information. At this time the word of zeros before the parity word would be sent with a FULL signal, however nothing should happen in the channel. If another EMPTY was received, the Lost Data FF would set giving a status indication that the channel did not accept all the data sent by the disk. Figure 2-14 shows the timing on the completion of the read.

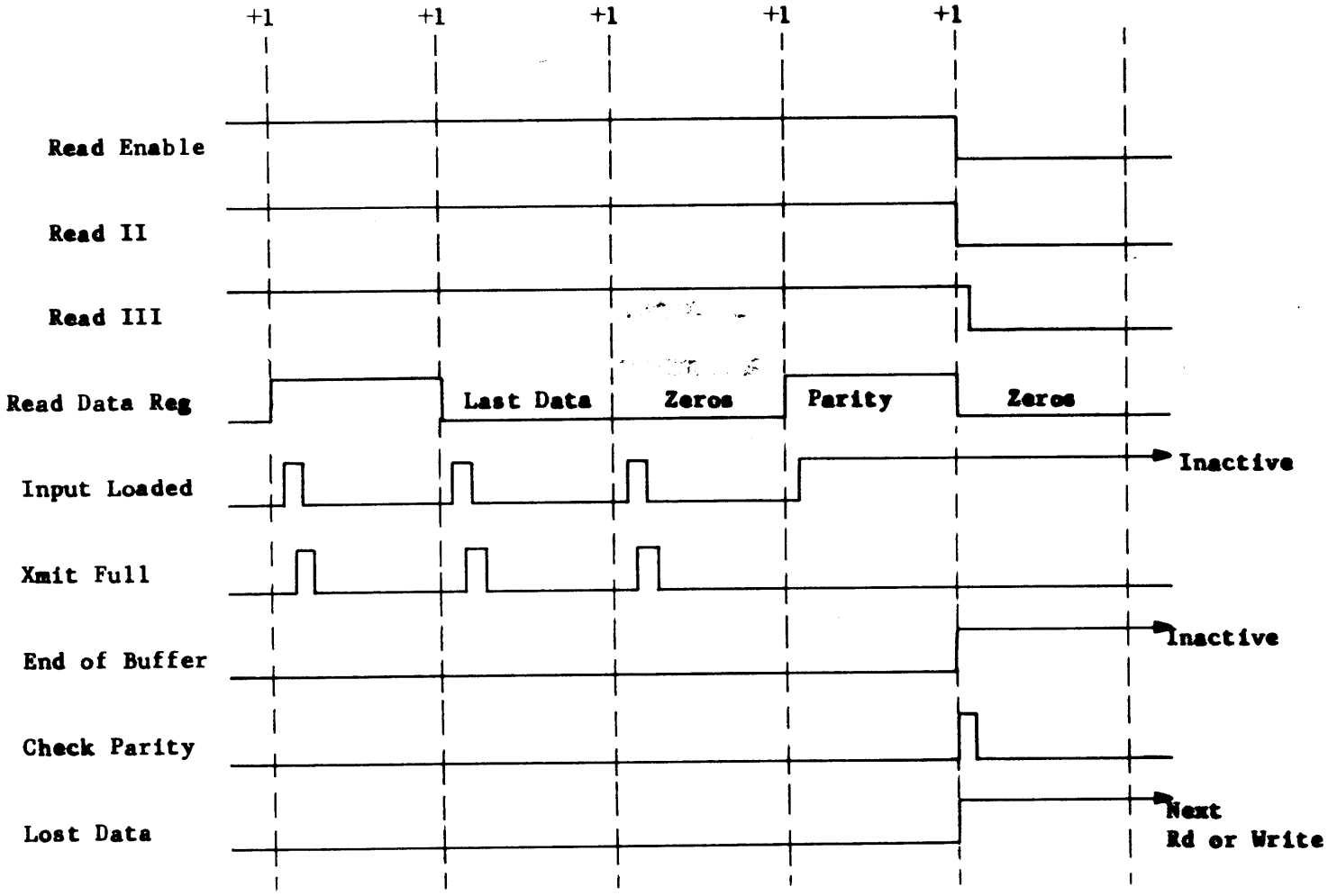


Figure 2-14.

CONTROL DATA INSTITUTES

3255 Hennepin Avenue So.
MINNEAPOLIS, MINNESOTA
55408

5630 Arbor Vitae Street
LOS ANGELES, CALIFORNIA
90045

3717 Columbia Pike
ARLINGTON, VIRGINIA
22204

c/o New School for
Social Research Building
66 West 12th Street
NEW YORK, NEW YORK
10011

60 Hickory Drive
Bear Hill Industrial Park
WALTHAM, MASSACHUSETTS
02154

Exchange Park Garden Mall
DALLAS, TEXAS
75235

Bockenheimer Landstr. 10
6000 FRANKFURT/M.
GERMAN FEDERAL REPUBLIC

CONTROL DATA
CORPORATION