PARALLEL INPUT/OUTPUT
DIRECT MEMORY ACCESS

CGC 7900 SERIES
COLOR GRAPHIC COMPUTERS

CHROMATICS

CGC 7900 COLOR GRAPHICS COMPUTER SYSTEM

Parallel Input/Output
Direct Memory Access Interface
(PIO/DMA) User's Manual

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Chapter 1 -- Introduction

This is the User's Manual for the CGC 7900 Parallel Input/Output, Direct Memory Access circuit board (PIO/DMA).

1.1. Manual Organization

This manual covers the following topics:

Section 1 covers general concepts of the PIO/DMA board, and describes the terms to be used.

Section 2 covers installation and configuration procedures.

Section 3 and **Section 4** cover the functional and electrical aspects of the Parallel Input/Output hardware.

Section 5 and **Section 6** cover the DMA hardware.

Appendix A explains how to program the PIO/DMA board.

Appendices B through D cover the Long Line DMA Interface option.

1.2. PIO/DMA General Hardware

The CGC 7900 PIO/DMA card occupies one slot in the 7900 card cage. The circuit board has five connectors along the outside edge: two for the PIO interface, two for the DMA interface and one for Interrupt and Bus Grant Level Prioritizing. See Figure 1-1 for a layout of the board.

The PIO/DMA board makes available four separate 16-bit parallel ports. Two are programmable ports over which the user has full control; the other two are DMA ports which perform all transfers independent of the CPU when activated. The 7900 can hold up to 10 PIO/DMA boards. See Figure 1-2 for a block diagram of the ports and registers.

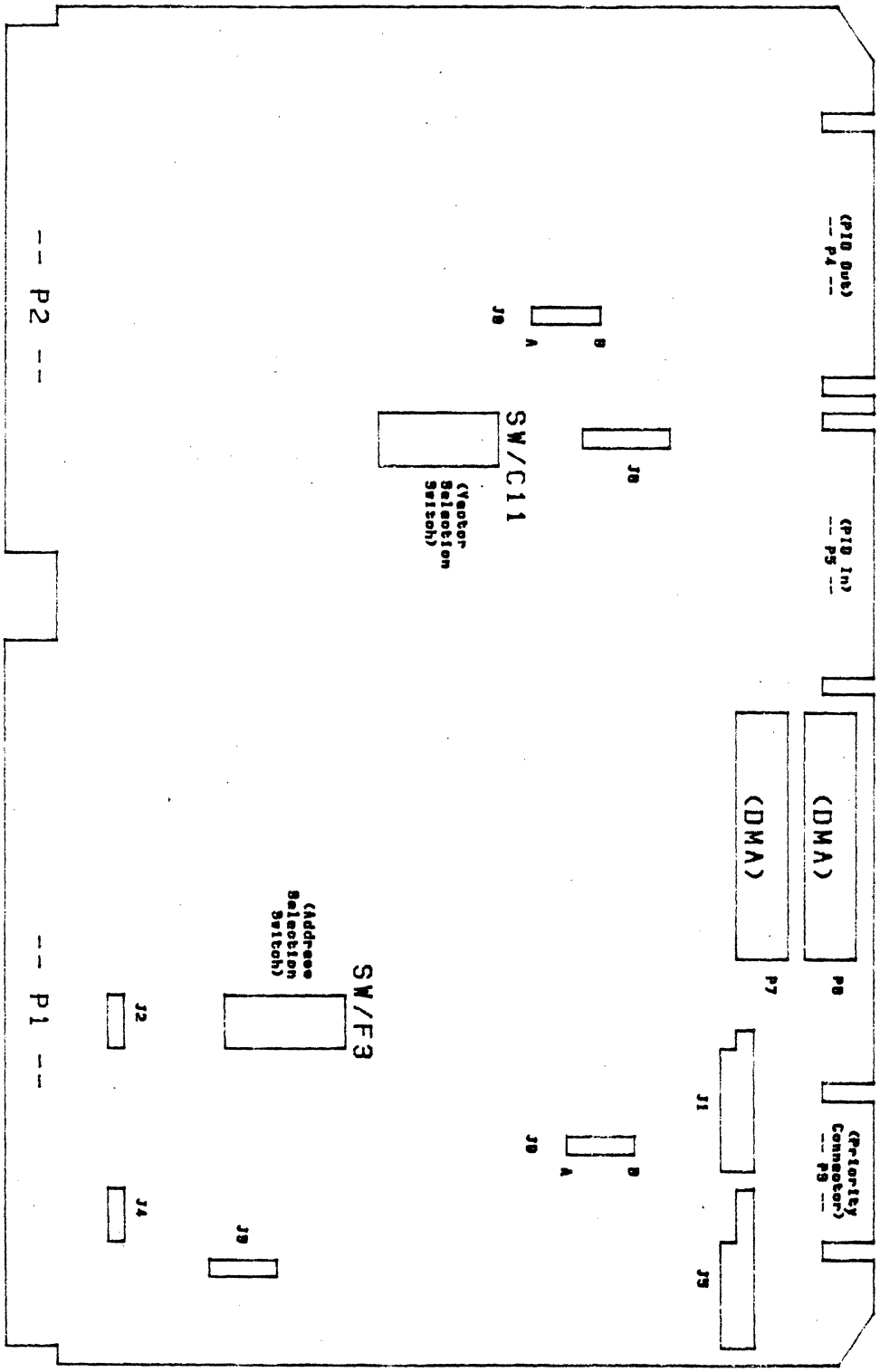


Figure 1-1. PIO/DMA Board Layout

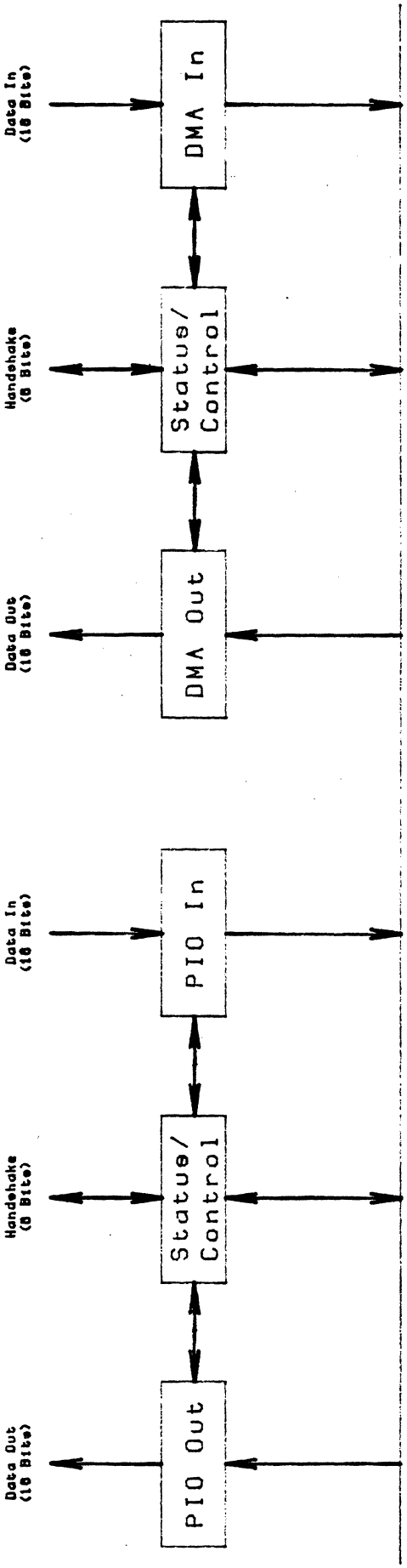


Figure 1-2. PIO/DMA Functional Diagram

1.3. PIO General Description

The programmable ports can be configured for either polled or interrupt-driven operation.

In polled operation, the CPU tests the PIO status register to determine when a port is ready to communicate. This can be done with a two-instruction sequence, known as a "polling loop."

Example:

```
Wait    BTST.B  #2,PIOSTAT     Do we have some data?
        BNE.S   Wait           Not yet, continue polling.
```

When the polling loop indicates the port is ready to go, it will leave the loop and the program will continue reading or writing data to the port.

The second mode of operation is interrupt-driven I/O. When the board has a data word or byte for the CPU (or is ready to transfer another word or byte out the port), it notifies the CPU via an interrupt. This forces the CPU to pause and execute a user-written routine to service the parallel port.

The Parallel Port consists of two 16-bit data registers, one for input and the other for output. Each of these two ports can be subdivided into two 8-bit ports, each with its own status, interrupt, and control circuitry.

The main features of the Parallel Port are:

1) Two 16 bit ports; one for input, one for output. Each port has its own control signals.

2) Word or byte transfers.

3) CPU interaction by polling or interrupts.

4) All receivers and drivers are differential according to RS-422 and RS-423 standards.

5) Transfer rates of up to 150K words or bytes per second.

1.4. DMA General Description

DMA (Direct Memory Access) is a method to transfer blocks of data between memory and a peripheral device. DMA makes these transfers without CPU intervention. Since this scheme eliminates the overhead of CPU polling or CPU interrupts on each data transfer, the DMA process is considerably faster than a similar transfer under direct program control.

The DMA interface is compatible with three DEC DMA interfaces: the DRV11-B, DR11-W and DR11-B. The main features of the DMA interface are:

1) Two 16 bit ports, one for input and one for output.

2) Data transfers up to 500K words per second.

3) Separate 40 pin connectors for input and output.

4) Transfer of up to 64K words at once without processor intervention.

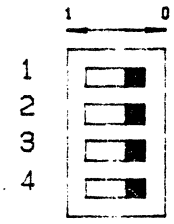
5) Capable of Burst or Single Cycle operation.

Chapter 2 -- Installation and Configuration

This section describes installation procedures and certain hardware options that are applicable to both PIO and DMA portions of the board. Options which apply strictly to either the PIO or DMA hardware will be discussed in the appropriate sections of this manual.

2.1. Memory Address Selection

If you need more than one PIO/DMA board in your system, you must set the base address differently for each board. This is to avoid conficts between the registers on different boards. A switch located at UF3 on the board determines the starting base address of all the registers. They can be relocated in memory between FF8400 and FF84F0. See Table 2-1 for switch setting versus memory address information.



SW/F3

Base Address	Switches 1	2	3	4
FF8400	Ø	Ø	Ø	Ø
FF8410	1	Ø	Ø	Ø
FF8420	Ø	1	Ø	Ø
FF8430	1	1	Ø	Ø
FF8440	Ø	Ø	1	Ø
FF8460	Ø	1	1	Ø
FF8470	1	1	1	Ø
FF8480	Ø	Ø	Ø	1
FF8490	1	Ø	Ø	1
FF84A0	Ø	1	Ø	1
FF84B0	1	1	Ø	1
FF84C0	Ø	Ø	1	1
FF84D0	1	Ø	1	1
FF84E0	Ø	1	1	1
FF84F0	1	1	1	1

Base Address Switch Postions
Table 2-1.

NOTE:

All Chromatics software that requires the PIO/DMA board assumes that there is a board set to base address FF8400. Other boards may be set as desired by the user.

DO NOT set more than one board to the same base address -- the results are unpredictable.

2.2. Interrupt Level Selection

If the interrupt capability on the board is to be used, the two interrupt level jumpers must be installed. These jumpers select the interrupt level for all the interrupts on the board.

The available interrupt levels are levels 1, 2, 3 and 6. Levels 4 and 5 are reserved for the CPU board; level 7 is reserved for the power up interrupt. Jumpers J2 and J3 are the interrupt level jumpers. The jumpers must be set to the same interrupt level. Thus, if J2 has a jumper in position 2, J3 must also have a jumper in position 2. Each header must have only one jumper installed. To complete interrupt acknowledge decoding, there must also be a jumper installed on header J1 at position IN0. See section 2.5, "Multi PIO/DMA Board Systems," if more than one board is to be installed at the same interrupt level.

2.3. Vector Address Selection

The interrupt vector addresses of all the interrupts on the board are switch selectable. They can be relocated between addresses 200 and 3E0. There are seven possible ways to generate an interrupt on the PIO/DMA card. The switch used to select the vector addresses is located at position UC11. See Table 2-2 for vector address selection.

The interrupt vectors are defined as follows (assuming a base address of 200):

200 NOT USED BY PIO/DMA BOARD

204 Ready to Read Word

208 Ready to Read High Byte

20C Ready to Read Low Byte

210 Ready to Write Word

214 Ready to Write High Byte

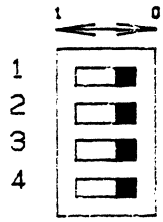
218 Ready to Write Low Byte

21C DMA Done

For more information on interrupt handling, see the 68000 Reference Manual.

2.4. Bus Grant Selection

The level of bus master control granted to each PIO/DMA board is selectable by jumpers located at J4 and J5. If there is only one board in the system. there must be one jumper installed in both J4 and J5 headers and they must agree with each other. Thus, if bus master level three is desired, J4 must have a jumper at 3 and J5 must have a jumper at 3 in the four leftmost positions. See section 2.5. "Multi-PIO/DMA Board Systems," if more than one board is to share the same Bus Master level.



SW/C11

Base Address	Switches 1	2	3	4
200	0	0	0	0
220	1	0	0	0
240	0	1	0	0
260	1	1	0	0
280	0	0	1	0
2A0	1	0	1	0
2C0	0	1	1	0
2E0	1	1	1	0
300	0	0	0	1
320	1	0	0	1
340	0	1	0	1
360	1	1	0	1
380	0	0	1	1
3A0	1	0	1	1
3C0	0	1	1	1
3E0	1	1	1	1

Base Interrupt Vector Switch Positions
Table 2-2.

2.5. Multi-PIO/DMA Board Systems

This section describes how more than one PIO/DMA board can be used in one system.

If you wish to have two PIO/DMA boards share the same interrupt level or bus grant level, obtain the Priority Cable and install it between the two boards at position P3. This cable is a 26-pin card edge to card edge cable available from Chromatics (P/N 060027).

2.5.1. Interrupt Expansion

The interrupt priority jumpers must be positioned properly on both boards. The board which is to have the highest priority within the level must have jumpers at positions IN 0 and OUT 1 on J1. The next board in the chain must have jumpers at positions IN 1 and OUT 2, and so on down the line. Up to 10 PIO/DMA boards may share the same interrupt level.

2.5.2. Bus Master Expansion

Bus Master Expansion works in much the same manner that Interrupt Expansion does. The board which is to have the highest priority within the bus grant level must have jumpers at positions IN 2 and OUT 1 on J5. The next board in the chain will have jumpers at positions IN 3 and OUT 2, and so on. This sequence will continue up to the last board in the chain.

All boards in the same level must have the jumper at J4 in the same position, indicating a shared level. Thus, any board in the chain can request the bus from the CPU. The first board in the chain will receive the bus grant signal from the processor; if it does not want the bus at the present time, it will send the signal out to the next board and so on down the chain.

NOTE:

Make sure there are no conflicts in the switch settings for either the memory or vector addresses.

2.6. PIO Receiver Configurations

The PIO inputs can be configured in three possible ways. See section 4.3, "PIO Optioning," for details.

Chapter 3 -- PIO Theory of Operation

This section of the manual describes how the PIO portion of the PIO/DMA board operates.

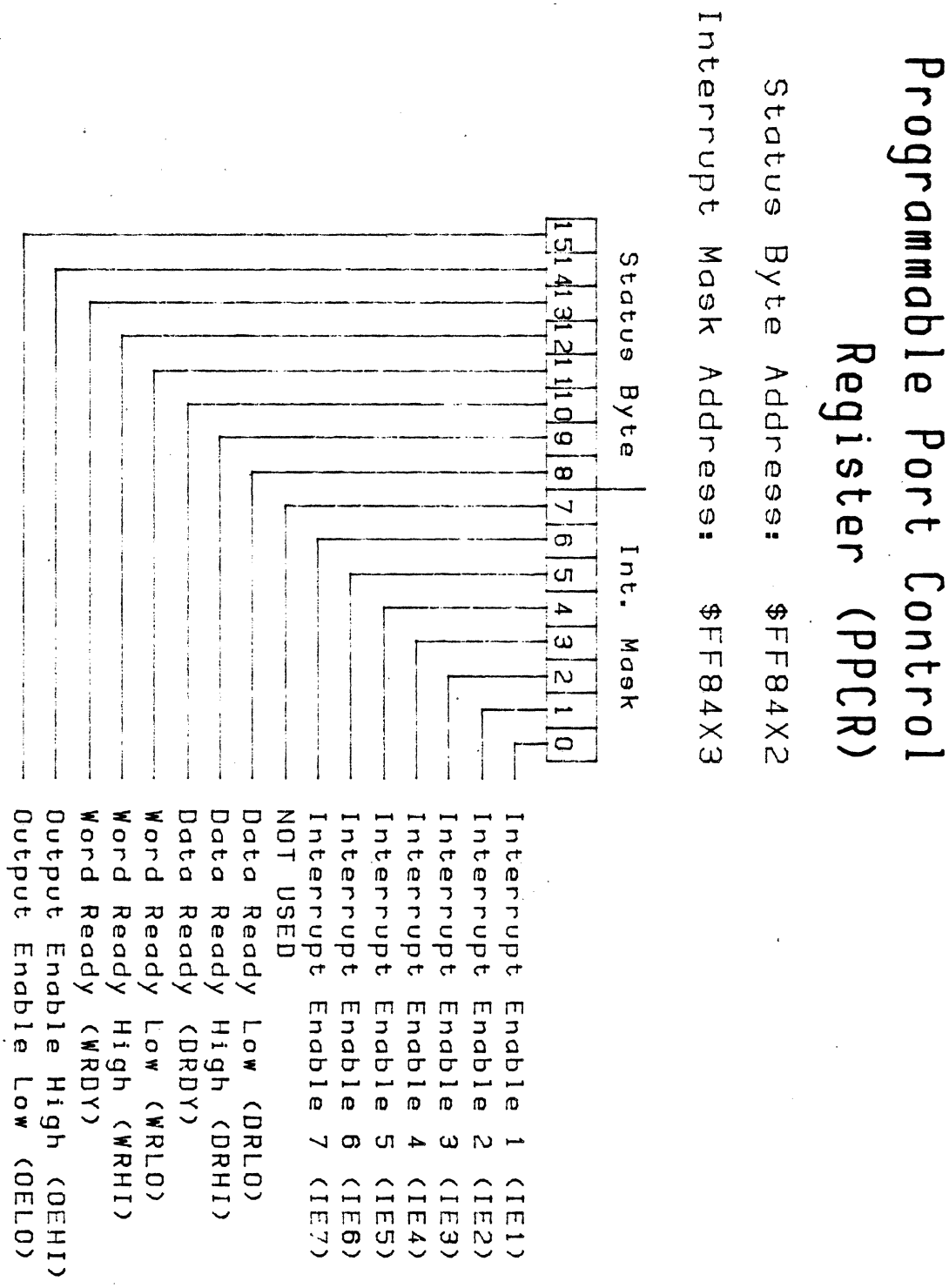
3.1. Programmable Port Control Registers

The programmable parallel port consists of one 16 bit control register and two 16 bit data registers. The addresses of these registers are as follows:

FF84X0 high data byte read or write address
FF84X1 low data byte read or write address
FF84X2 Parallel Port Status byte (See Figure 3-1)
FF84X3 Parallel Port Interrupt mask (See Figure 3-1)

X is selected by address switch; see section 2.1

Figure 3-1 on the next page is a definition of the Parallel Port Control Register. Following the figure is the definition of each bit.



Programmable Control Register Definition
Figure 3-1.

The Interrupt Enable bits located in the low byte of the control word are used to enable any one of seven interrupts and are defined as follows:

IE1 Enables interrupts to occur when the present DMA transfer is complete. This indicates to the CPU that the interface must now be reprogrammed in order to perform another transfer. (0=Interrupt Enabled, 1=Interrupt Masked)

IE2 Enables interrupts on the low byte of the out-going data. This interrupt indicates to the CPU that more data can now be sent out to this byte of the port. (0=Interrupt Enabled, 1=Interrupt Masked)

IE3 Enables interrupts on the high byte of the out-going data. This interrupt indicates to the CPU that more data can now be sent out to this byte of the port. (0=Interrupt Enabled, 1=Interrupt Masked)

IE4 Enables interrupts on the entire sixteen bit output. This interrupt indicates to the CPU that the entire word is now ready to transmit more data. (0=Interrupt Enabled, 1=Interrupt Masked)

IE5 Enables interrupts on the low byte of the incoming data. Indicates to the CPU that a byte has been received on input data bits 0-7 and is ready to be read. (0=Interrupt Enabled, 1=Interrupt Masked)

IE6 Enables interrupts on the high byte of the incoming data. Indicates to the CPU that a byte has been received on input data bits 8-15 and is ready to be read. (0=Interrupt Enabled, 1=Interrupt Masked)

IE7 Enables interrupts on the incoming data word, indicates to the CPU that data has been received on input data bits 0-15 and is now ready to be read. (0=Interrupt Enabled, 1=Interrupt Masked).

The PIO Status Register is located in the high byte of the Control Word. These bits are READ ONLY, except where noted, and are assigned as follows:

Data Ready Low Indicates to the CPU that there is data present at the low byte of the input data buffers. (Active=1)

Data Ready High Indicates to the CPU that there is data present at the high byte of the input data buffers.

Data Ready Indicates to the CPU that there is data present at the input word to the data buffers. (Active=1)

Word Ready Low Indicates to the CPU that the data on the low byte of the output data buffers has been transferred and more data can now be written out to it. (Active=1)

Word Ready High Indicates to the CPU that the data on the high byte of the output data buffers has been transferred and more data can now be written out to it. (Active=1)

Word Ready Indicates to the CPU that the entire output word has been transferred and more data can now be written out to it. (Active=1)

OELO This is a READ/WRITE control bit which enables the output data drivers D0-D11, which are otherwise tri-state. (Enable=1)

OEHI This is a READ/WRITE control bit which enables the output data drivers D12-D15, which are otherwise tri-state. (Enable=1)

NOTE:

OELO and **OEHI** must be set HIGH for the output port to work at all.

3.2. Polling Theory of Operation

This portion of the manual will describe how to use the programmable parallel port in polling mode. There are two polling sequences the CPU can use for the programmable port: polling waiting to write and polling waiting to read.

3.2.1. PIO Polling to Write

When the CPU is ready to write out either a word or a byte, the appropriate status bit can be tested. If the bit is active (set to 1), it indicates to the CPU that the previous data has been transferred and more data can now be sent. This operation can continue as long as there is more data to be transmitted or until the device on the other end of the interface stops reading the data being transmitted.

3.2.2. PIO Polling to Read

When the CPU is expecting input data from the parallel port, it may test the appropriate byte or word status bit. If the status bit is found to be active, the CPU may read the byte or word, store it and continue to poll for as long as needed.

All control signals to the interface are manipulated by hardware which is triggered from the CPU reads or writes.

3.3. PIO Write Operations Using Interrupts

There are three types of interrupts which can trigger the CPU to transfer data out to the parallel output port. The first is the write word interrupt. This interrupt occurs when the PIO output hardware has transferred both the high and the low bytes out to the user device and can now accept another word for transmission.

The second type of write interrupt which can occur is the write high byte interrupt. This interrupt occurs when the PIO output hardware has completed the transmission of the data on the high byte of the parallel output latch and can now accept more data to be transmitted out on that byte.

The final type of write interrupt which can occur is the write low byte interrupt. This interrupt occurs when the parallel output hardware has completed the transmission of the data on the low byte of the parallel output port and can now accept more data to be transmitted on that byte. For any of these interrupts, the appropriate interrupt mask bit must be set to zero in the control status word (see section 3.1).

3.4. PIO Read Operations Using Interrupts

Three types of interrupts exist from which the 7900 CPU can receive an interrupt from the parallel input port:

1) **Read Word Interrupt.** This interrupt occurs when all 16 bits of input data have been presented to the parallel port input buffers and is ready to be read by the CPU.

2) **Read High Byte Interrupt.** This interrupt occurs when data has been presented to the high input data buffer of the parallel port and is ready to be read by the CPU.

3) **Read Low Byte Interrupt.** This interrupt occurs when data has been presented to the high byte of the parallel port input buffers and is ready to be read by the CPU.

Chapter 4 -- PIO Hardware Description

4.1. General

Once the CPU has determined that the output port desired is available for transfer, a write operation is performed to the appropriate location in memory. On the trailing low to high transition of the write operation, signal (1), the output data is latched into the output buffers and one of the OUTPUT DATA READY signals (2) are set active as follows:

ODRLO - Output Data Ready Low Byte
ODRHI - Output Data Ready High Byte
ODR - Output Data Ready Word

These signals will remain active until one of the Output Data Acknowledgements, signals (3), are received at the interface as follows:

ODAKLO - Output Data Acknowledge Low Byte
ODAKHI - Output Data Acknowledge High Byte
ODAK - Output Data Acknowledge Word

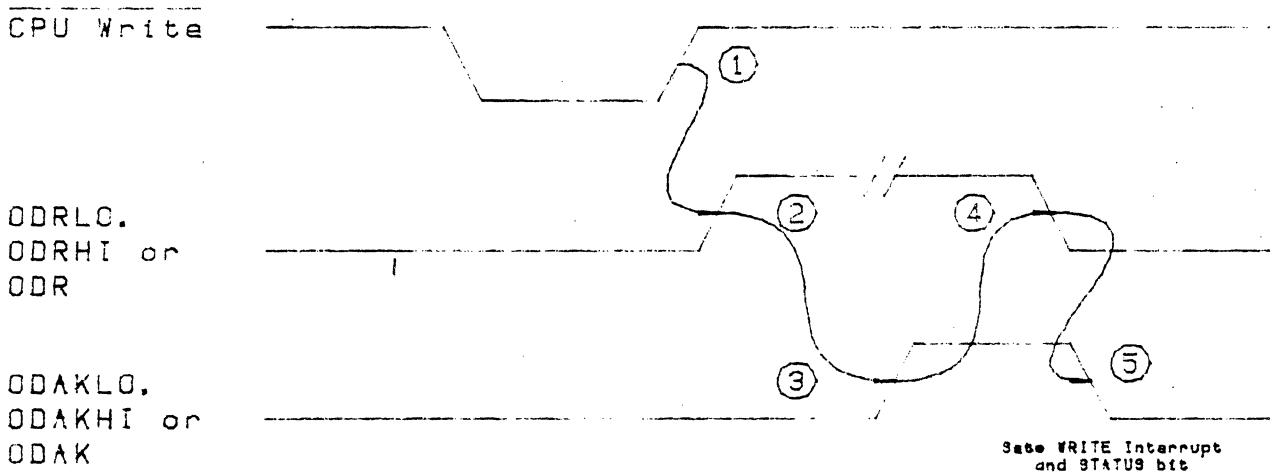


Figure 4-1. PIO Write Timing

Signal (3) causes signal (4), which then causes signal (5). Once the appropriate data acknowledgments, signals (5), go inactive, the status bits will be set to indicate to the CPU that another transfer can now be performed.

4.2. Hardware Theory of Operation

If a user device has data to be input to the CPU, it must first set up the data at the appropriate data inputs. It must then assert the appropriate positive input data ready signal, signal (1), as follows:

IDRLO - Input Data Ready Low Byte
IDRHI - Input Data Ready High Byte
IDR - Input Data Ready Word

These signals as well as the data inputs must remain active until the data has been read by the CPU. On the low to high transition of the CPU READ signal, signal (3), at the input port, the appropriate input data acknowledgement signals (4), will be set active as follows:

IDAKLO - Input Data Acknowledge Low Byte
IDAKHI - Input Data Acknowledge High Byte
IDAK - Input Data Acknowledge Word

Signal timing should be as follows:

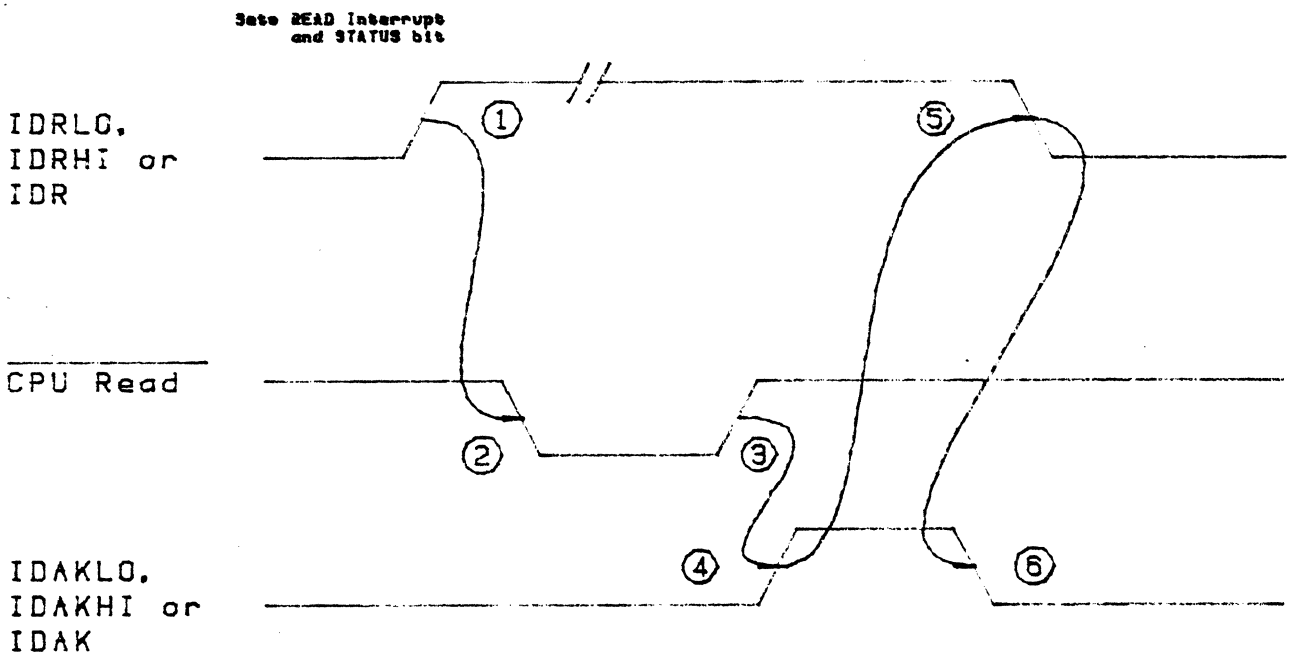


Figure 4-2. PIO Read Timing

4.3. PIO Optioning

There are three configurations under which the PIO receivers can be operated:

1) Straight differential receivers with no bias or terminating resistors.

2) Differential receivers with a shunt terminating resistor across the positive to negative inputs.

3) Single ended receiver with terminating resistors at the minus input holding it at a threshold of approximately 3.0 volts, and a single resistor terminator to ground on the positive input.

To implement each of the three configurations, see Table 4-1 for resistor pack values and locations.

Configuration	A	B	C
R4	-	-	T
R5	-	S	P
R6	-	S	P
R7	-	-	T
R8	-	-	T
R9	-	S	P
R10	-	S	P
R11	-	-	T
R16	-	S	T
R17	-	-	P
R18	-	-	1/4 W 330 ohm *
R19	-	-	1/4 W 470 ohm *
R20	-	-	1/4 W 330 ohm *
R21	-	-	1/4 W 330 ohm *
R23	-	-	1/4 W 470 ohm *
R24	-	-	1/4 W 330 ohm *

PIO Terminator Options
Table 4-1.

* See the note below.

Configuration A is straight differential with no resistors.

Configuration B is straight differential with shunt resistors.

Configuration C is a single ended receiver with 3.0 volt bias at the minus input and a terminator to ground on the positive input.

Resistor S is an 8 pin 220 ohm series resistor pack.

Resistor P is an 8 pin 220 ohm common end resistor pack.

Resistor T is a 10 pin 470 ohm/330 ohm terminating resistor pack.

NOTE:

When configuration B is selected, a 1/4 watt 220 ohm resistor must be installed between the signal ends of R18 and R19, and R23 and R24.

Below are three schematic representations of each of the available configurations which can exist on the input to the PIO card.

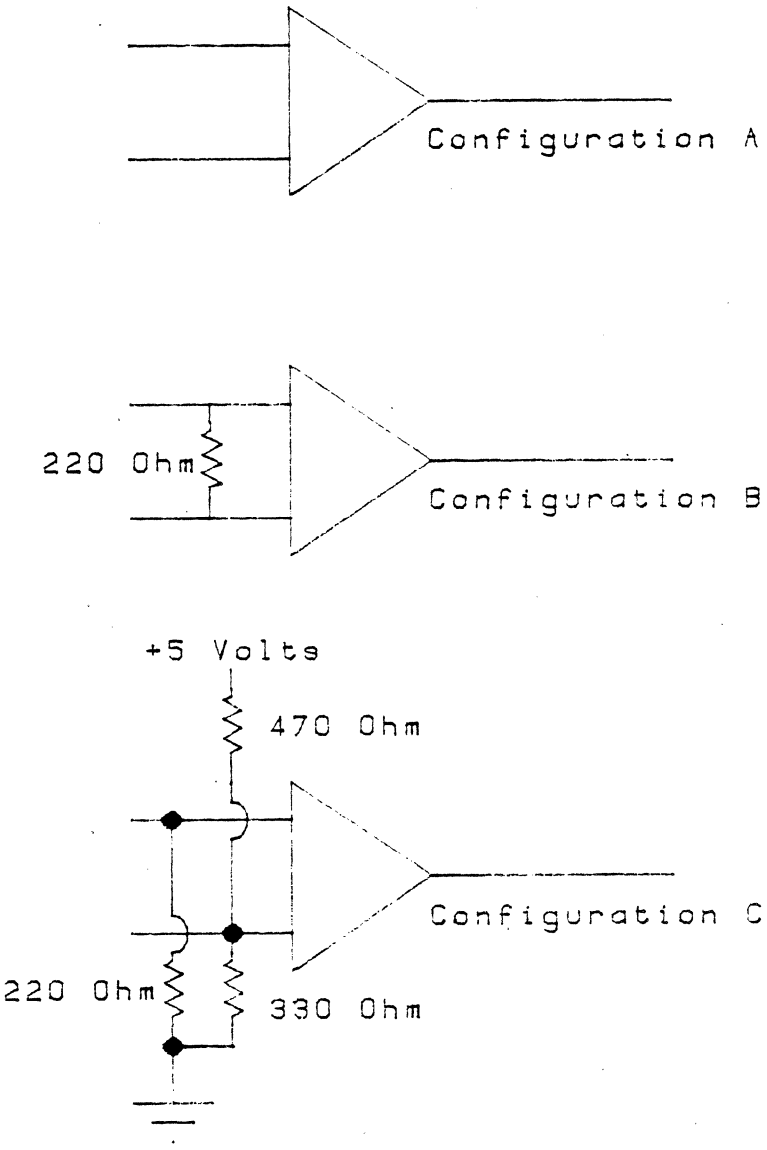


Figure 4-3. PIO Terminator Configurations

4.4. PIO Input/Output Optioning

On the P4 connector of the PIO port, there are 16 data outputs, three output control lines, three input control lines, three ground connections, and three connections for +5 volts. These signals are all that are needed for the parallel port to operate in the mode described in Section 3. "PIO Theory of Operation."

Certain applications, such as a parallel printer interface, require both output and input lines on the same port. The PIO/DMA board allows you to configure the PIO port to have 12 output lines (which would be used for data) and 4 input lines (for status information). Two things must be done to configure the port:

1) Make the upper four bits of the PIO output port tri-state by clearing bit 6 in the PIO control register.

2) Install jumpers at location J6. This routes the lower four bits of the PIO input port to the upper four bits of the PIO output port. Since D12-D15 on the output port are disabled, there is no conflict.

4.5. PIO Connector Definition

The PIO/DMA board has two 50-pin card edge connectors which are to be used strictly for programmed parallel transfers to and from the CPU. The two connectors are designated P4 and P5, P4 being the data output connector and P5 being the data input connector. Below are lists of all the pins available at the connectors, the associated signal name for each pin and a brief description of each is given.

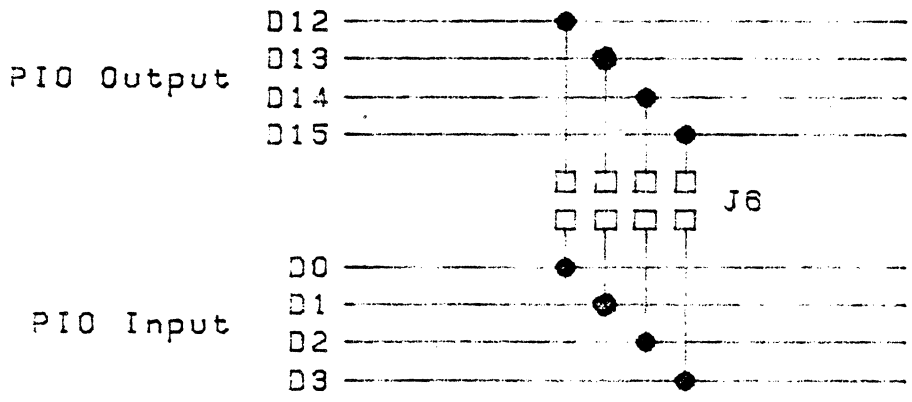


Figure 4-4. PIO Input Rerouting

PIO/DMA P4 Connector Designation

Pin Number		Signal Name	Pin Number		Signal Name
1		DATA OUT 0	26	*	DATA OUT 12
2	*	DATA OUT 0	27		DATA OUT 13
3		DATA OUT 1	28	*	DATA OUT 13
4	*	DATA OUT 1	29		DATA OUT 14
5		DATA OUT 2	30	*	DATA OUT 14
6	*	DATA OUT 2	31		DATA OUT 15
7		DATA OUT 3	32	*	DATA OUT 15
8	*	DATA OUT 3	33		GND
9		DATA OUT 4	34		+5 Volts
10	*	DATA OUT 4	35		GND
11		DATA OUT 5	36		+5 Volts
12	*	DATA OUT 5	37		GND
13		DATA OUT 6	38		+5 Volts
14	*	DATA OUT 6	39		ODRHI
15		DATA OUT 7	40	*	ODRHI
16	*	DATA OUT 7	41		ODRLO
17		DATA OUT 8	42	*	ODRLO
18	*	DATA OUT 8	43		ODR
19		DATA OUT 9	44	*	ODR
20	*	DATA OUT 9	45		ODAKHI
21		DATA OUT 10	46	*	ODAKHI
22	*	DATA OUT 10	47		ODAKLO
23		DATA OUT 11	48	*	ODAKLO
24	*	DATA OUT 11	49		ODAK
25		DATA OUT 12	50	*	ODAK

PIO/DMA P4 Connector Designation
Table 4-2.

* Signal Complement (asserted LOW)

PIO/DMA P5 Connector Designation

Pin Number	Signal Name	Pin Number	Signal Name
1	DATA IN 0	26	* DATA IN 12
2	* DATA IN 0	27	DATA IN 13
3	DATA IN 1	28	* DATA IN 13
4	* DATA IN 1	29	DATA IN 14
5	DATA IN 2	30	* DATA IN 14
6	* DATA IN 2	31	DATA IN 15
7	DATA IN 3	32	* DATA IN 15
8	* DATA IN 3	33	GND
9	DATA IN 4	34	+5 Volts
10	* DATA IN 4	35	GND
11	DATA IN 5	36	+5 Volts
12	* DATA IN 5	37	GND
13	DATA IN 6	38	+5 Volts
14	* DATA IN 6	39	IDRHI
15	DATA IN 7	40	* IDRHI
16	* DATA IN 7	41	IDRLO
17	DATA IN 8	42	* IDRLO
18	* DATA IN 8	43	IDR
19	DATA IN 9	44	* IDR
20	* DATA IN 9	45	IDAKHI
21	DATA IN 10	46	* IDAKHI
22	* DATA IN 10	47	IDAKLO
23	DATA IN 11	48	* IDAKLO
24	* DATA IN 11	49	IDAK
25	DATA IN 12	50	* IDAK

PIO/DMA P5 Connector Designation
Table 4-3.

* Signal Complement (asserted LOW)

Chapter 5 -- DMA Theory of Operation

This section describes how general purpose direct memory transfers are accomplished to and from the CGC 7900.

The DMA portion of the PIO/DMA card has been designed to be compatible with DEC's DR11-W, DRV11-B and DR11-B DMA parallel interfaces. Details concerning the DMA hardware are in Chapter 6, "DMA Hardware Description." This section deals with the overall operation of the interface.

5.1. DMA Transfer Modes

There are two modes in which data can be transferred to or from the DMA interface. These are Burst Mode transfers and Single Cycle Mode transfers. In both modes of operation, the interface is armed by the CPU. The specified transfer size then determines how many transfers will be done without further CPU intervention.

The difference between the two modes lies in how the bus arbitration is handled between the CPU and the DMA board. In Burst Mode, once the interface is armed, the logic on the DMA board will acquire the system bus and not relinquish it until the entire transfer is complete. In Single Cycle Mode, the DMA logic will share the system bus with the processor. It uses every second memory cycle, and the CPU uses the ones in between. In both Burst Mode and Single Cycle Mode, there are two types of data transfers which can be performed:

1) Write Words (7900 to DR11)

2) Read Words (DR11 to 7900)

NOTE:

The DR11-W, DRV11-B and DR11-B interfaces also support read-modify write mode and byte transfers. These two modes are not supported on the CGC DMA board.

How each of these modes are selected and their effects on the system will be discussed in section 5.5.

5.2. DMA Transfers

There are two types of transfers which can be performed to or from a DR11 interface. One is a program controlled transfer, the other is a DMA transfer.

The program controlled transfer is very similar to that of the PIO transfer; i.e., all transfers are performed under control of the CPU. However, the user determines when data is valid and not valid. Data is transferred via the data buffer registers using the STATUS and FUNCTION lines to determine data availability. This section of the manual describes in detail how a DMA transfer operation is performed from the CGC 7900 to a receiving device.

5.3. DMA Register Initialization

Before a DMA transfer is initiated by the CGC 7900, the following registers must be set up:

1) Word Count Register

2) Control Register

3) Bus Address Register

4) Extended Address Register

The write to the Extended Address Register triggers the interface to begin transferring data. Depending on whether the transfer is from CGC 7900 to DR11, or from DR11 to CGC 7900. the DMA logic will perform one of two sequences described in the following section.

5.4. DMA Bus Cycles

5.4.1. 7900 Bus Request Cycle

The DMA control circuitry will drive the selected Bus Request Line low on the CPU control bus and wait for the corresponding Bus Grant Signal from the CPU. Once the CPU has granted the bus and completed its present bus cycle, the DMA control logic will remove its Bus Request and drive the Bus Grant Acknowledge Signal (BGACK) low. The activation of this signal causes the CPU buffers to go tri-state, removing the CPU from the system bus. The BGACK signal causes the CPU to remove its Bus Grant. The CPU is now completely off the bus and the DMA circuitry has full access to the entire system.

5.4.2. 7900 DMA Logic Data Fetch Cycle

When the DMA control logic has taken control of the bus, it immediately enables its output buffers, which contains the address and all control bus information for the desired data. After a period of approximately 70 nanoseconds, the DMA control logic asserts the Address Strobe and the necessary Data Strobes. It then waits for the Data Transfer Acknowledge signal back from the selected memory (DTACK).

When the DTACK signal is received, the DMA logic will wait 200 nanoseconds and then latch the data into data output buffers. It will also remove the Address Strobe and the necessary Data Strobes, remove its address buffers from the bus, increment its word count register and bus address registers and release its hold of the bus by de-asserting BGACK. The CPU will then begin normal execution exactly where it left off before the bus was relinquished to the DMA control logic.

5.4.3. 7900 Cycle Request to the DR11-W, DRV11-B or DR11-B

Once the data has been loaded into the output data buffers and is ready for transfer to the DR11 interface, the DMA control logic will assert CYCLE REQUEST. This will cause the DR11 interface to initiate a bus cycle, and assert the BUSY signal in the 7900 DMA control logic.

The 7900 DMA control logic will then remove its cycle request and wait for the BUSY signal to be de-asserted. The 7900 DMA control logic will then check to see if the transfer is complete. If not, it will continue the transfer by once again requesting the system bus. When the transfer is complete, the DMA logic can interrupt the CPU. The CPU can also poll for a completed transfer by testing the DMA READY bit in the DMA Status Register.

If the transfer is to be from the DR11 interface to the 7900, the 7900 Cycle Request is performed first, acquiring the data to be written into the 7900 memory. The 7900 DMA control logic will then perform a Bus Request Cycle as described above. Once the system bus has been acquired, the sequence in section 5.4.4 will be performed.

5.4.4. 7900 Data Write Operation

Once the system bus has been acquired, the DMA control logic will enable its DMA READY buffers, data buffers, function code buffers and write signal buffer. Approximately 70 nanoseconds later. the Address Strobe and the necessary Data Strobes will be asserted.

When the selected memory responds with DTACK, the DMA logic will wait 200 nanoseconds and then de-assert the Address Strobe and the Data Strobes, as well as remove all other buffers from the data bus. It will finally relinquish the bus by de-asserting BGACK.

See Figures 5-1 and 5-2 for signal relationships.

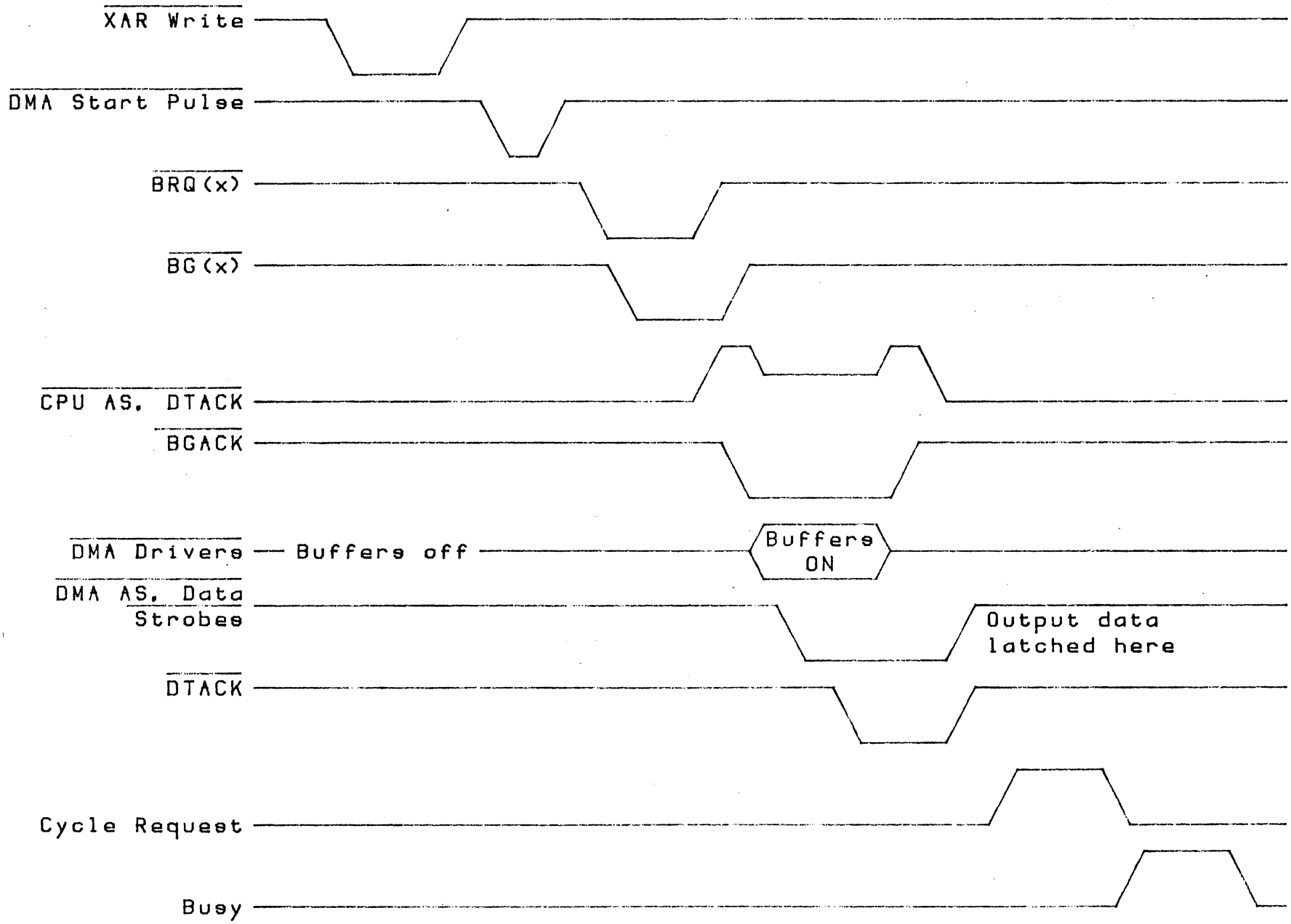


Figure 5-1. CGC to DEC Host Timing

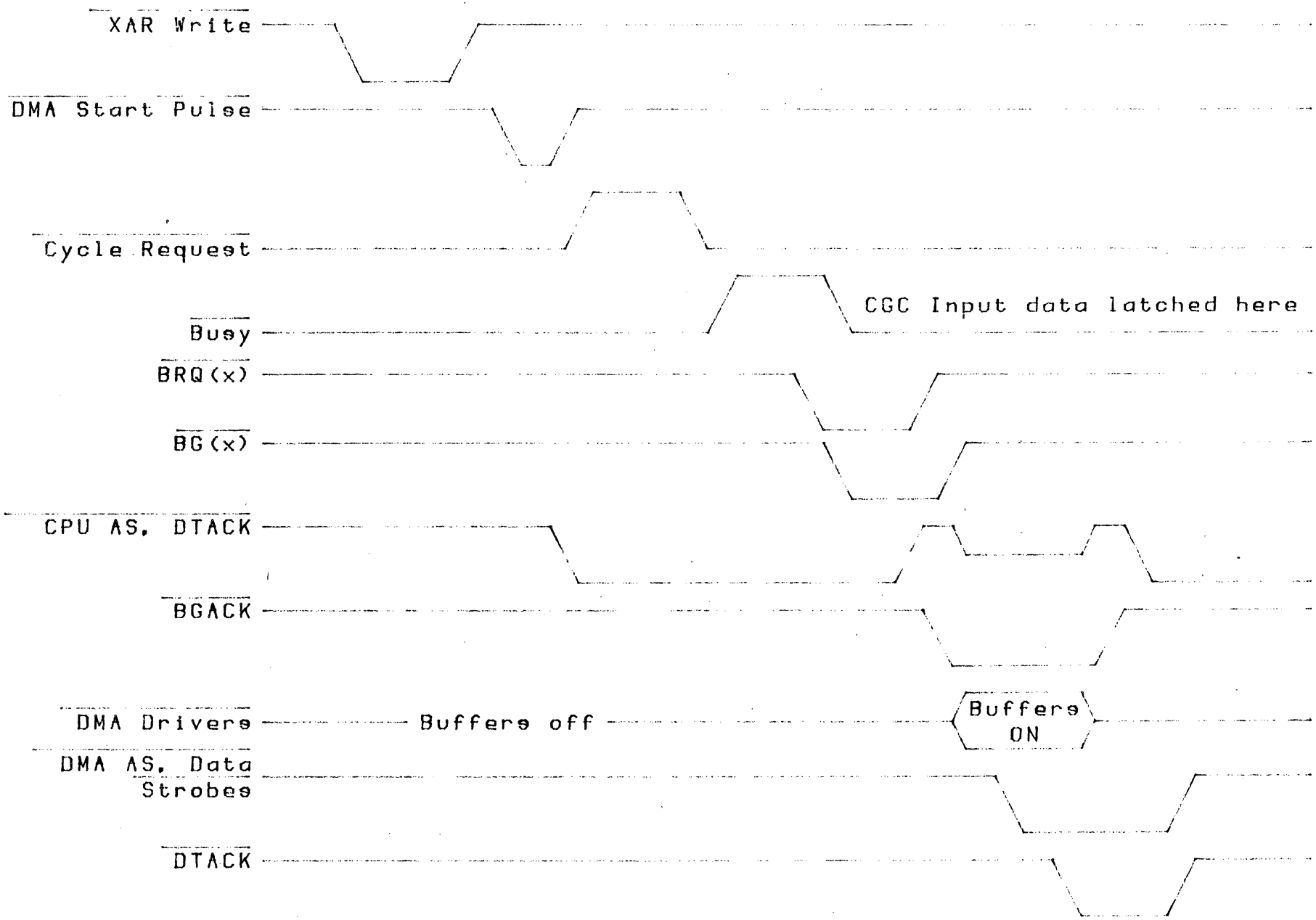


Figure 5-2. DEC Host to CGC Timing

5.5. DMA Register Definition

There are six registers which are used strictly by the DMA portion of the PIO/DMA circuit board. This section of the manual describes how those registers are used.

OUTBUF - This is a 16-bit output data latch which can be written to by the CPU or through the DMA hardware. The CPU can write to this buffer only when the DMA is not active. Once the interface is armed and until the transfer is complete, all transfers to the OUTBUF are under control of the DMA hardware.

INBUF - This is a 16-bit input latch used to receive data from the host device. This buffer can be read either directly by the CPU, or via the DMA hardware. Once the interface is armed and until the transfer is complete, all control of the INBUF is via the DMA hardware.

Bus Address Register(BAR) - This register contains the least significant 16 address bits of the address to be transferred. This is a WRITE ONLY register.

Control Register(CTRLREG) - The Control Register is an 8-bit read/write register which is used to control all details of the transfer to be done. The Control Register and the Extended Address Register combine to make up one 16-bit register. The Control Register takes the least significant byte. (See Figure 7)

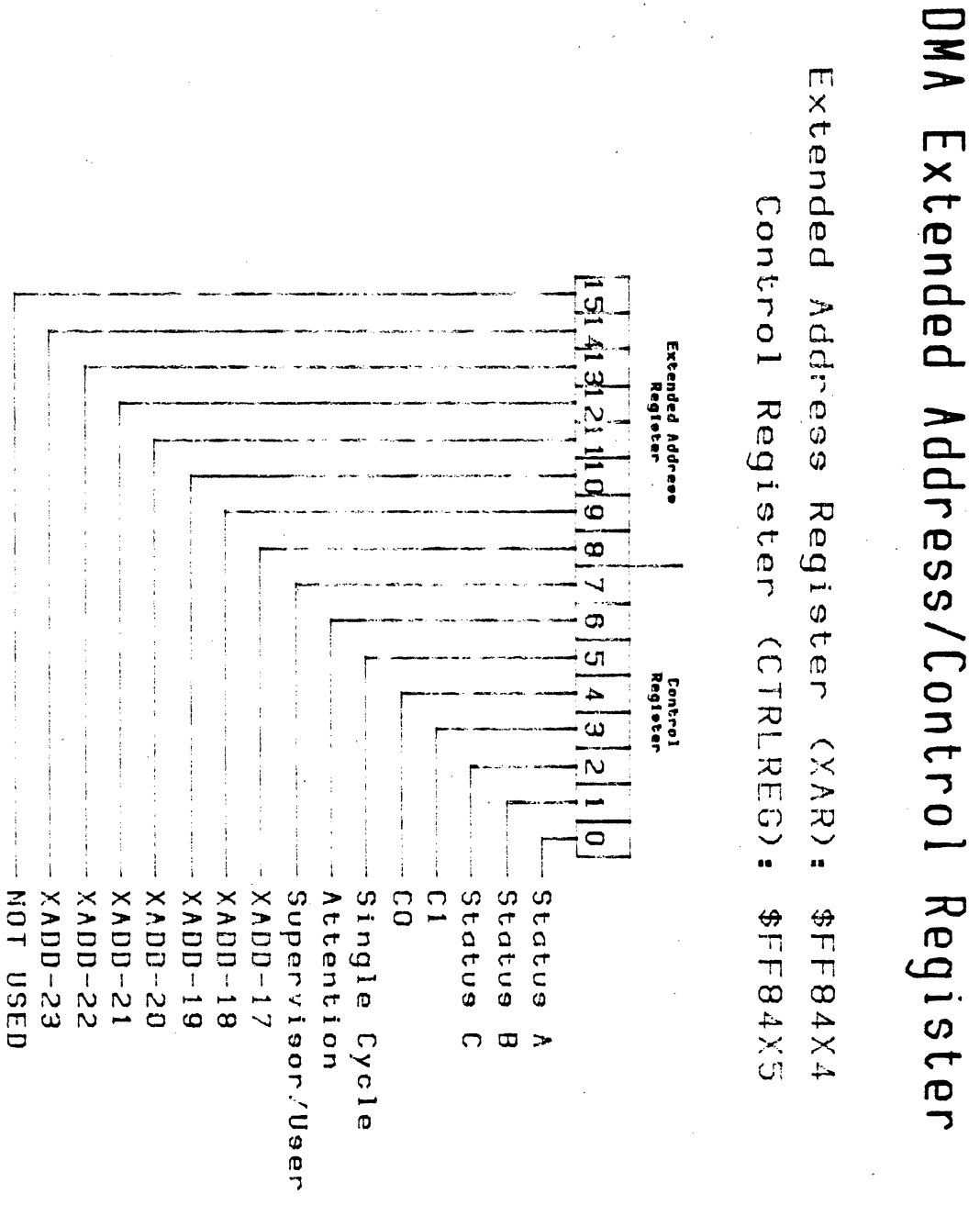
Extended Address Register(XAR) - This is an 8-bit write only register containing the most significant 7 bits of address information. This makes up a 16-bit register when combined with the Control Register. The XAR takes the most significant byte with the highest bit not used. Loading this register triggers the transfer. (See Figure 7)

Word Count Register - This is a write only register which is loaded with the twos complement of the word count to be transferred.

The addresses for all registers pertaining to the DMA portion of the PIO/DMA card are as follows:

FF84X4 Address Bits 17-23 of the DMA address (See Figure 7)
FF84X5 Read Write Control bits pertaining to DMA transfers (See Figure 7)
FF84X6 Bits 8 - 15 of the word count
FF84X7 Bits 0 - 7 of the word count
FF84X8 address bits 1 - 16 of the starting DMA address
FF84XA Read/Write DMA High data word
FF84XD DMA Status byte (See Figure 7)

(X selected by address switch; see section 2.1.)



Extended Address/Control Register Definition
Figure 5-3.

XADD17 through XADD23 - Used to hold the most significant 7 bits of the CGC address to or from which the transfer is to be performed.

Status A, B and C - User defined status bits, used for program controlled transfers to indicate data ready or data received.

C0 and C1 - These two output control signals are used by the DR11 machine to indicate the type of bus cycle to be performed. They are defined as follows:

C0	C1	Bus Cycle
0	0	Word Transfer to CGC
1	0	Not Used
0	1	Word Transfer from CGC
1	1	Not Used

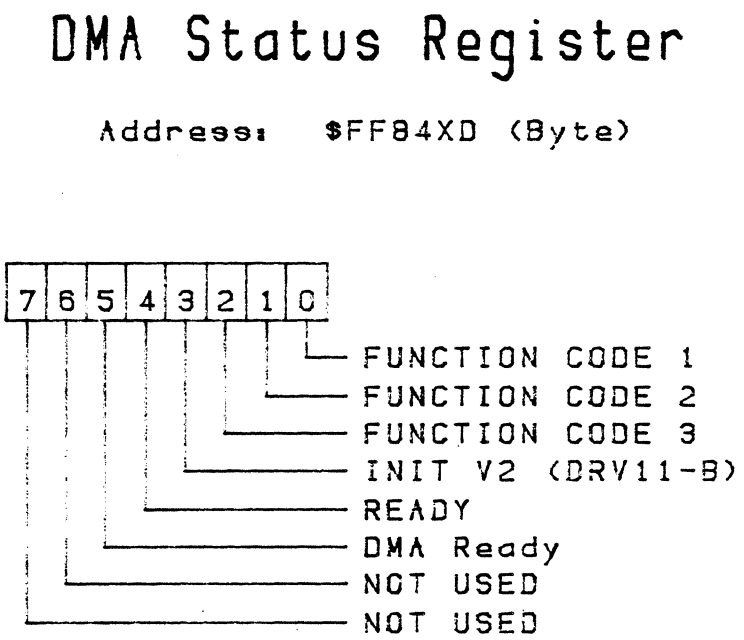
Bus Cycle Definitions
Table 5-1.

Single Cycle - This signal indicates to the DR11 under which bus master mode the transfer is to take place. When this bit is high, the transfer is done one cycle at a time, thus sharing the bus with the CPU. When this bit is low, the transfer is done all at once and the system bus is not relinquished until the transfer is complete.

Attention - Used to notify the PDP-11 that an exception has occurred and the present transfer must be aborted.

Supervisor/User - Used to define the type of memory area in which the CGC transfer is to take place. When it is high, it will be a supervisor data area transfer and when it is low it will be a user data area transfer.

DMA Status Register - The DMA Status Register contains five signals from the interface which are used in determining the state of the interface. These bits are not part of the Control Register and are read only. Below is the definition of the Status Register with a description of each bit following.



DMA Status Register Definition
Figure 5-4.

FUNCTION CODES 1, 2 and 3 - These are status bits which can be used to convey interface information to the 7900. These bits can be set or cleared by the interface.

If FUNCTION CODE 2 is set high by the interface, it will send an interrupt to the 7900. The DMA interrupt enable bit must be cleared in the Interrupt Mask Register for the interrupt to be recognized. This bit will remain active and must be cleared by the user after an acknowledgment has occurred.

INIT V2 - Used for interprocessor communication, it will reflect the state of FUNCTION CODE 2.

READY - Indicates to the CGC that the user device is ready to begin a transfer. (Active = 0)

DMA Ready - This bit when active indicates that the DMA hardware has completed the most recent transfer and is now ready to be initialized for another transfer.

Chapter 6 -- DMA Hardware Description

6.1. General

As was mentioned earlier, there are two 40-pin right angle connectors located on the card edge of the PIO/DMA card which are used strictly for transfers to a host computer. All signals on these connectors are compatible with DEC's DR11-W, DR11-B and DRV11-B DMA interfaces, with a few minor differences which will be discussed here. Connections are made to the DEC computer system via a pair of 40 pin flat ribbon cables.

If a DRV11-B is connected, the cables will connect directly onto the DRV11-B circuit board on the DEC Q-Bus.

If a DR11-B is connected, the cables will connect directly to the CGC 7900 through a DR11-B adapter board supplied by Chromatics (P/N 100428). See Cable Diagrams A and B for these two cable inter-connections.

If a DR11-W is connected, the cables will connect directly into the DR11-W on the UNIBUS. *

* "UNIBUS" is a trademark of Digital Equipment Corporation.

6.2. DMA Connector Definition

P6 Connector Pin	Signal	P7 Connector Pin	Signal
B	CYCLE REQUEST	B	BUSY
D	INIT V2	D	ATTN
F	READY	F	A00
J	WC INC ENB	J	BA INC ENB
K	SINGLE CYCLE	K & L	FNCT 3
L	STATUS A	N	C0
N	INIT	R	FNCT 2
R	STATUS B	T	C1
T & V	STATUS C	V	FNCT 1
LD	08 IN	DD	08 OUT
FF	09 IN	FF	09 OUT
JJ	10 IN	JJ	10 OUT
LL	11 IN	LL	11 OUT
NN	12 IN	NN	12 OUT
RR	13 IN	RR	13 OUT
TT	14 IN	TT	14 OUT
VV	15 IN	VV	15 OUT
CC	07 IN	CC	07 OUT
EE	06 IN	EE	06 OUT
HH	05 IN	HH	05 OUT
KK	04 IN	KK	04 OUT
MM	03 IN	MM	03 OUT
PP	02 IN	PP	02 OUT
SS	01 IN	SS	01 OUT
UU	00 IN	UU	00 OUT

CGC 7900 DMA Connector Pin Outs
Table 6-1.

All signals described in this section of the manual are also described in the associated DEC User Manuals for the DRV11-B, DR11W, and the DR11-B DMA interfaces.

00 OUT - 15 OUT	16 TTL output lines to the interface.
00 IN - 15 IN	16 TTL input lines from the interface.
STATUS A,B,C	Three TTL output lines to the interface. The function of these lines is defined by the user.
FUNCT 1,2,3	Three TTL input lines from the interface. The function of these lines is defined by the user. *
INIT	One TTL input Status line from the interface.
INIT V2 (DRV11-B)	One TTL input line from the interface. Used by DEC machines for inter-processor communication. It can be user defined for CGC 7900 applications.
A00	One TTL output line to the interface. This line is normally for word transfers. During byte transfers, this line controls address bit 00 in the host.
BUSY	One TTL input line from the interface. BUSY is low when the DRV11-B or the DR11-B control logic requests control of the LSI-11 bus or when a DMA cycle is in progress. A low to high transition indicates the end of the cycle. BUSY is high when the DR11-W requests the bus or performs a data transfer. A high to low transition indicates the end of the cycle.
READY	One TTL input line from the interface. When the READY line goes low, DMA transfers may be initiated by the CGC 7900.

C0,C1	Two TTL output lines to the interface. These lines control the type of bus cycle that the DMA hardware logic will execute.
SINGLE CYCLE	One TTL output line to the interface. This line is pulled high on the interface. When it goes low. it indicates that the DMA hardware is in burst mode. This line does not affect the DR11-W interface. #
WC INC ENB	One TTL output line to the interface. When this line is high. Word Counter incrementing is enabled. Low inhibits incrementing.
BA INC ENB	One TTL output line to the interface. When this line is high. incrementing the bus address counter inside the DR11 DMA logic is enabled. A low on this line inhibits incrementing.
CYCLE REQUEST	One TTL output line to the interface. A low to high transition of this line initiates a DMA request.
ATTN	One TTL output line to the interface. This line is driven high to terminate DMA transfers, to set the READY bit and request an interrupt if the interrupt enable bit is set.

* Whenever the DEC computer drives the F2 line high at the CGC interface, it will cause the interrupt bit to be set and the present transfer if there is one to be terminated. This is activated by the level of F2. It is not edge-triggered.

Although the Chromatics DMA hardware can operate in burst mode, it does not work with the DR11-W.

6.3. DMA Connector Pin Assignments

P6 Connector Pin	Signal	P7 Connector Pin	Signal
B	CYCLE REQUEST	B	BUSY
D	INIT V2	D	ATTN
F	READY	F	A00
J	WC INC ENB	J	BA INC ENB
K	SINGLE CYCLE	K & L	FNCT 3
L	STATUS A	N	C0
N	INIT	R	FNCT 2
R	STATUS B	T	C1
T & V	STATUS C	V	FNCT 1
LD	08 IN	DD	08 OUT
FF	09 IN	FF	09 OUT
JJ	10 IN	JJ	10 OUT
LL	11 IN	LL	11 OUT
NN	12 IN	NN	12 OUT
RR	13 IN	RR	13 OUT
TT	14 IN	TT	14 OUT
VV	15 IN	VV	15 OUT
CC	07 IN	CC	07 OUT
EE	06 IN	EE	06 OUT
HH	05 IN	HH	05 OUT
KK	04 IN	KK	04 OUT
MM	03 IN	MM	03 OUT
PP	02 IN	PP	02 OUT
SS	01 IN	SS	01 OUT
UU	00 IN	UU	00 OUT

CGC 7900 DMA Connector Pin Outs
Table 6-1.

All pins are lettered in alphabetical order: A through Z and AA through VV.
Skip labels G, I, O. Q, GG, II, OO and QQ

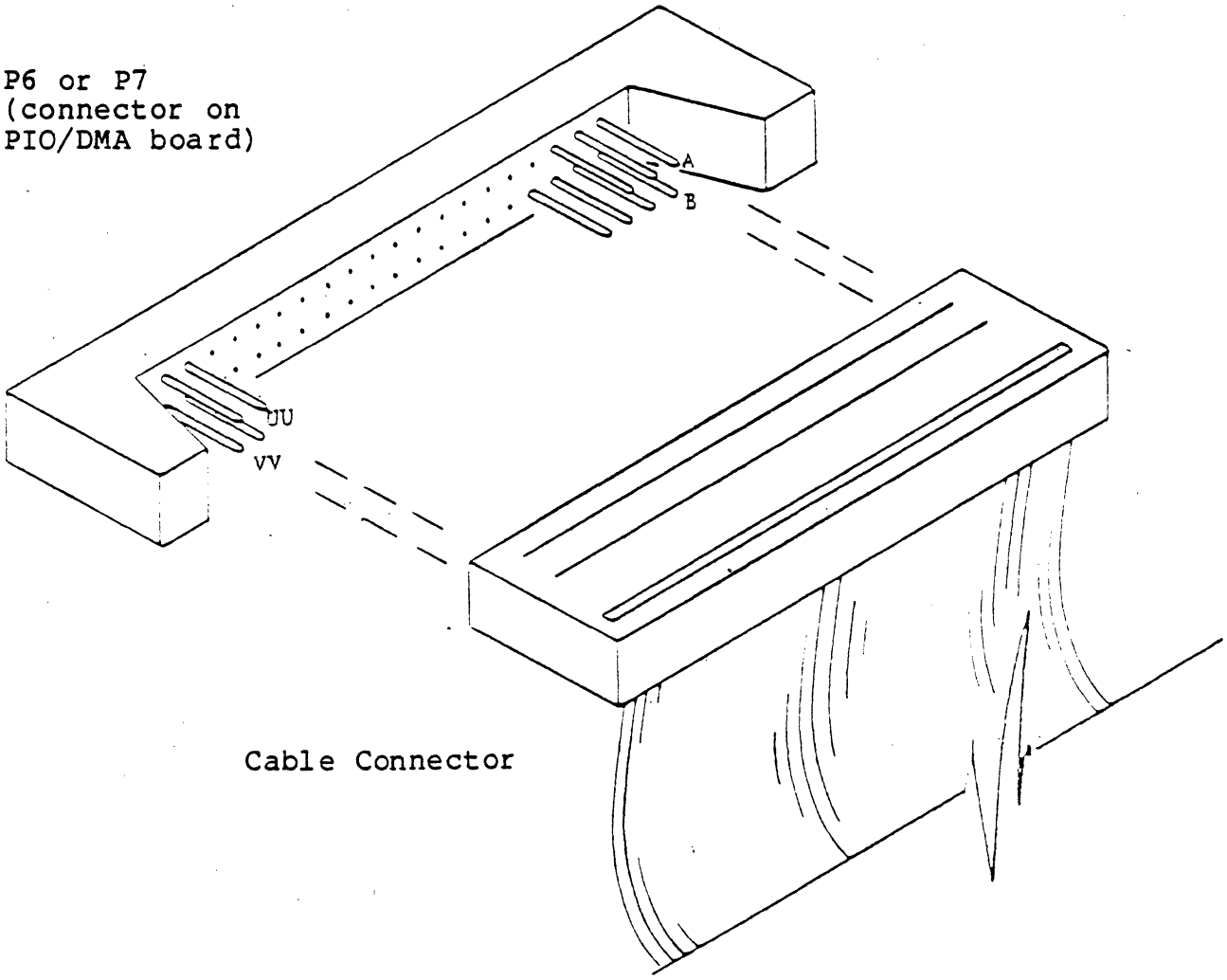


Figure 6-1. P6 or P7 Pin Definition

6.4. DMA Jumper Options

There are two jumper headers that are related strictly to the DMA portion of the circuit: J8 and J9. J8 selects the polarity of the CYCLE REQUEST line at the user interface connections. J9 selects the polarity of the BUSY line. See Figure 1-1 for jumper relative positions.

The high state of the signal at the user interface will be between 2.2 volts and 5 volts.

6.4.1. Option 1 (DR11-W)

The first jumper configuration is to be used with the DR11-W interface. Jumper J8 is in the B position and jumper J9 is in the A position, selecting a high CYCLE REQUEST and a high BUSY signal.

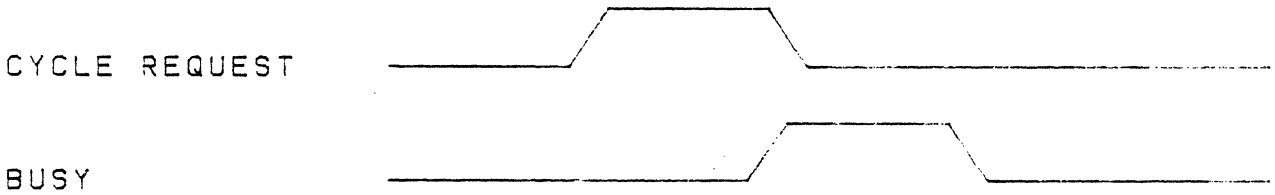


Figure 6-2. Option 1 Waveforms

6.4.2. Option 2 (DRV11-B)

The second jumper configuration is for DRV11-B applications. Both jumpers are in the B position, selecting a high CYCLE REQUEST and a low BUSY signal.

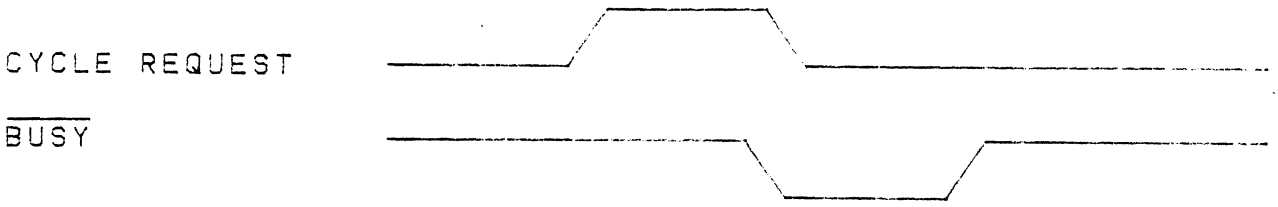


Figure 6-3. Option 2 Waveforms

6.4.3. Option 3 (DR11-B)

The third jumper configuration is for DR11-B applications. Both jumpers are in position A to select a low CYCLE REQUEST and a high BUSY signal.

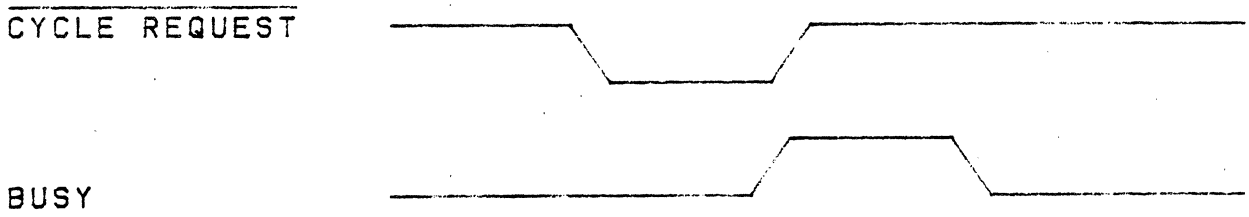


Figure 6-4. Option 3 Waveforms

6.4.4. Option 4

The fourth and final possibility is with jumper J8 in position A and jumper J9 in position B. In this configuration a low CYCLE REQUEST and a low BUSY signal is selected.

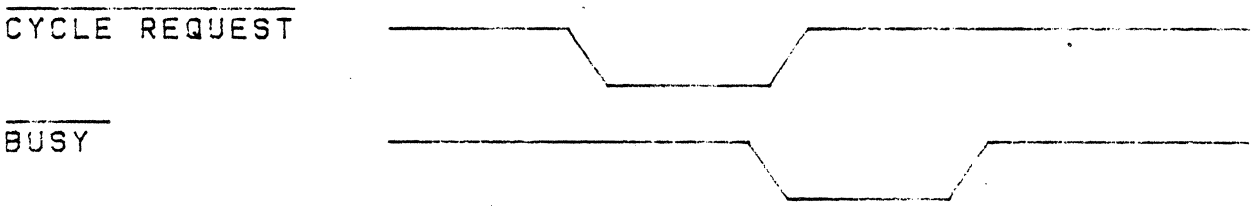


Figure 6-5. Option 4 Waveforms

NOTE:

The BUSY signal in all of the above configurations must be in its inactive state in order for CYCLE REQUEST ever to go active. The above waveforms illustrate that requirement.

The DR11 DMA interface must be activated before activating the 7900 DMA hardware.

6.5. DMA Configurations

6.5.1. CGC 7900 to DR11-B Hardware Configuration

The DR11-B is a direct memory access I/O device which is designed to be used with the DEC UNIBUS. This interface consists of a small card cage which is mounted inside the DEC computer framework. Inside the card cage is all the logic necessary to perform a DMA transfer to the DEC UNIBUS. To complete a connection from the CGC 7900 DMA board to a DEC computer having a DR11-B, two operations must be performed.

First, the DR11-B to CGC 7900 adapter board must be inserted into the DR11-B card cage at location C and D-4.

The second step is to connect the two 40-conductor ribbon cables as follows:

1) P6 of the CGC DMA Board to J1 of the Adapter Board. The red line on the cable should be UP on the PIO/DMA side and DOWN on the Adapter Board.

2) P7 of the CGC DMA Board to J2 of the Adapter Board. Observe the above orientation for this connection also.

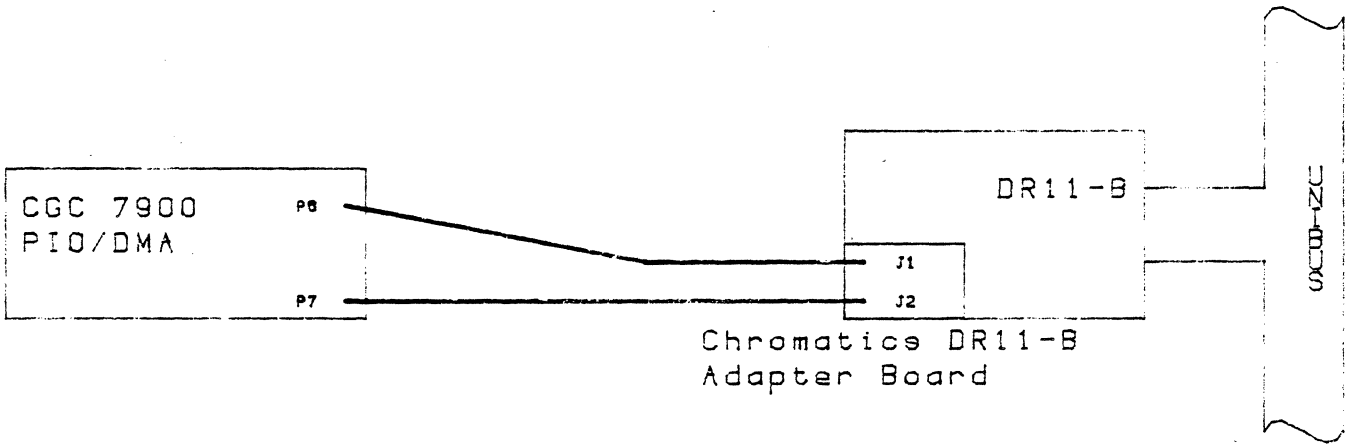


Figure 6-6. DR11-B System Configuration

6.5.2. CGC 7900 to DR11-W Hardware Configuration

The DR11-W is a single board replacement for the DR11-B. It is a general purpose DMA device used to transmit data to and from the DEC UNIBUS. To complete a hook up to a DR11-W, connect the two 40 pin ribbon cables as follows:

P6 of the CGC 7900 DMA Board to J1 of the DR11-W
P7 of the CGC 7900 DMA Board to J2 of the DR11-W

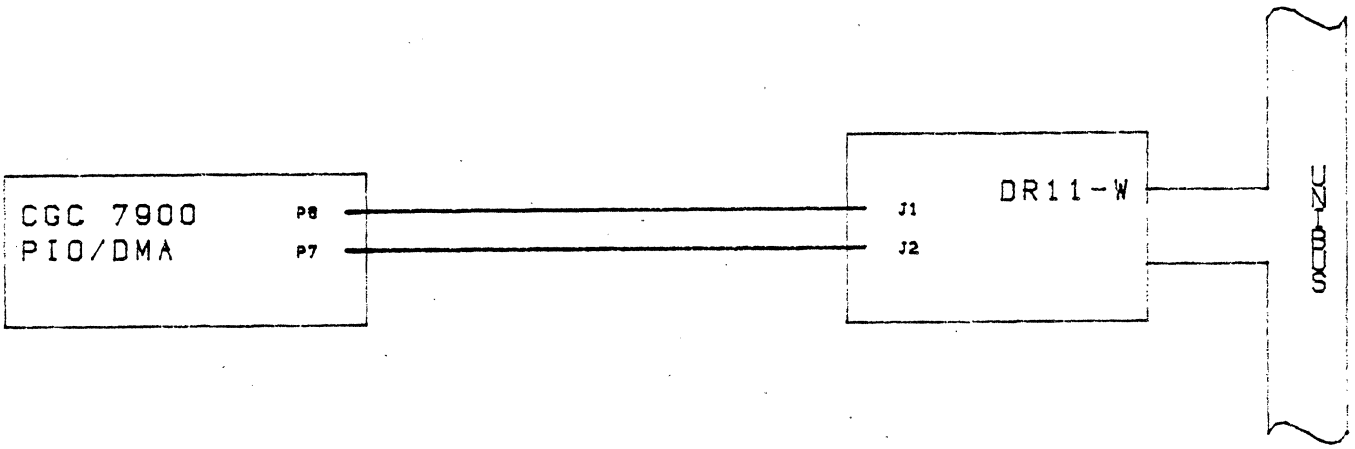


Figure 6-7. DR11-W System Configuration

6.5.3. CGC 7900 to DRV11-B Configuration

The DRV11-B is a general purpose DMA device used to transfer data to and from the DEC Q-Bus. This is the bus which is used in LSI-11 computer systems. The DRV11-B is a single board which plugs directly into the Q-Bus. To complete a hook-up to the DRV11-B, the two 40-pin ribbon cables must be installed as follows:

P6 of the CGC 7900 DMA board to J1 of the DRV11-B
P7 of the CGC 7900 DMA board to J2 of the DRV11-B

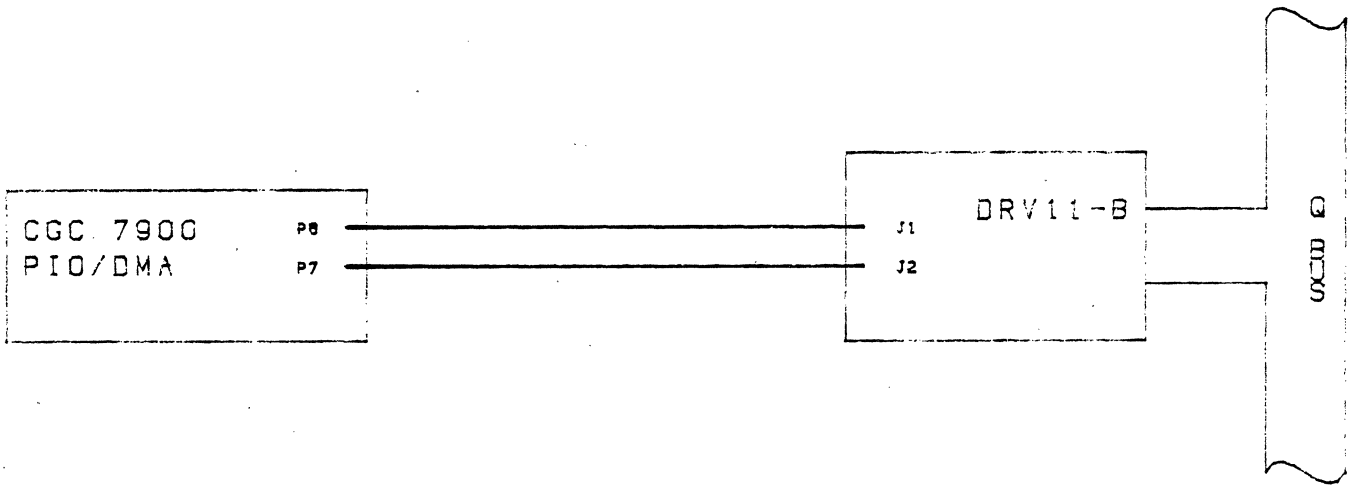


Figure 6-8. DRV11-B System Configuration

Appendix A -- Example Interface Program

```
*************************************************************************
*************************************************************************
****                                                                 ****
****                                                                 ****
****      Module Name : DmaDr                                        ****
****      Function    : DMA I/O driver                               ****
****                                                                 ****
****                                                                 ****
****      Description - The purpose of this module is to             ****
****      provide an easy interface for the system programmer        ****
****      to the CGC 7900's DMA interface board.  All entry          ****
****      and exit registers are defined below.  This program.       ****
****      with the PIO/DMA User's Manual, should provide             ****
****      all the information needed to make use of the DMA          ****
****      portion of the PIO/DMA card.                               ****
****                                                                 ****
****         When this module is called, it assumes that             ****
****      the specified data areas have been carefully               ****
****      selected by the system programmer.                         ****
****                                                                 ****
****                                                                 ****
*************************************************************************
*************************************************************************
*************************************************************************


*
*       PIO/DMA Board Registers
*

PHI     EQU $FF8400     High Data Byte Parallel Port
PLO     EQU $FF8401     Low Data Byte Parallel Port
PSTAT   EQU $FF8402     Status Byte for the Parallel Port
IMASK   EQU $FF8403     Interrupt Mask for PIO/DMA board
ARHI    EQU $FF8404     High seven address bits for DMA transfer
DMACTRL EQU $FF8405     Control Register for DMA transfer
WCREG   EQU $FF8406     High Byte Word Count Register (DMA Transfer)
WCLO    EQU $FF8407     Low Byte Word Count Register (DMA Transfer)
AREG    EQU $FF8408     High Byte (A9-A16) DMA Address Register
ARLO    EQU $FF8409     Low Byte (A1-A8) DMA Address Register
DMADAT  EQU $FF840A     Read DMA Data Word, Write DMA High Byte
DMALO   EQU $FF840B     Write DMA Data Low Byte
DMASTAT EQU $FF840D     DMA Status Byte

*
*       Mask Bits in The Interrupt Mask Register
*

MRDWD   EQU $6      Mask Interrupt Bit for Read Word
MRDLO   EQU $4      Mask Interrupt Bit for Read Low Byte
MRDHI   EQU $5      Mask Interrupt Bit for Read High Byte
MWRWD   EQU $3      Mask Interrupt Bit Write Word
MWRLO   EQU $1      Mask Interrupt Bit Write Low Byte
MWRHI   EQU $2      Mask Interrupt Bit Write High Byte
MDMADON EQU $0      Mask interrupt Bit for DMA done
```

```
*
*       Status Register Bit Definition, Parallel Port
*

IDRLO   EQU $0      Input Data Ready Low byte
IDRHI   EQU $1      Input Data Ready High byte
IDR     EQU $2      Input Data Ready Word
ODRLO   EQU $3      Ready to Write Low Byte
ODRHI   EQU $4      Ready to Write High Byte
ODR     EQU $5      Ready to Write Word

*
*       Interrupt Vector Locations
*

Vlbytin EQU $20C        Interrupt Vector Low Byte Read
Vhbytin EQU $208        Interrupt Vector High Byte Read
Vwordin EQU $204        Interrupt Vector Word Read
Vlbytwr EQU $218        Interrupt Vector Low Byte Write
Vhbytwr EQU $214        Interrupt Vector High Byte Write
Vwordwr EQU $210        Interrupt Vector Write Word
Vdmadon EQU $21C        Interrupt Vector DMA done


    ORG.L   $1F000


DMABOOT MOVE.B  DMASTAT,D0      Make sure interrupt is reset
        MOVE.L  #RDINT,Vdmadon  Set up vector address
        BCLR    #MDMADON.IMASK  Enable DMA done interrupt
        RTS


*
*   This subroutine actually enables the hardware
*
*   Enter with:
*
*       D0 = Lower 23 Bits of the word address
*       D1 = Word Count
*       D2 = Control Information
*
ARMIT   BTST    #0,DMASTAT      Reset the interrupt
        MOVE.W  D0,AREG         Set up low 16 address bits
        LSR.L   #8,D0
        LSR.L   #8,D0           Move upper address bits for final write
        NEG.W   D1
        MOVE.W  D1,WCREG        Set up word count
        MOVE.B  D2,DMACTRL      Write to control register and wait
        MOVE.B  D0,ARHI         Zero out high seven bits of address
        RTS


*
*   A write to the High address register initiates the transfer
*

        END DMASMPLE
```

Appendix B -- Long Line DMA Interface Option

B.1. General

The Chromatics Long Line DMA Interface enables the DMA portion of the PIO/DMA board to communicate with a host over distances of up to 2,000 feet. The interface to the Long Line Board on the host side is DR11-WA compatible. All signals received and transmitted by the Long Line board are RS-422 compatible. Absolutely no software modifications are required in converting a DEC/7900 (DR11-W) DMA interface to a DEC/7900 (DR11-WA) Long Line interface.

B.2. Physical Description

The Long Line board occupies one slot in the 7900 backplane and picks up power, ground and system clock from the 7900 bus. Other signals are received from the PIO/DMA circuit board and the host system.

The Long Line Interface connects to P6 and P7 on the PIO/DMA board and J4 and J5 on the Long Line Interface board, using a pair of 40-pin ribbon cables (supplied by Chromatics). The host adapter is interfaced through three 40-pin connectors (J1, J2 and J3), and three 40-conductor cables (not supplied by Chromatics).

The signals passed between the PIO/DMA board and the Long Line board are single ended TTL. These signals are received and then passed through differential line drivers and retransmitted to the host. Signals received from the host are terminated with a 100 ohm shunt resistor across the inputs of the differential line receivers and then sent to the PIO/DMA circuit board.

B.3. Handshake Integrity

There are two signals on the DR11-W interface which are used to control the transfer of data between the host and the 7900: **CYCLE REQUEST** and **BUSY**.

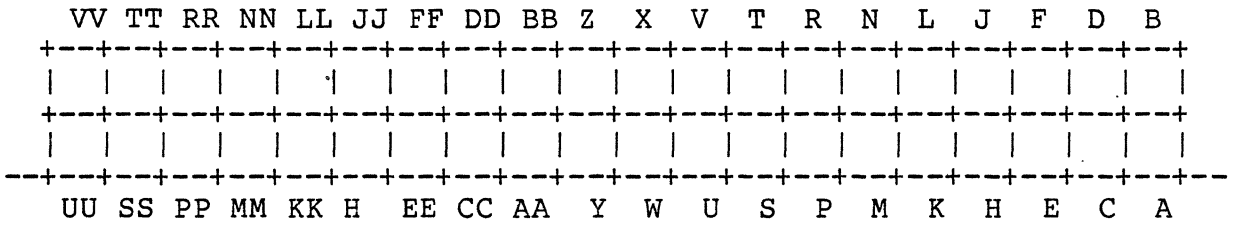
CYCLE REQUEST is transmitted by the 7900 to the DR11-W and indicates that a new data word is being requested from the host's main memory or a new data word is ready for transfer into the host's main memory. When the DR11-W detects **CYCLE REQUEST**, it asserts **BUSY**. This indicates to the 7900 that the DR11-W is requesting the system bus in preparation for the transfer of the data into or out of main memory.

When using the Long Line Interface, it is possible that the data being transferred between the host and the 7900 has not had sufficient set up time on either the 7900 end or the host end. This relationship between the set of the data and the signals indicating that the data is indeed set up is known as skewing. Two circuits have been included on the Long Line Interface board to allow for more set up time on either the host end or the 7900 end. Each circuit consists of a shift register and a jumper header. One each has been designed into the **CYCLE REQUEST** and **BUSY** signals. Depending on the position of the jumper on each header, the set time of the data to the corresponding signal going active can be varied from 70 to 280 nsecs.

Appendix C -- Connections and Connector Pinouts

PIO/DMA ------	Long Line
P6	J4
P7	J5

Long Line ----	DR11-WA
J1	J1
J2	J2
J3	J3



Front View all Connectors

J1 Connector Pin Out

Long Line Signal	DR11-W Signal	Direction	Pin
READY DIFF (H)	READY	To 7900	A
READY DIFF (L)		To 7900	B
N.C.			C
N.C.			D
BUSY DIFF (H)	BUSY	To 7900	E
BUSY DIFF (L)		To 7900	F
FNCT 3 DIFF (H)	FNCT 3	To 7900	H
FNCT 3 DIFF (L)		To 7900	J
FNCT 2 DIFF (H)	FNCT 2	To 7900	K
FNCT 2 DIFF (L)		To 7900	L
FNCT 1 DIFF (H)	FNCT 1	To 7900	M
FNCT 1 DIFF (L)		To 7900	N
N.C.			P
N.C.			R
BAI ENB DIFF (H)	BAI ENB	To HOST	S
BAI ENB DIFF (L)		To HOST	T
BURST DIFF (H)	BURST (SGL CYC)	To HOST	U
BURST DIFF (L)		To HOST	V

Note 1: BAI ENB = Bus Address Increment Enable

J1 Pin Out Cont.

Long Line Signal	DR11-W Signal	Direction	Pin
CYC REQ DIFF B	CYC REQ B	NOT USED	W
CYC REQ DIFF B		NOT USED	X
END CYC DIFF B		NOT USED	Y
END CYC DIFF B		NOT USED	Z
GO DIFF		NOT USED	AA
GO DIFF		NOT USED	BB
WCI ENB DIFF (H)	WCI ENB	TO HOST	CC
WCI ENB DIFF (L)		TO HOST	DD
NC			EE
NC			FF
STAT A DIFF (H)	STATUS A	TO HOST	HH
STAT A DIFF (L)		TO HOST	JJ
STAT B DIFF (H)	STATUS B	TO HOST	KK
STAT A DIFF (L)		TO HOST	LL
STAT C DIFF (H)	STATUS C	TO HOST	MM
STAT C DIFF (L)		TO HOST	NN
CYC REQ A DIFF (H)	CYCLE REQUEST	TO HOST	PP
CYC REQ A DIFF (L)		TO HOST	RR
C1 DIFF (H)	C1	TO HOST	SS
C1 DIFF (L)		TO HOST	TT
A00 DIFF (H)	A00	TO HOST	UU
A00 DIFF (L)		TO HOST	VV

Note 1: WCI ENB = Word Count Increment Enable
Note 2: CYC REQ = Cycle Request

J2 Connector Pin Out

Long Line Signal	DR11-W Signal	Direction	Pin
D OUT 00 (H)	D OUT 00	TO HOST	A
D OUT 00 (L)		TO HOST	B
D OUT 01 (H)	D OUT 01	TO HOST	C
D OUT 01 (L)		TO HOST	D
D OUT 02 (H)	D OUT 02	TO HOST	E
D OUT 02 (L)		TO HOST	F
D OUT 03 (H)	D OUT 03	TO HOST	H
D OUT 03 (L)		TO HOST	J
D OUT 04 (H)	D OUT 04	TO HOST	K
D OUT 04 (L)		TO HOST	L
D OUT 05 (H)	D OUT 05	TO HOST	M
D OUT 05 (L)		TO HOST	N
D OUT 06 (H)	D OUT 06	TO HOST	P
D OUT 06 (L)		TO HOST	R
D OUT 07 (H)	D OUT 07	TO HOST	S
D OUT 07 (L)		TO HOST	T
NC			U
NC			V
NC			W
NC			X
D OUT 08 (H)	D OUT 08	TO HOST	Y
D OUT 08 (L)		TO HOST	Z

J2 Pin Out Cont.

Long Line Signal	DR11-W Signal	Direction	Pin
D OUT 09 (H)	DOUT 09	TO HOST	AA
D OUT 09 (L)		TO HOST	BB
D OUT 10 (H)	D OUT 10	TO HOST	CC
D OUT 10 (L)		TO HOST	DD
D OUT 11 (H)	D OUT 11	TO HOST	EE
D OUT 11 (L)		TO HOST	FF
D OUT 12 (H)	D OUT 12	TO HOST	HH
D OUT 12 (L)		TO HOST	JJ
D OUT 13 (H)	D OUT 13	TO HOST	KK
D OUT 13 (L)		TO HOST	LL
D OUT 14 (H)	D OUT 14	TO HOST	MM
D OUT 14 (L)		TO HOST	NN
D OUT 15 (H)	D OUT 15	TO HOST	PP
D OUT 15 (L)		TO HOST	RR
C0 DIFF (H)	C0	TO HOST	SS
C0 DIFF (L)		TO HOST	TT
ATTN DIFF (H)	ATTN	TO HOST	UU
ATTN DIFF (L)		TO HOST	VV

J3 Connector Pin Out

Long Line Signal	DR11-W	Direction	Pin
D IN 00 (H)	DIN 00	TO 7900	A
D IN 00 (L)		TO 7900	B
D IN 01 (H)	DIN 01	TO 7900	C
D IN 01 (L)		TO 7900	D
D IN 02 (H)	DIN 02	TO 7900	E
D IN 02 (L)		TO 7900	F
D IN 03 (H)	DIN 03	TO 7900	H
D IN 03 (L)		TO 7900	J
D IN 04 (H)	DIN 04	TO 7900	K
D IN 04 (L)		TO 7900	L
D IN 05 (H)	DIN 05	TO 7900	MM
D IN 05 (L)		TO 7900	NN
D IN 06 (H)	DIN 06	TO 7900	PP
D IN 06 (L)		TO 7900	RR
D IN 07 (H)	DIN 07	TO 7900	SS
D IN 07 (L)		TO 7900	TT
NC			U
NC			V
NC			W
NC			X
D IN 08 (H)	DIN 08	TO 7900	Y
D IN 08 (L)		TO 7900	Z

J3 Pin Out Cont.

Long Line Signal		DR11-W	Direction	Pin
D IN 09	(H)	DIN 09	TO 7900	AA
D IN 09	(L)		TO 7900	BB
D IN 10	(H)	DIN 10	TO 7900	CC
D IN 10	(L)		TO 7900	DD
D IN 11	(H)	DIN 11	TO 7900	EE
D IN 11	(L)		TO 7900	FF
D IN 12	(H)	DIN 12	TO 7900	HH
D IN 12	(L)		TO 7900	JJ
D IN 13	(H)	DIN 13	TO 7900	KK
D IN 13	(L)		TO 7900	LL
D IN 14	(H)	DIN 14	TO 7900	MM
D IN 14	(L)		TO 7900	NN
D IN 15	(H)	DIN 15	TO 7900	PP
D IN 15	(L)		TO 7900	RR
INIT DIFF	(H)	INIT	TO 7900	SS
INIT DIFF	(L)		TO 7900	TT
INITV2 DIFF	(H)	IV2	TO 7900	UU
INITV2 DIFF	(L)		TO 7900	VV

Appendix D -- Custom Interface Notes

The Chromatics PIO/DMA User Manual contains all the information necessary to perform DMA transfers. If the DMA connection between the 7900 and the user device is not a DR11-W type interface the notes below should aid in keeping the connection simple. The signals that are most crucial in performing DMA transfers to and from the CGC 7900 are:

- **CYCLE REQUEST**
- **BUSY**
- **READY**
- **Data IN**
- **Data OUT**
- **C1**

It is important to understand from the outset that all DMA operations performed through the PIO/DMA circuit board are initiated by the 7900. This "master/slave" relationship between the 7900 and the host, or other user device, must be understood by anyone trying to do a custom interface. Under the DR11-W protocol, the READY signal going from the host to the 7900 indicates that the DR11-W has been programmed and is now ready to respond to any **CYCLE REQUEST**s generated by the 7900. Once the 7900 firmware has detected **READY**, the appropriate registers will be loaded and the hardware will begin to issue **CYCLE REQUEST**s.

The host, or other user device, is expected to respond to the **CYCLE REQUEST** with **BUSY.** Data being transferred to the host is valid on the leading edge of the **CYCLE REQUEST** signal. Data being transferred from the host is latched into the onboard data buffers on the trailing edge of **BUSY.** This handshake will continue until the word count register on the DMA circuit board has been exhausted. A more detailed description of the interface operation is given in the the PIO/DMA User Manual.

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