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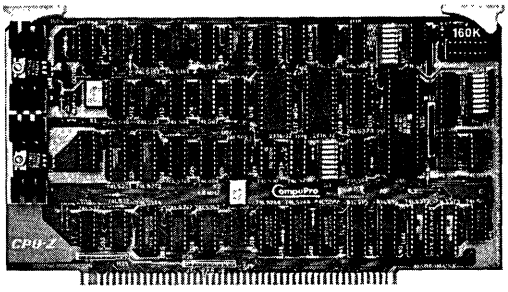
# CPU-Z
## Technical Manual




IEEE 696/S-100
2-6 MHz CPU (SWITCH SELECTABLE)
WITH ON-BOARD RAM/ROM AND INTERRUPT CONTROL

CPU-Z
Technical Manual

Hayward, CA 94545

Document No: 11608
File Name: CPUZ.MAN
Board No: 160K

First Edition: 1982
Second Edition: February 1984
Latest Printing: August, 1984

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# CONTENTS

# HOW TO GET YOUR CPU-Z UP AND RUNNING WITHOUT READING THE MANUAL

This section is for those of you who are anxious to see your new CPU board working without having to read the entire manual. By setting all the switches off except for switch 3, position 5, which should be switched on, the board will be set up for the standard CompuPro configuration. This assumes that you are not planning to run at the slow CPU-Z speed and that you do not require wait states generated on the CPU.

After you install the board and attach the cables, your board should work. If it doesn't, do not panic. Relax, read the rest of the manual and proceed with patience.

## TECHNICAL OVERVIEW

The CPU-Z with a Z80 CPU, features on-board memory sockets, a power-on-jump circuit to any 256 byte boundary, a Memory Manager to extend the addressing range of the system from 64 Kbytes to a maximum of 16 Mbytes of system RAM, fully maskable vectored interrupts to speed up system throughput by eliminating polling loops, and wait state generation circuitry for all machine cycles.

Other features standard to all CompuPro boards include thorough bypassing of all supply lines to suppress transients, on board regulators, and low power Schottky TTL and MOS technology integrated circuits for reliable, cool operation. All this and sockets for all ICs go into a double sided, solder masked printed circuit board with a complete component legend.

## USING VECTORED INTERRUPTS

The CPU chip recognizes 8 instructions as Restart0 - Restart7. These instructions will cause the program counter to jump to one of eight locations depending on the Restart instruction.

| RESTART | Program Counter(HEX) |
|---|---|
| 0 | 0 |
| 1 | 8 |
| 2 | 10 |
| 3 | 18 |
| 4 | 20 |
| 5 | 28 |
| 6 | 30 |
| 7 | 38 |

At these locations, jumps to interrupt driver routines can be placed into either RAM or PROM. Then when one of the VI0 - VI7 lines goes low, the specific routine can instantly be started to service the interrupting device. Upon Power-on-Clear or reset (pRESET*) the interrupt mask is cleared, enabling all eight interrupt lines (NOTE: This does NOT mean that the Z80 has interrupts enabled.) Then (with the VI switch [SW3-8] turned ON) when any of the VI inputs goes low the Restart will be generated if the CPU has previously received an Enable Interrupts (FB[H]) command. To disable an individual interrupt line, or a group of lines, the mask must be set up by an output to Port FE(H) with the desired mask in the Accumulator. A "1" in the mask will disable the interrupt line, and a "0" will enable the interrupt line.

If it is desired to use this CPU-Z board with the Z80 mode 2 interrupts, the on-board vector generation circuitry must be disabled. To do this switch SW3-8 should be turned OFF, and all 1s should be output to the interrupt mask port (Port FE[H]). This will prevent the CPU-Z from responding to the VI lines, but it will still respond to the bus interrupt signal (bus pin 73).

| EXAMPLE | (HEX) | (BINARY) |
|---|---|---|
| to disable VI5-VI7 | 03 | (00000111) |
| to disable VI2 | 20 | (00100000) |
| to disable all | FF | (11111111) |

Note that the VI lines are all open collector and more than one device can be connected to each VI line by using open collector gates.

It is recommended to put a "DEAD MEMORY" error recovery routine at location 38 (H), since this location will be jumped to in case the CPU encounters an FF (H) instruction, which corresponds to a restart 7. This is the instruction that will be read from a memory location for which there is no system memory. Location 38 is the most common launching pad for CPU flights into never-never land.

**USING THE NONMASKABLE INTERRUPT**

The S-100 bus has a NMI* pin (bus pin 12) which is implemented on the CPU card for any function that the user desires. NMI* is primarily used for a catastrophic system failure, such as loss of primary power. This interrupt enables the processor to execute a short program to save current system parameters on either a disk or some other nonvolatile memory before total power is lost (which usually takes milliseconds, lots of time for a computer). The NMI* causes the CPU to jump to address 66(H), which should be initialized with a routine to control the interrupt.

**EXTENDED ADDRESSING**

Address lines A16-A23 are driven through output port FD(H) and can be changed with a simple output instruction. Upon Power-on-Clear or reset (pRESET*) the extended address lines will be reset to 0, bringing the system up in base page. To access memory in other than base page requires an output to Port FD(H) with the desired page address in the Accumulator in order to set the extended address lines A16-A23. These address lines are pin numbers 16, 17, 15, 59, 61, 62, 63, & 64, for address lines A16-A23 respectively.

Example:

| ACCUMULATOR DATA (HEX) | TO ACCESS PAGE (BINARY) | (HEX) |
|---|---|---|
| 40 | 01000000 | 40 |
| 2 | 00000010 | 2 |
| F0 | 11110000 | F0 |

Of course, to take advantage of this extended addressing feature requires memory boards which respond to extended address lines. If a board does not monitor the S-100 extended address lines, then only the normal 16 address lines will be decoded.

**WAIT STATES**

A single wait state may be added to any processor cycle by closing the corresponding dip switch on SW1. A wait may be added to:

| CYCLE | SWITCH POSITION |
|---|---|
| ON-BOARD MEMORY | 1 |
| I/O | 2 |
| MEMORY | 3 |
| INSTRUCTION | 4 |

Due to critical timing requirements of the Z80 during an instruction fetch (M1), extra time may be required for marginally slow memory chips. When running at 4 MHz or 6 MHz some RAM chips may also need more time for each memory operation than is normally allowed. The on-board-memory sockets may be used for many different speed parts, and when running at 4 MHz or 6 MHz a wait state may be needed for a fetch there also. In addition, since the internal architecture of the RAM 16 and RAM 21 are optimized for 16 bit CPUs, a memory request wait state (S1-3) may be required when running either of these memory boards with the 6 MHz CPU-Z.

**ON-BOARD-MEMORY SOCKETS**

The MEMORY sockets on this board are set up to take INTEL 2716, T.I. 2516 2Kx8 EPROMS, or any of the new 2Kx8 RAM chips which are pin compatible (Hitachi HM6116 or equivalent). By cutting J2(A-B) on the solder side above U17, J4 on the solder side to the left of U29, an J5(A-C) on the solder side to the left of U29 and installing jumpers J2(A-C) and J5(A-B) the sockets can now be used for 2732 4Kx8 EPROMS. (NOTE: Extreme care must be used when soldering in the jumpers so as not to damage the board or any of the traces. A soldering iron of no more than 25 watts should be used.) With 2732s SW3-4 is no longer used to address the sockets. The on-board sockets will be totally disabled when switch SW3-5 is ON. With SW3-6 ON, the sockets are addressable anywhere in base page (A16-A23 are all 0) on a 4K boundary (8K for the 2732s). This feature allows the user to have on-board-memory in base page only. With SW3-6 OFF, the sockets ignores address lines A16 - A23 and occupies every page of memory. A prime example of how to use the

sockets in this "shadow" mode would be to use them with SW3-6 turned ON and the Power-on-jump set to the start of the PROM address, then when the system is initially turned on the program in the PROM will start and either initialize the system by booting in a disk program, or some other type of routine. Then the last thing the PROM will do is jump to the RAM address where the initialization routine was loaded. The first thing that program will do is an output to port FD(H) of anything except 0. This will set the extended page address to the page that was in the Accumulator, and the sockets will be disabled. RAM which was overlapped with the PROM can now be used and a complete memory map is available to the user. SW3 positions 1-4 are used for address lines A15-A12. The socket closest to the Z-80 chip is the low address half and the left socket the high half.

| | SWITCH S3 | | | | DESIRED START ADDRESS (HEX) | |
|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 2716 | 2732 |
| | 0 | 0 | 0 | 0 | 0000-0FFF | 0000-1FFF |
| | 0 | 0 | 0 | 1 | 1000-1FFF | |
| ON = "0" | 0 | 0 | 1 | 0 | 2000-2FFF | 2000-3FFF |
| OFF = "1" | 0 | 0 | 1 | 1 | 3000-3FFF | |
| | : | : | : | : | : : | : : |
| | : | : | : | : | : : | : : |
| | 1 | 0 | 1 | 0 | A000-AFFF | A000-BFFF |
| | : | : | : | : | : : | |
| | 1 | 1 | 1 | 1 | F000-FFFF | |

To disable sockets completely, turn ON SW3-5

**CLOCK**

The clock for this system can be set to allow the CPU to run at either 3 MHz or 6 MHz. SW1-5 is used to select between these two speeds. When SW1-5 is ON the CPU will run at 3 MHz and bus pin 24 ($\phi$) will have a 3 MHz square wave on it. When SW1-5 is OFF, the system will run at 6 MHz and bus pin 24 will have a 6 MHz square wave on it. With a 16 MHz crystal used for X1 the speed switch SW1-5 will select between processor speeds of 4 MHz (when OFF) and 2 MHz (when ON). Bus pin 49 (CLK) will always have a 2 MHz signal on it.

**POWER-ON-JUMP/JUMP-ON-RESET**

Provisions have been made on this board to allow the processor to jump to any memory location on a 256 byte boundary on either a power-on only, or every reset also. To enable this feature, JMP ENABLE (SW1-8) should be turned ON and the jump address should be set on switch S2 according to the following table. To enable the jump on every reset also, SW3-7 should also be turned ON.

| SWITCH POSITION | FUNCTION | |
|---|---|---|
| 1 | ADDRESS A15 | |
| 2 | ADDRESS A14 | |
| 3 | ADDRESS A13 | |
| 4 | ADDRESS A12 | ON = "1" |
| 5 | ADDRESS A11 | OFF = "0" |
| 6 | ADDRESS A10 | |
| 7 | ADDRESS A9 | |
| 8 | ADDRESS A8 | |

EXAMPLE: To jump to E900 for a North Star floppy disk system, S2 positions 1-3,5, and 8 should be ON and S2 positions 4,6,and 7 should be OFF. JMP ENABLE (SW1-8) should be ON to enable this feature. NOTE: Since the jump circuitry disables the input buffer, it is unnecessary to use the phantom line (S-100 pin 67) for proper operation.

**MWRITE GENERATION**

The CPU-Z has circuitry on board for generating the MWRITE signal (bus pin 68) and a positive going strobe will be generated for each memory write operation. This circuitry looks at the bus and whenever the sOUT signal is low, and the pWR* signal strobes low, an MWRITE strobe will be generated. This signal must be generated at only one source in each system. If there is a front panel in your system it also may be generating the MWRITE signal, and the signal from the CPU-Z must be disabled. There are two ways to disable this signal:

A) Cut jumper J7 on the solder side below U36 and R21; or

B) Remove pin 9 of U36 from its socket and let the pin hang out.

This makes it easier to reconnect the pin should you ever want MWRITE to be generated from the CPU-Z board in the future. If MWRITE is generated in more than one place, memory boards that rely on MWRITE as their write strobe may not work properly.

**IMSAI FRONT PANEL USAGE**

If you have an IMSAI type front panel this CPU will require minor modifications to work properly. The problems arise from the fact that the IMSAI front panel (which does not conform to the IEEE standard) requires some signals that are not on the S-100 bus. Jumper pads are provided to allow these lines to be used. J6, and J8 should be installed to connect bus pins 53, and 21 (J8 connect C to 2) respectively to control the CPU from the front panel. If the system is set to run at 4 MHz or 6 MHz, the front panel will force the CPU to run at 2 MHz or 3 MHz when the RUN/STOP signal is in the STOP mode. This will allow for proper front panel operation which is speed dependent. Socket J3 in the upper right corner is for the front panel connector. Jumper J9 can be installed to have the CPU drive bus pin 27 (which was the WAIT

line). Pin 13 of U38 must also be removed from the socket and tied to +5 volts. This can be done by connecting the free hanging pin 13 to pin 14 and keeping pin 14 in the socket. This will allow the DATA OUT bus to reflect the DATA IN bus information which the front panel reOuires. The MWRITE circuitry will also have to be disabled if the front panel is going to generate MWRITE (bus pin 68).

## CIRCUIT DESCRIPTION

### VECTORED INTERRUPTS AND MASK

Upon reset (pRESET*) U23 is cleared, and will output all lows to the OR gates (U33 & U34). The VI0 - VI7 inputs normally sit at a high level, and hence all inputs on U22 are high. This resting state makes the GS output high. Upon receiving a vectored interrupt when one of the VI0 - VI7 inputs goes low, U22 will output a value corresponding to the highest priority interrupt on the lines. This value will go to U44 and when the CPU acknowledges the interrupt, the proper Restart command will go to the CPU. When a 1 has been written into the mask port FE(H), U23 will output a high to the associated OR gate (U33 & U34). Then when an interrupt pulls the input low, U22 will still have a high input and will never detect interrupts that are being masked out.

### EXTENDED ADDRESSING

When an OUT FD(H) instruction is executed, the data bits in the Accumulator are latched into U24 and output on bus lines A16-A23. These address lines will be TRI-STATEd$^{tm}$ along with the other 16 address lines when ADDR-DSABL (bus pin 22) is driven low by an external device requesting control of the bus.

### CPU STATUS LINES

The S-100 bus has eight status signals that all bus masters must provide, these signals come from U45. During either a read cycle or a write cycle these status signals are latched on the bus. A short time after the read or write signal goes away the status signals are allowed to toggle. The S-100 status signals are shown below, along with their associated bus pins. (A * suffix means active low signal.)

| SIGNAL | BUS PIN |
|---|---|
| sWO* | 97 |
| sMEMR | 47 |
| sINTA | 96 |
| sM1 | 44 |
| sINP | 46 |
| sOUT | 45 |
| sHLTA | 48 |
| sXTRQ* | 58 |

These status bits are decoded from the seven control signals coming from the Z80 as shown (a * suffix means active low signal):

**STATUS SIGNALS**

| CONTROL SIGNAL | sWO* (a) | or | (b) | sMEMR | sINTA | sM1 | sINP | sOUT | sHLTA |
|---|---|---|---|---|---|---|---|---|---|
| RFSH* | 1 | | X | X | X | X | X | X | X |
| MRQ* | 0 | | X | 0 | X | X | X | X | X |
| RD* | 1 | | X | 0 | X | X | 0 | X | X |
| WR* | X | | 0 | X | X | X | X | 0 | X |
| IORQ* | X | | X | X | 0 | X | 0 | 0 | X |
| M1* | X | | X | X | 0 | 0 | X | X | X |
| HALT* | X | | X | X | X | X | X | X | 0 |

An X means a don't care condition.
The sXTRQ* signal is permanently high since this is an 8 bit processor.

**SYSTEM CLOCK**

The system clock circuitry consists mainly of U1, U3, and U4. The 16 or 24 MHz square wave is fed into U4 which divides it down to the desired system clock speed. The multiplexer U3 will feed either 16 and 24 MHz or 8 and 12 MHz to the pSYNC and pSTVAL* generation circuitry and 2 and 3 MHz or 4 and 6 MHz to the Z80 and bus for the system clock. If jumper J8 (C-2) is used, then when the SINGLE STEP LINE (bus pin 21) is low the input to U5 will be low and cause the system to run at 2 MHz. This is the same circuitry that switch SW1-5 uses to determine the system speed. X2 & U27 generate a 4 MHz clock which is divided down to 2 MHz by U2 and then through a buffer to bus pin 49, which is the clock signal.

**POWER-ON-JUMP(POJ)/JUMP-ON-RESET(JOR)**

The jump circuitry consists of octal inverter U21 (81LS96), DIP switch SW2, SIP resistor R13, hex o.c. inverter U32 (74LS05), a "D" flip flop U2, the POJ enable switch SW1-8, and JOR enable switch SW3-7. With the POJ enable switch ON, upon receiving a power-on-clear, the "D" flip flop is cleared which disables input buffer U43, and enables jump buffer U21. This action starts a three byte sequence which will cause the CPU to jump to the proper starting location. The CPU is reset to address 0, and from the jump buffer a jump (C3H) instruction is put on the data bus. At address 1 the low order address of zero is then put on the data bus, then at address 2 the high order address coming from the jump switch setting is placed on the data bus. When address 2 is in the address buffer the "D" flip flop will then be clocked to the set state and disable the jump buffer while enabling the data input buffer. The "D" flip flop will not get cleared again until the next Power-On-Clear (POC). This complete sequence also occurs for

every RESET*, if switch SW3-7 is turned ON. This option will allow the CPU to come up with a known jump on power-on and then later when a reset is recognized the CPU can either start again at 0(H) or jump to the address in switch SW2.

**WAIT STATES**

The CPU wait line (Z80 pin 24) is driven by three main sources, causing the processor to give more time for certain devices or system states. The three sources are:

a) The RDY (pin 72) bus signal, which will be driven by an external device which must have more time to respond to the CPU,

b) The XRDY (pin 3) bus signal which is driven by the front panel (if the system has one), and

c) On board selector to generate a wait state for four different states.

The on-board wait state will come from the settings of SW1 positions 1-4. M1 (SW1-4) will generate a wait state for every instruction cycle. The MRQ (SW1-3) will generate a wait state for every memory fetch cycle. The IORQ (SW1-2) will generate a wait state during every I/O operation. Finally, the ROM switch (SW1-1) will generate a wait state for every access of the on-board MEMORY. U8 will remain in the set mode with Q high unless one of these switches (SW1 positions 1-4) is turned ON. Then when one of the selected inputs go low, U8 will be cleared and cause the wait input (on the CPU) to go low. These wait states can only start when pSYNC is high. When pSYNC goes low U8 will be set and end the wait. A wait will also be generated for each interrupt acknowledge cycle to allow external interrupt controllers to respond.

**SWITCH SUMMARY**

| S1 POSITION | FUNCTION |
|---|---|
| 1 | WAIT STATE FOR ON-BOARD MEMORY |
| 2 | WAIT STATE FOR I/O |
| 3 | WAIT STATE FOR MEMORY |
| 4 | WAIT STATE FOR INSTRUCTION FETCH |
| 5 | SPEED SWITCH (OFF = HIGH SPEED) |
| 6 | NOT USED |
| 7 | NOT USED |
| 8 | POWER-ON-JUMP ENABLE |

| S2 POSITION | FUNCTION | |
|---|---|---|
| 1 | JUMP ADDRESS BIT A15 | |
| 2 | JUMP ADDRESS BIT A14 | |
| 3 | JUMP ADDRESS BIT A13 | ON = "1" |
| 4 | JUMP ADDRESS BIT A12 | OFF = "0" |
| 5 | JUMP ADDRESS BIT A11 | |
| 6 | JUMP ADDRESS BIT A10 | |
| 7 | JUMP ADDRESS BIT A9 | |
| 8 | JUMP ADDRESS BIT A8 | |

| S3 POSITION | FUNCTION | |
|---|---|---|
| 1 | SOCKET ADDRESS BIT A15 | |
| 2 | SOCKET ADDRESS BIT A14 | ON = "0" |
| 3 | SOCKET ADDRESS BIT A13 | OFF = "1" |
| 4 | SOCKET ADDRESS BIT A12 | |
| 5 | SOCKET DISABLE (WHEN ON) | |
| 6 | SOCKET BASE PAGE ONLY (WHEN ON) | |
| 7 | JUMP-ON-RESET ENABLE | |
| 8 | INTERRUPT ENABLE FOR VECTORED INTERRUPTS | |

**TYPICAL SWITCH SETTING**

For a typical CompuPro system with a CompuPro DISK 1 floppy disk controller board, all switch positions should be OFF except SW3-5. This will have the CPU-Z running at the high speed, no wait states, no power-on-jump, no vectored interrupts, and no on-board memory.

**JUMPER SUMMARY**

J2 - Used with J4, J5, to convert memory sockets for 2732 use
J3 - Front panel data socket
J4 - See J2
J5 - See J2
J6 - SSDSBL for IMSAI type systems
J7 - MWRITE brought to Bus pin 68
J8 - Run or single step for IMSAI type systems
J9 - WAIT brought to Bus pin 27

**LOGIC DIAGRAM**

The numbers inside the ovals on the logic diagram indicate where a signal comes from or goes to, for example:

U20-21 2/2D = [IC # 20] - [Pin # 21] [Page # 2] / [Coordinates 2D]

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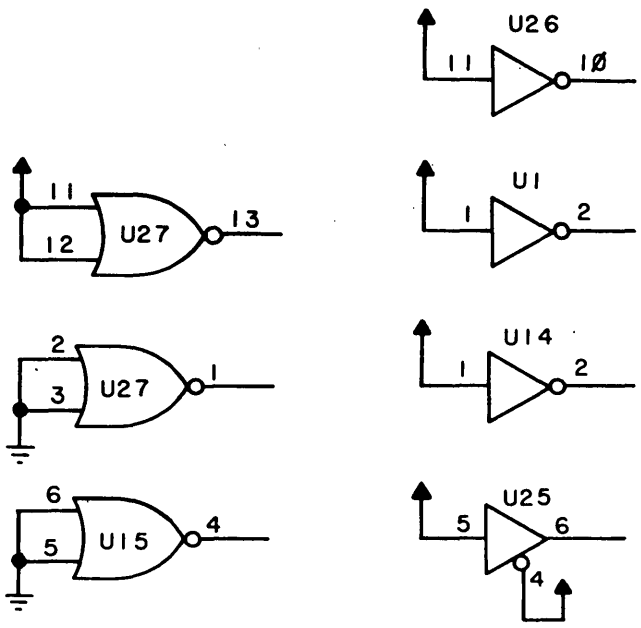
**UNUSED GATES**

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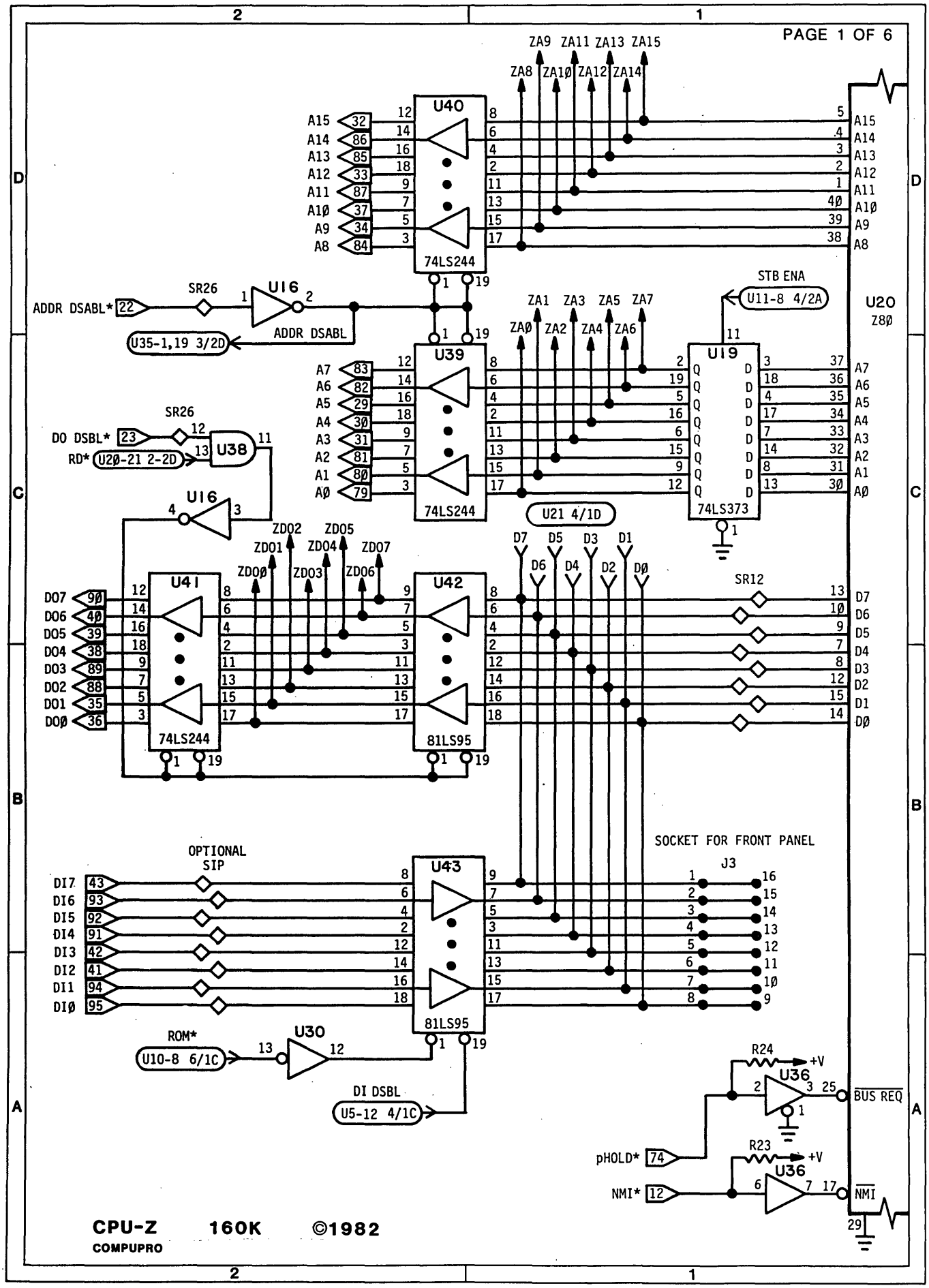
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ZA9 ZA11 ZA13 ZA15
ZA8 ZA10 ZA12 ZA14
U40
74LS244
A15 A14 A13 A12 A11 A10 A9 A8
U20
Z80
SR26
ADDR DSABL*
U16
ADDR DSABL
U35-1,19 3/2D
STB ENA
U11-8 4/2A
ZA1 ZA3 ZA5 ZA7
ZA0 ZA2 ZA4 ZA6
U39
74LS244
U19
74LS373
SR26
DO DSBL*
RD*
U20-21 2-2D
U38
U16
U21 4/1D
D7 D5 D3 D1
D6 D4 D2 D0
ZD02 ZD05
ZD01 ZD04 ZD07
ZD00 ZD03 ZD06
U41
74LS244
U42
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DO7 DO6 DO5 DO4 DO3 DO2 DO1 DO0
D7 D6 D5 D4 D3 D2 D1 D0
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J3
DI7 DI6 DI5 DI4 DI3 DI2 DI1 DI0
ROM*
U10-8 6/1C
U30
DI DSBL
U5-12 4/1C
R24
+V
U36
BUS REQ
pHOLD*
R23
+V
U36
NMI*
NMI
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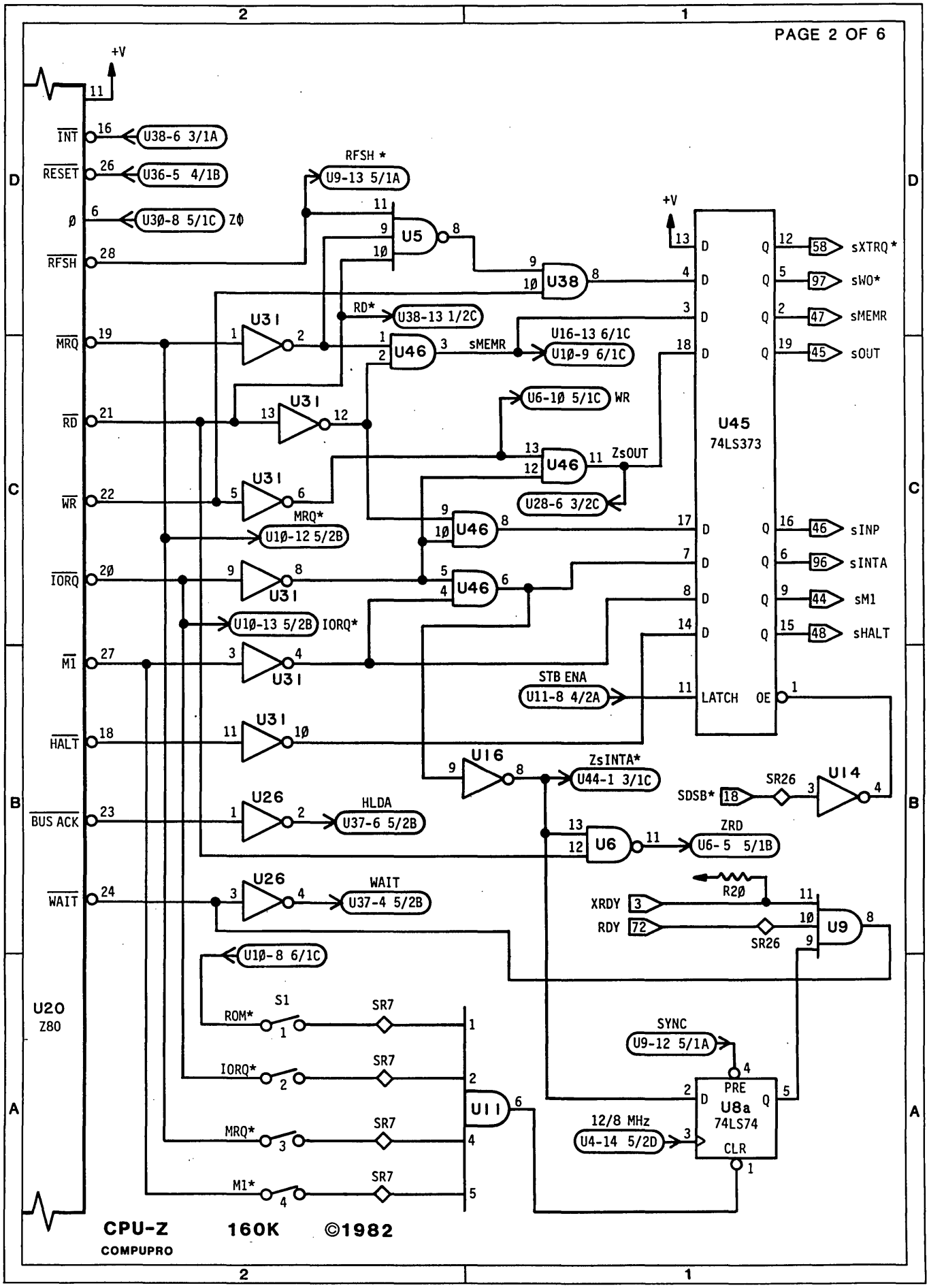
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+V
INT
RESET
Ø
RFSH
MRQ
RD
WR
IORQ
M1
HALT
BUS ACK
WAIT
U38-6 3/1A
U36-5 4/1B
U3Ø-8 5/1C
ZØ
RFSH *
U9-13 5/1A
U5
U38
RD*
U38-13 1/2C
U31
U46
sMEMR
U16-13 6/1C
U1Ø-9 6/1C
U6-1Ø 5/1C
WR
ZsOUT
U28-6 3/2C
MRQ*
U1Ø-12 5/2B
IORQ*
U1Ø-13 5/2B
U45
74LS373
sXTRQ*
sWO*
sMEMR
sOUT
sINP
sINTA
sM1
sHALT
STB ENA
U11-8 4/2A
LATCH
OE
U16
ZsINTA*
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U37-6 5/2B
U26
ZRD
U6-5 5/1B
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U37-4 5/2B
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XRDY
RDY
U9
U1Ø-8 6/1C
U20
Z80
S1
ROM*
IORQ*
MRQ*
M1*
SR7
U11
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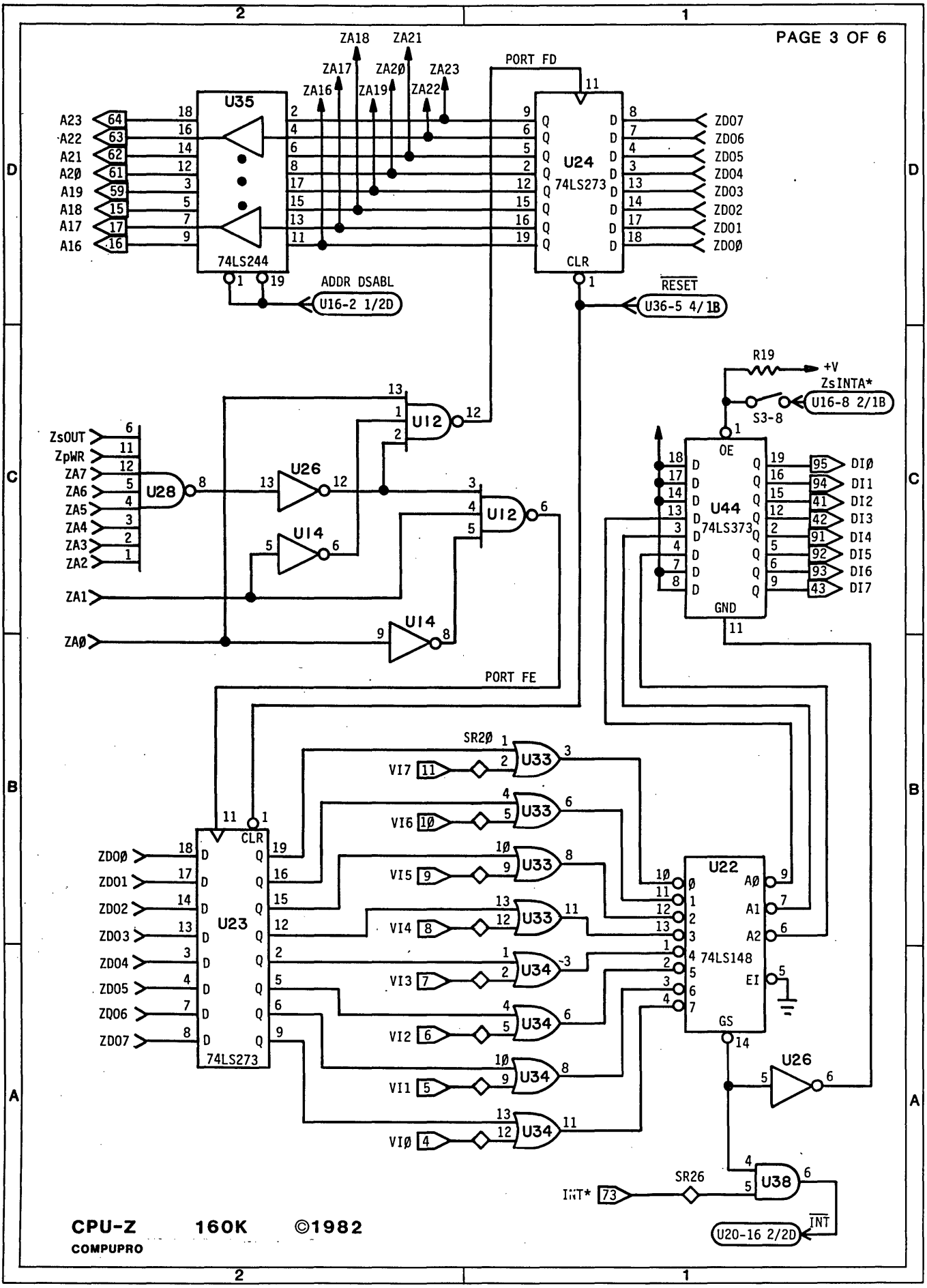
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ZA17
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ZD04
ZD03
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ZD01
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RESET
U36-5 4/1B
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ZsINTA*
U16-8 2/1B
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ZA5
ZA4
ZA3
ZA2
ZA1
ZA0
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U26
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U44
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DI2
DI3
DI4
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DI6
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VI3
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VI1
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U33
U34
U23
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U22
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GS
EI
U38
SR26
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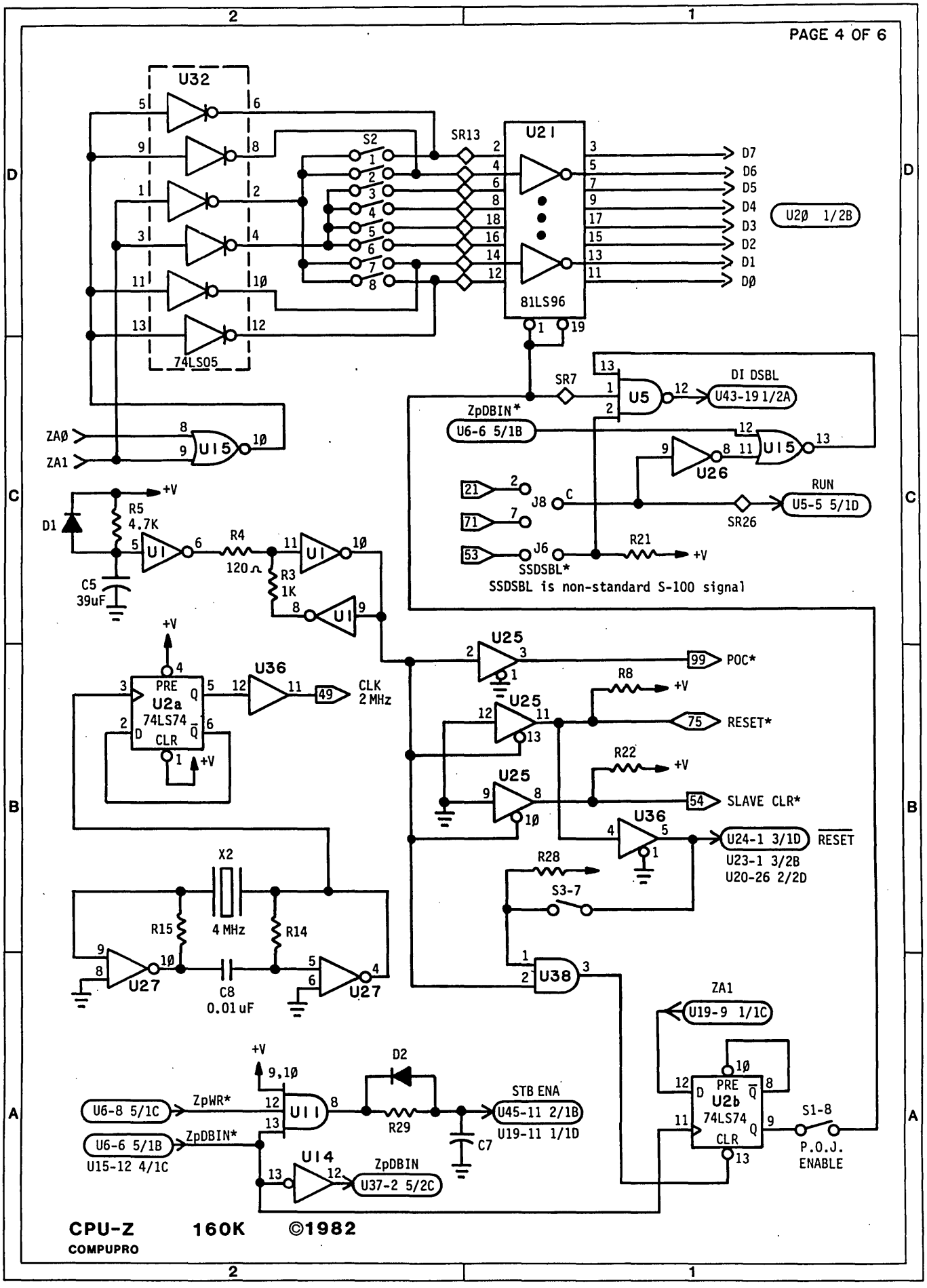
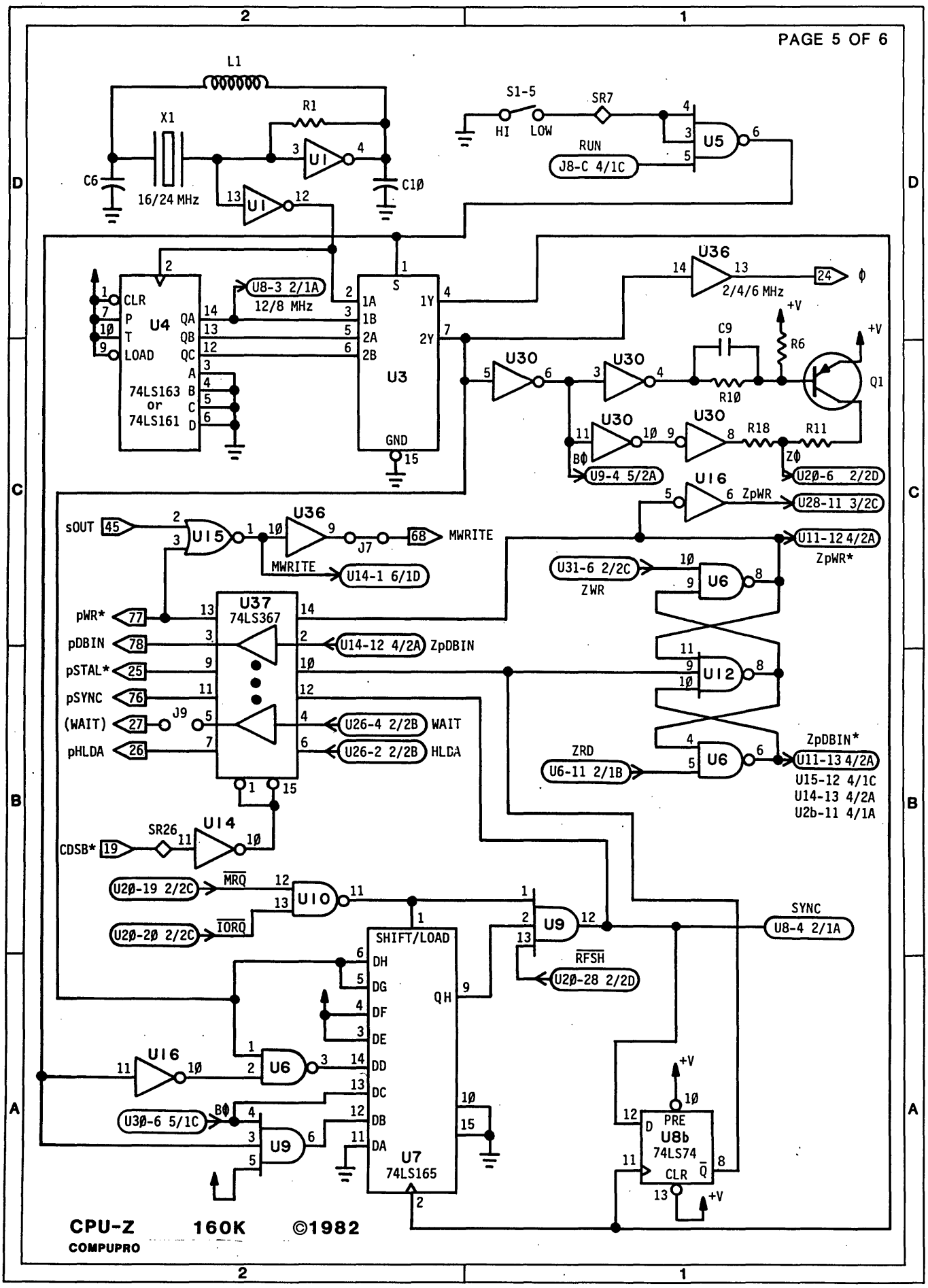

U32
74LS05
S2
SR13
U21
81LS96
D7
D6
D5
D4
D3
D2
D1
DØ
U2Ø 1/2B
ZAØ
ZA1
U15
SR7
U5
DI DSBL
U43-19 1/2A
ZpDBIN*
U6-6 5/1B
U26
RUN
U5-5 5/1D
SR26
J8
J6
SSDSBL*
R21
+V
SSDSBL is non-standard S-100 signal
D1
R5
4.7K
U1
R4
120Ω
R3
1K
C5
39uF
U25
99
POC*
R8
RESET*
R22
SLAVE CLR*
U36
U24-1 3/1D
RESET
U23-1 3/2B
U20-26 2/2D
R28
S3-7
U38
U2a
74LS74
PRE
CLR
CLK
2 MHz
X2
4 MHz
R15
R14
C8
0.01 uF
U27
ZA1
U19-9 1/1C
U2b
S1-8
P.O.J.
ENABLE
9,1Ø
D2
U6-8 5/1C
ZpWR*
U11
R29
STB ENA
U45-11 2/1B
U19-11 1/1D
C7
U6-6 5/1B
ZpDBIN*
U15-12 4/1C
U14
ZpDBIN
U37-2 5/2C
CPU-Z 160K ©1982
COMPUPRO

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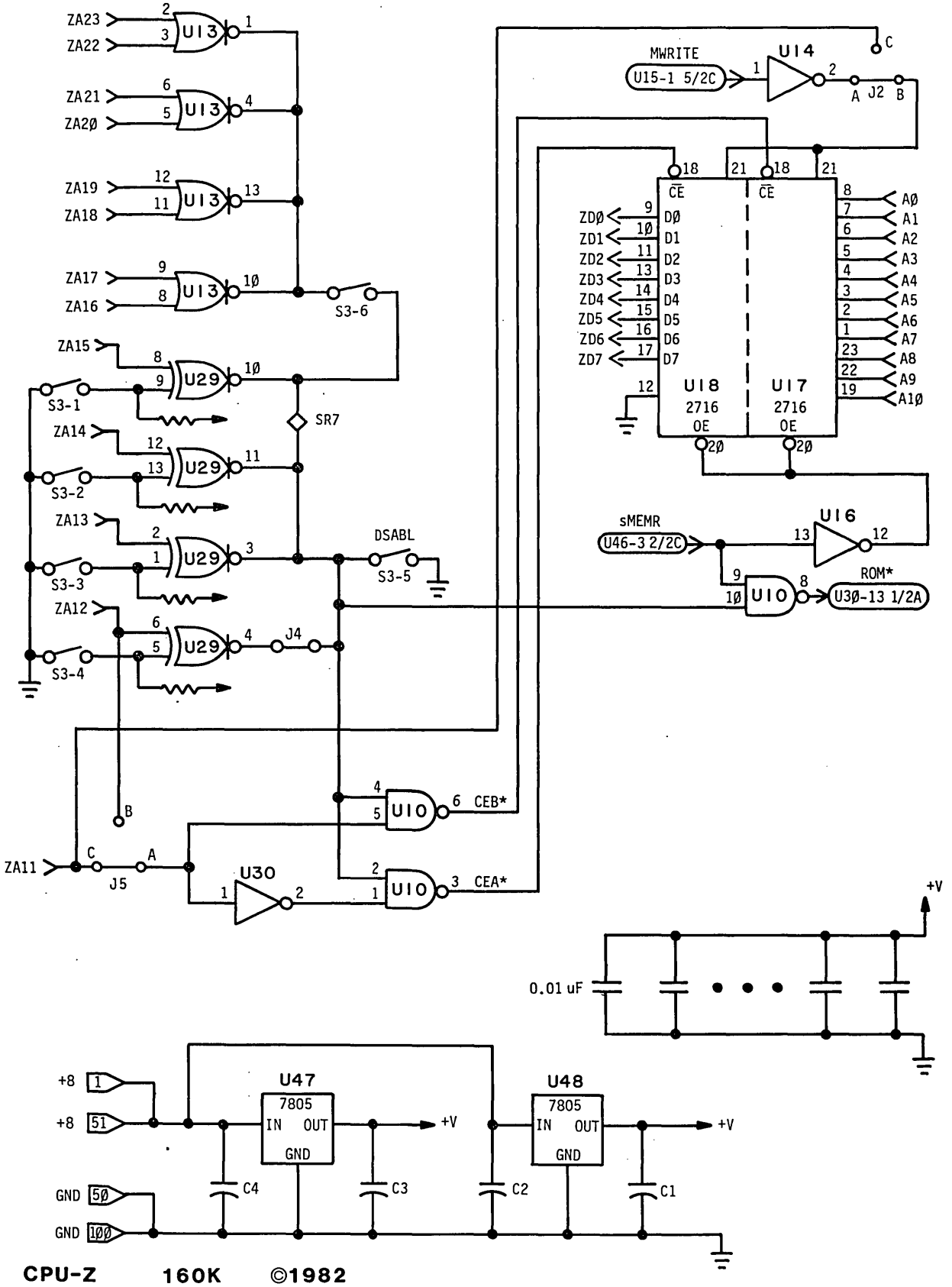
JUMPERS J2, J4, & J5
ARE TO USE 2732's



# PARTS LIST

| SEMICONDUCTOR | |
|---|---|
| U1 | 74LS04 |
| U2 | 74LS74 |
| U3 | 74LS157 |
| U4 | 74LS161/3 |
| U5 | 74LS10 |
| U6 | 74LS00 |
| U7 | 74LS165 |
| U8 | 74LS74 |
| U9 | 74LS11 |
| U10 | 74LS00 |
| U11 | 74LS21 |
| U12 | 74LS10 |
| U13 | 74LS33 |
| U14 | 74LS04 |
| U15 | 74LS02 |
| U16 | 74LS04 |
| U17 | 2716-32 |
| U18 | 2716-32 |
| U19 | 81LS95 |
| U20 | Z80B |
| U21 | 81LS96/98 |
| U22 | 74LS148 |
| U23 | 74LS273 |
| U24 | 74LS273 |
| U25 | 74LS125 |
| U26 | 74LS04 |
| U27 | 74LS02 |
| U28 | 74LS30 |
| U29 | 74LS266 |
| U30 | 74LS04 |
| U31 | 74LS04 |
| U32 | 74LS05 |
| U33 | 74LS32 |
| U34 | 74LS32 |
| U35 | 74LS244 |
| U36 | 74LS367 |
| U37 | 74LS367 |
| U38 | 74LS08 |
| U39 | 74LS244 |
| U40 | 74LS244 |
| U41 | 74LS244 |
| U42 | 81LS95 |
| U43 | 81LS95 |
| U44 | 74LS373 |
| U45 | 74LS373 |
| U46 | 74LS08 |
| U47 | 7805 |
| U48 | 7805 |

| RESISTOR | VALUE |
|---|---|
| R1 | |
| R2 | 1K ohm |
| R3 | 1K ohm |
| R4 | 120 ohm |
| R5 | 4.7K ohm |
| R6 | 150 ohm |
| R7 | 5.1K ohm SIP |
| R8 | 1.5K ohm |
| R9 | 4.7K ohm |
| R10 | 910 ohm |
| R11 | 33 ohm |
| R12 | 5.1K ohm SIP |
| R13 | 5.1K ohm SIP |
| R14 | 1K ohm |
| R15 | 1K ohm |
| R16 | 4.7K ohm |
| R17 | 4.7K ohm |
| R18 | 33 ohm |
| R19 | 4.7K ohm |
| R20-24 | 1.5K ohm |
| R25 | 1.5K ohm SIP |
| R26 | 1.5K ohm SIP |
| R27 | 4.7K ohm |
| R28 | 4.7K ohm |
| R29 | 390 ohm |

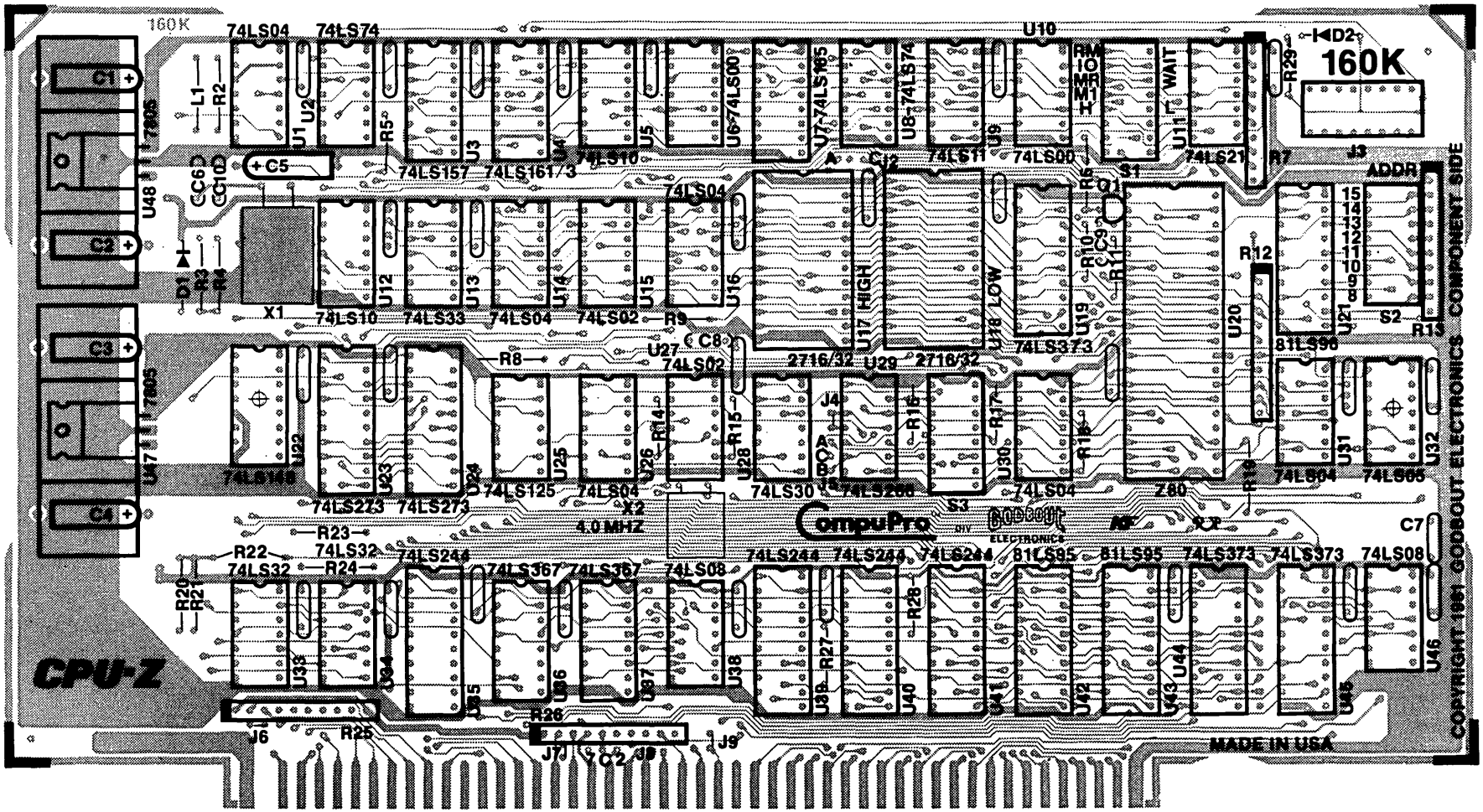
| CAPACITOR | VALUE |
|---|---|
| C1-5 | Tantalum Bypass |
| C6 | 62 pF |
| C7 | 390 pF |
| C8 | 0.01 uF |
| C9 | 43 pF |
| UNMARKED | 0.01 uF |

| INDUCTOR | |
|---|---|
| L1 | 1.0 uH |

| CRYSTAL | VALUE |
|---|---|
| X1 | 24 MHz |
| X2 | 4 MHz |

| DIODE | |
|---|---|
| D1-2 | Signal Diode |

| TRANSISTOR | |
|---|---|
| Q1 | 2N3906 |




COMPONENT LAYOUT

# LIMITED WARRANTY

COMPUPRO warrants this computer product to be in good working order for a period of one (1) year, (two [2] years CSC and six [6] months for disk drives) from the date of purchase by the original end user. Should this product fail to be in good working order at any time during this warranty period, COMPUPRO will, at its option, repair or replace the product at no additional charge except as set forth below. Repair parts and replacement products will be furnished on an exchange basis and will be either reconditioned or new. All replaced parts and products become the property of COMPUPRO. This limited warranty does not include service to repair damage to the product resulting from accident, disaster, misuse, abuse, or unauthorized modification of the product.

If you need assistance, or suspect an equipment failure, always contact your COMPUPRO System Center or dealer first. COMPUPRO System Center technicians are factory trained to provide prompt diagnosis and repair of equipment failures. If you prefer, or if you are not satisfied by the actions taken by your System Center/dealer, you may return the product to COMPUPRO for warranty service. Please call COMPUPRO at (415) 786-0909 to obtain a **R**eturn **M**aterial **A**uthorization (**RMA**) number, or, write to COMPUPRO at 3481 Arden Road, Hayward, California 94545, Attn.: RMA. Be sure to include a copy of the original bill of sale to establish purchase date. If the product is delivered by mail or common carrier, you agree to insure the product or assume the risk of loss or damage in transit, to prepay shipping charges to the warranty service location (System Center or COMPUPRO) and to use the original shipping container or equivalent. Contact your COMPUPRO System Center/dealer or write to COMPUPRO at the above address for further information.

ALL EXPRESS AND IMPLIED WARRANTIES FOR THIS PRODUCT, INCLUDING THE WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, ARE LIMITED IN DURATION TO A PERIOD OF ONE (1) YEAR FROM THE DATE OF PURCHASE, AND NO WARRANTIES, WHETHER EXPRESS OR IMPLIED, WILL APPLY AFTER THIS PERIOD. SOME STATES DO NOT ALLOW LIMITATIONS ON HOW LONG AN IMPLIED WARRANTY LASTS, SO THE ABOVE LIMITATIONS MAY NOT APPLY TO YOU.

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**COMPUPRO**
**3481 Arden Road**
**Hayward, CA 94545**
**(415) 786-0909**

Note: This warranty supersedes all previous warranties, and all other warranties are now obsolete.