REV	DESCRIPTION	DR	CH	DATE	APPROVAL
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[illegible]	IN[illegible] PER EN [illegible]	[illegible]	[illegible]	12-7-7?	[illegible]
[illegible]	INCORP PER EN 6[illegible]	[illegible]			
[illegible]	INCORP PER EN [illegible]	[illegible]			
4	INCORP PER EN [illegible]	[illegible]			
[illegible]	INCORP PER EN C7[illegible]	[illegible]			
EG	INCORP PER EN C55?H	[illegible]	[illegible]	12-7-78	[illegible]

P1	SIGNAL	DIRECTION	LOCATION
PIN 101	GND	←	C15
102	GND	←	C15
103	+12V	←	D15
104	+12V	←	D15
105	+12V	←	C15
106	+12V	←	C15
107	-12V	←	C15
108	-12V	←	C15
109	D PIN	←	A38
110	D PØT	→	A38
111		NU	
112		NU	
113	+5V	←	C15
114	+5V	←	C15
115	MST	←	A19
116		NU	
117	MACK	←	A19
118	RD	←	D40
119	EBA	←	A23
120	SLB	←	A38
121	PFD	NU	
122	MDIS	←	B19
123	AB08	↕	C38
124	AB09	↕	C38
125	AB10	↕	A24
126	AB11	↕	A24
127	GND	↕	C15
128	GND	↕	C15
129	AB12	↕	B24
130	AB13	↕	B24
131	AB14	↕	A24
132	AB15	←	A38
133		NU	
134		NU	
135	STØP	NU	
136	SACK	←	A88
137	MBIN	←	A38
138	MBØT	→	A38
139	DB00	↔	D79
140	DB01	↕	D79
141	DB02	↕	C79
142	DB03	↔	C79
PIN 143	+5V	←	C15

P1	SIGNAL	DIRECTION	LOCATION
PIN 144	+5V	←	C15
145	DB04	↔	D76
146	DB05	↕	D76
147	DB06	↕	C76
148	DB07	↔	C76
149	DB08	NU	
150	DB09	↕	
151	DB10	↕	
152	DB11	↕	
153	DB12	↕	
154	DB13	↕	
155	DB14	↕	
156	DB15	↕	
157	EXEC	↕	
158	IN	NU	
159	GND	←	C15
160	GND	←	C15
161	IØCL	NU	
162	OUT	NU	
163	CLK	←	C22
164	SER	NU	
165	IUR	→	C19
166	ILI	→	B82
167	IAR	NU	
168	IL2	NU	
169	RST	←	A85
170	IUA	NU	
171	PLSE	←	B85
172	ECHØ	NU	
173	+5V	←	C15
174	+5V	↕	C15
175	AB03	↕	A40
176	AB04	↕	A40
177	AB05	↕	B40
178	AB06	↕	B40
179	AB07	↕	B40
180	AB00	↕	D19
181	AB01	↕	C40
182	AB02	↕	C40
183	PRIN	←	D22
184	PRØT	→	D22
185	GND	←	C15
PIN 186	GND	←	C15

P2	SIGNAL	DIRECTION	LOCATION
PIN 201	GND	←	B15
202	GND	←	B15
203	+12V	NU	
204	+12V	↕	
205	+12V	↕	
206	+12V	NU	
207	-12V	←	C15
208	-12V	←	C15
209	DPIN	←	D22
210	DPØT	→	D22
211	EBSEL	NU	
212		NU	
213	+5V	←	B15
214	+5V	←	B15
215	MST	NU	
216		NU	
217	MACK	→	B27
218	RD	NU	
219	FCLK	↕	
220	SLB	↕	
221	PFD	NU	
222	MDIS	←	B35
223	AB08	NU	
224	AB09	↕	
225	AB10	↕	
226	AB11	NU	
227	GND	←	B15
228	GND	←	B15
229	AB12	NU	
230	AB13	↕	
231	AB14	↕	
232	AB15	NU	
233	DB16	↔	B86
234	DB17	↔	B86
235	STOP	NU	
236	SACK	NU	
237	MBIN	←	C19
238	MBØT	→	C19
239	DB00	↔	C79
240	DB01	↕	C79
241	DB02	↕	B79
242	DB03	↔	B79
PIN 243	+5V	←	B15

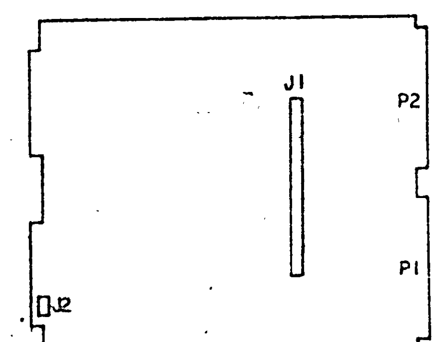
P2	SIGNAL	DIRECTION	LOCATION
PIN 244	+5V	←	B15
245	DB04	↔	C77
246	DB05	↕	C77
247	DB06	↕	C77
248	DB07	↕	B77
249	DB08	↕	B79
250	DB09	↕	B79
251	DB10	↕	B79
252	DB11	↕	A79
253	DB12	↕	B76
254	DB13	↕	B76
255	DB14	↕	B76
256	DB15	↔	A76
257	EXEC	NU	
258	IN	NU	
259	GND	←	B15
260	GND	←	B15
261	IØCL	NU	
262	OUT	↕	
263	CLK	↕	
264	SER	↕	
265	IUR	↕	
266	ILI	NU	
267	IAR	←	A85
268	IL2	NU	
269	RST	↕	
270	IUA	↕	
271	PLSE	↕	
272	ECHØ	NU	
273	+5V	←	B15
274	+5V	←	B15
275	AB03	NU	
276	AB04	NU	
277	AB05	NU	
278	AB06	←	C56
279	AB07	←	B56
280	AB00	NU	
281	AB01	←	C48
282	AB02	←	C48
283	PRIN	←	D22
284	PRØT	→	D22
285	GND	←	B15
PIN 286	GND	←	B15

J2	SIGNAL	DIRECTION	LOCATION
PIN 1	NU		
2	NU		
3	LO	→	A36
4	HI	→	A36
5	INTER	←	C23
6	ØOD	←	C23
7	E.LOW	←	B23
8	E.HIGH	←	B23
9	GND	←	C23
10	GND	←	B23
11	GND	←	B23
12	GND	←	C23
13	NU		
14	↕		
15	↕		
PIN 16	NU		

(12)

OPTION BLOCK

DASH NO.	COMPONENT OPTION C64-81	COMPONENT OPTION R40-57	JUMPER WIRE OPTION
-04	NOTUSED	12 OHM	W1, W5
-08	2700PF,10%,200V	10 OHM	W1, W5
-14	NOTUSED	12 OHM	W1, W2, W3, W5
-18	2700PF,10%,200V	10 OHM	W1, W2, W3, W5
-24	NOTUSED	12 OHM	W1, W2, W3, W4, W5
-28	2700PF,10%,200V	10 OHM	W1, W2, W3, W4, W5



TABULATION BLOCK

DASH NO.	DESCRIPTION
-04	4K X 16
-14	4K X 18+PARITY
-08	8K X 16
-18	8K X 18+PARITY
-24	4K+DMA+PARITY
-28	8K+DMA+PARITY

(13) ○ DENOTES COMMON FUNCTION AND COMMON PIN CONNECTIONS OF MULTI-ELEMENT DEVICES.

(12) FOR COMPONENT AND JUMPER WIRE OPTION SEE OPTION BLOCK

11. RP11-16, 19, ARE 75±2%, 1/8W
10. ALL RESISTOR PACKS ARE ±5%, 1/8W
9. ALL 6.8UF CAPACITORS ARE ±20%, 20V
8. ALL 2.2UF CAPACITORS ARE ±10%, 20V
7. ALL .022UF CAPACITOR ARE +80% -20%, 50V
6. ALL CAPACITOR VALUES ARE IN UF
5. ALL DIODES ARE IN4448
4. ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W
3. SIGNALS MARKED → ARE OUTGOING
2. SIGNALS MARKED ← ARE INCOMING
1. FOR LOGIC DRAWING NO. SEE TABULATION BLOCK.

NOTES: UNLESS OTHERWISE SPECIFIED

UNUSED GATES/IC

REF.DEG.	IC TYPE	UNUSED PINS IN	UNUSED PINS OUT
6	74S00	1,2	3
108	849	9,10	8
100	849	12,13	11
42	74S04	1	2
17	7438	9,10	8

-31

NOTES UNLESS SPECIFIED
1. TOLERANCES .XX ±.03 .XXX ±.010 ANGULAR ±½°
2. BREAK ALL SHARP EDGES .010 APPROX.
3. ALL DIM. IN INCHES

DASH NO.	NEXT ASSEMBLYS

DR. E.ZURAW [illegible]
CHK. DM [illegible]
DSG. E.ZURAW [illegible]
ENGR. [illegible]

COMPUTER AUTOMATION INC.

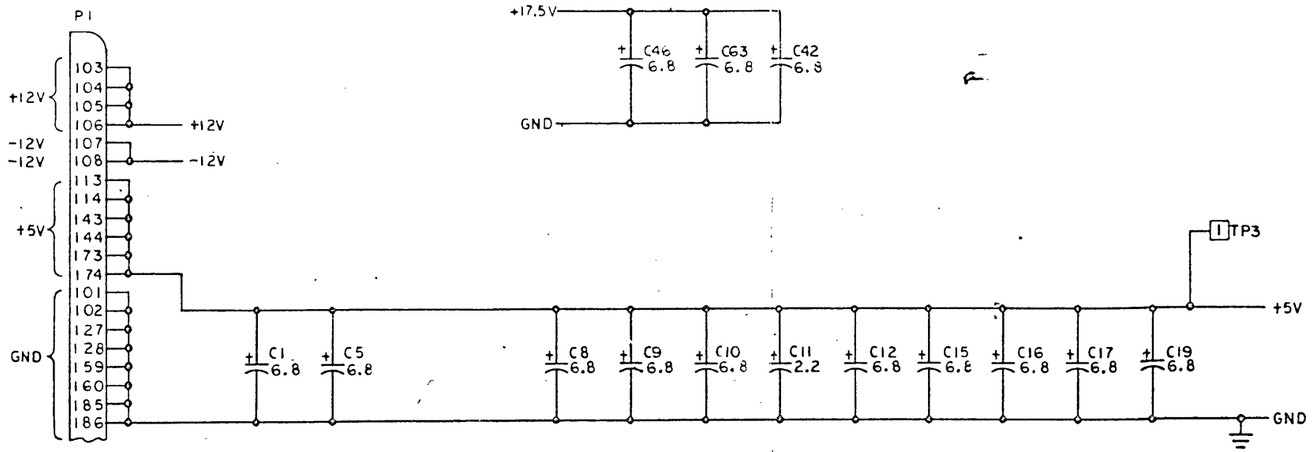
TITLE: LOGIC DIAGRAM, CORE MEMORY

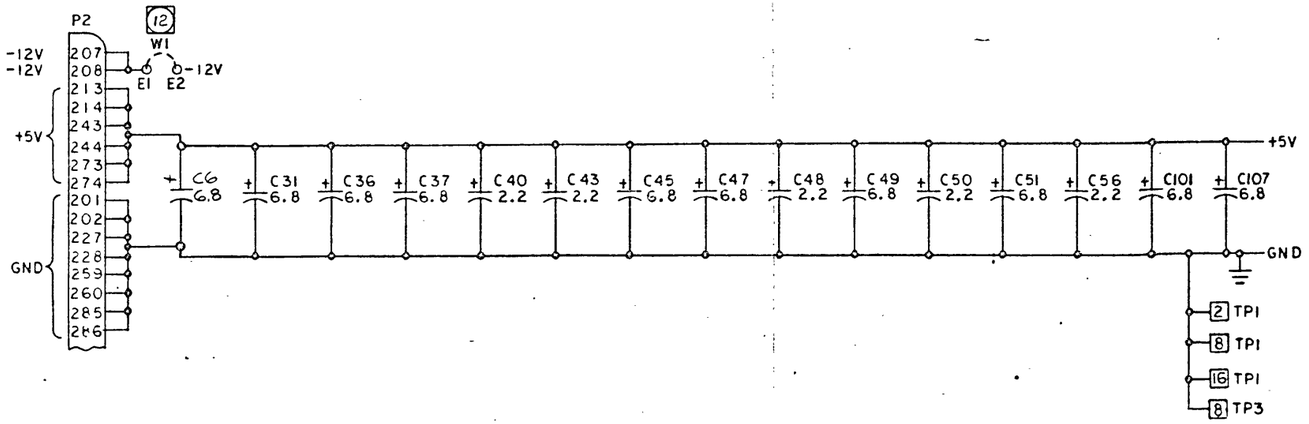
SIZE D | DWG. NO. 75-53677-XX | REV EG

DO NOT SCALE DRAWING | SCALE = NONE | SHT. 1 OF 12

REVISIONS

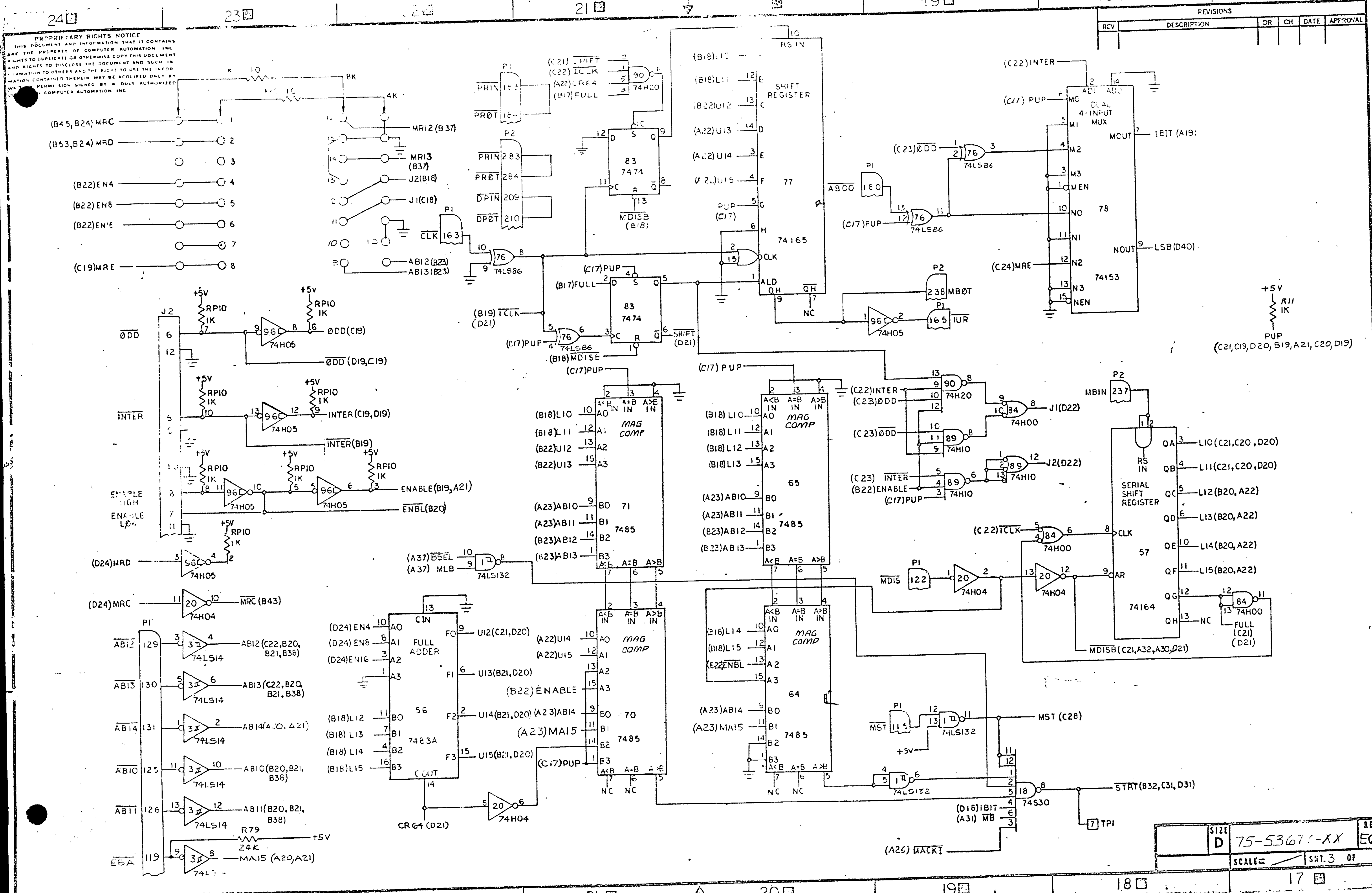
REV	DESCRIPTION	DR	CH	DATE	APPROVAL





SIZE		DEV
D	75-53677-XX	E6
SCALE=		SHT. 2 OF

75-53677-XX



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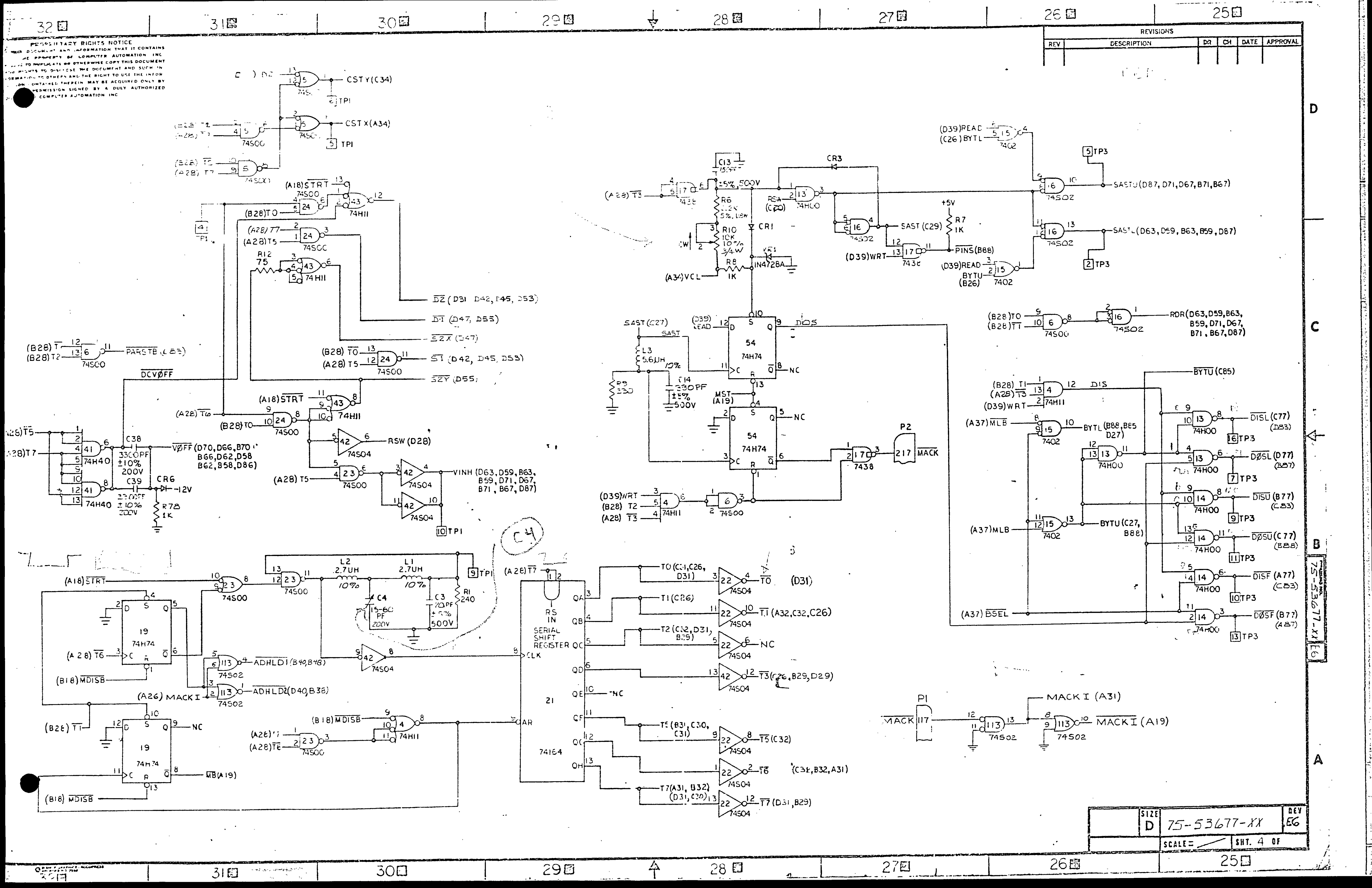
REVISIONS
REV
DESCRIPTION
DR
CH
DATE
APPROVAL
SHIFT REGISTER
74165
DUAL 4-INPUT MUX
74153
MAG COMP
7485
FULL ADDER
7483A
SERIAL SHIFT REGISTER
74164
74H05
74LS86
74H20
74H00
74H10
74H04
74LS14
74LS132
74S30
7474
ENABLE HIGH
ENABLE LOW
START (B32, C31, D31)
MST (C28)
TPI
SIZE D
75-5367?-XX
REV E6
SCALE
SHT. 3 OF



32
31
30
29
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26
25
PROPRIETARY RIGHTS NOTICE
REVISIONS
REV
DESCRIPTION
DR
CH
DATE
APPROVAL
CSTY(C34)
CSTX(A34)
TP1
74S00
74H11
74H40
74H74
74S04
74S02
74H00
7402
7438
74164
DZ (D31 D42, D45, D53)
DI (D47, D55)
SZX (D47)
SI (D42, D45, D53)
SZY (D55)
PARSTB (C83)
DCVØFF
VØFF (D70, D66, B70, B66, D62, D58, B62, B58, D86)
RSW (D28)
VINH (D63, D59, B63, B59, D71, D67, B71, B67, D87)
CR3
CR1
CR6
IN4726A
(A34) VCL
SAST (C29)
PINS (B88)
SASTU (D87, D71, D67, B71, B67)
SASTL (D63, D59, B63, B59, D87)
RDR (D63, D59, B63, B59, D71, D67, B71, B67, D87)
TP3
DOS
MACK
P2
BYTU (C85)
DIS
BYTL (B88, B65, D27)
BYTU (C27, B88)
DISL (C77)
DØSL (D77)
DISU (B77)
DØSU (C77)
DISF (A77)
DØSF (B77)
(A37) BSEL
(A37) MLB
SERIAL SHIFT REGISTER
RS IN
CLK
CLR
T0 (C31, C26, D31)
T1 (C26)
T1 (A32, C32, C26)
T2 (C32, D31, B29)
T3 (C26, B29, D29)
T5 (B31, C30, C31)
T5 (C32)
T6 (C32, B32, A31)
T7 (A31, B32) (D31, C30)
T7 (D31, B29)
NC
ADHLD1 (B40, B48)
ADHLD2 (D40, B38)
(A26) MACK I
MB (A19)
(B18) MDISB
MACK I (A31)
MACK I (A19)
P1
A
B
C
D
SIZE
D
75-53677-XX
REV
E6
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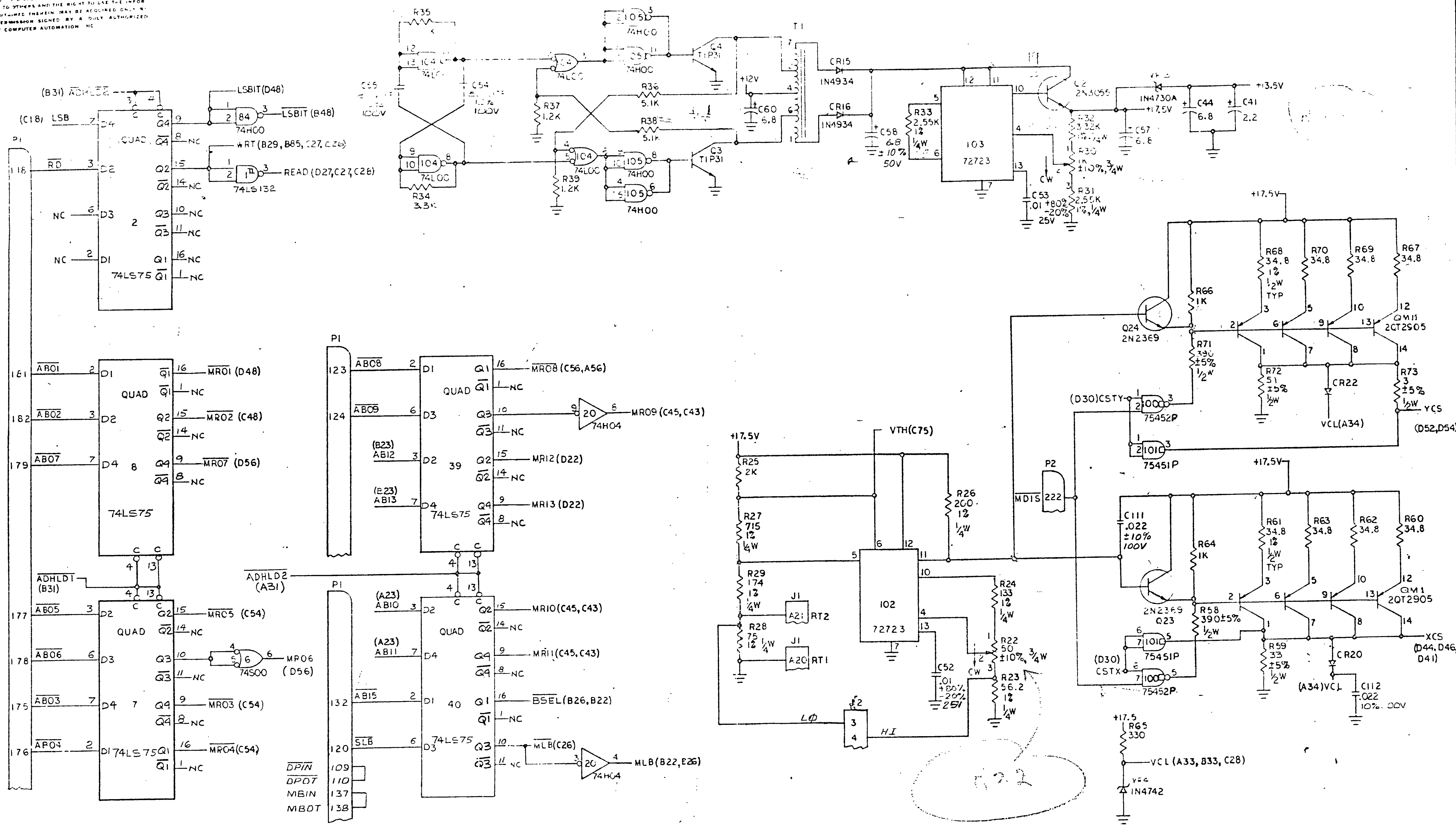
REVISIONS					
REV	DESCRIPTION	DR	CH	DATE	APPROVAL



D C B A

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SCALE =	SHT. 5 OF	

REVISIONS					
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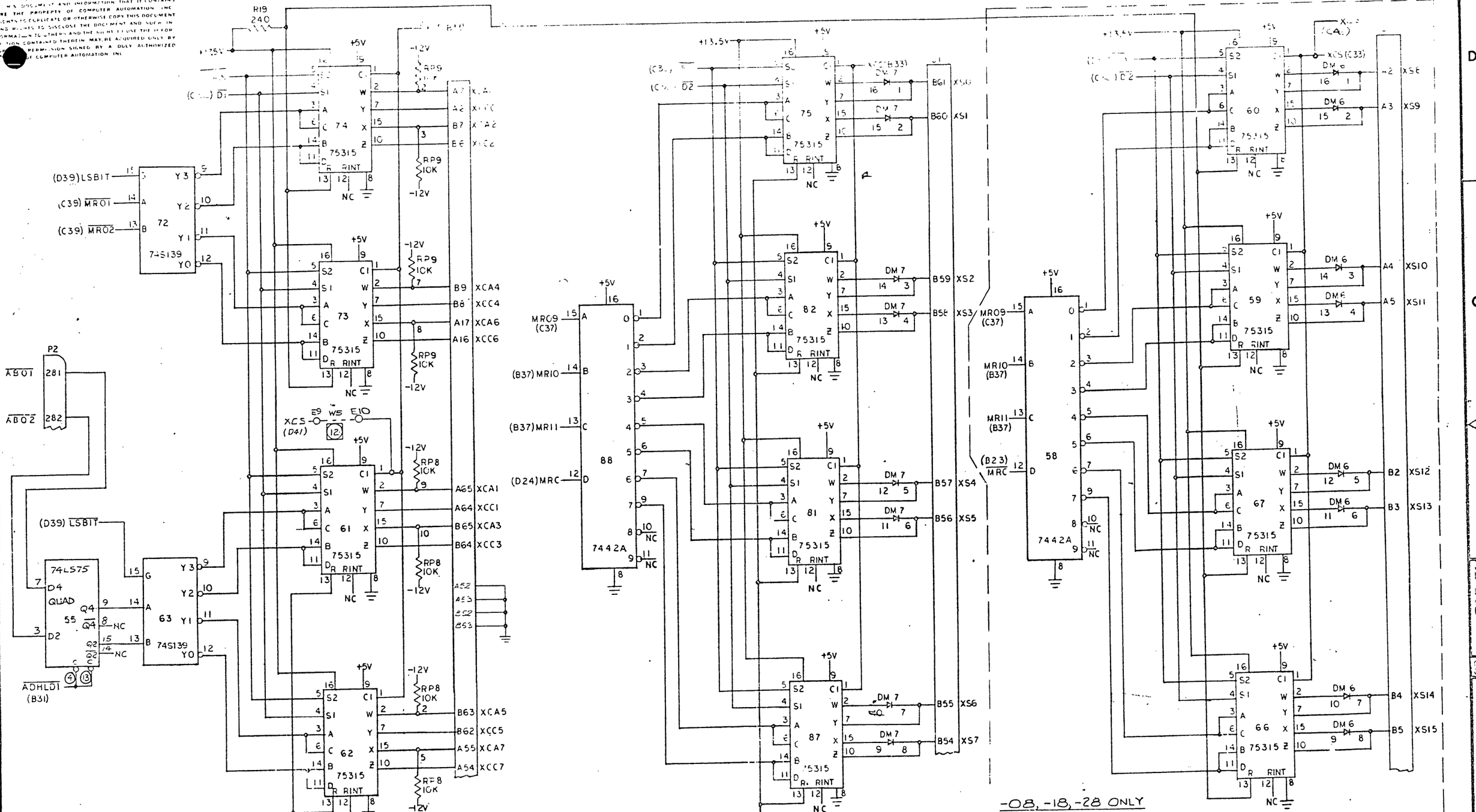

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REVISIONS					
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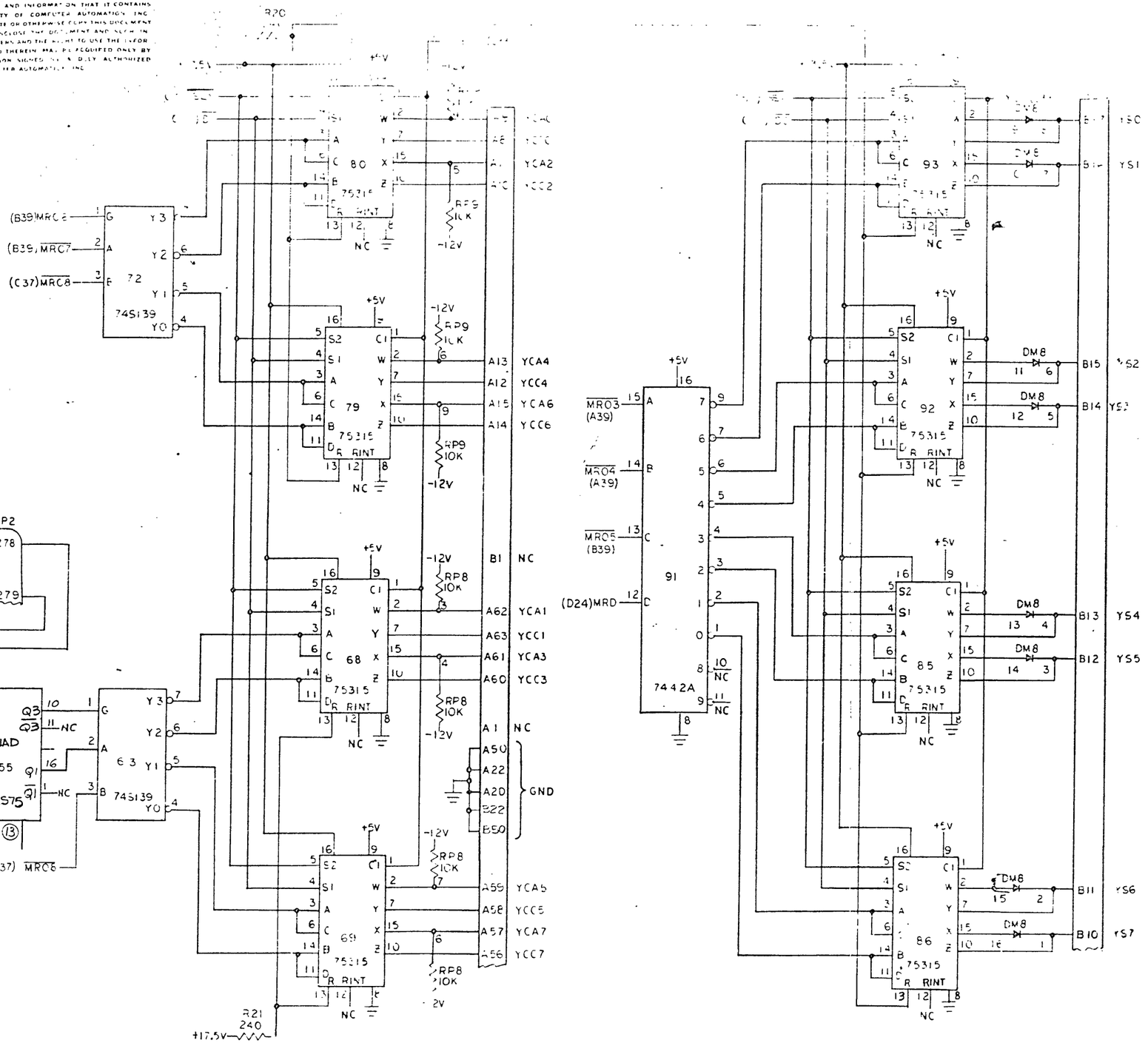

SIZE		REV
D	75-53677-XX	EG
SCALE=	SHT. 7 OF	

DRAWING NO. 75-53677-XX REV EG

REVISIONS					
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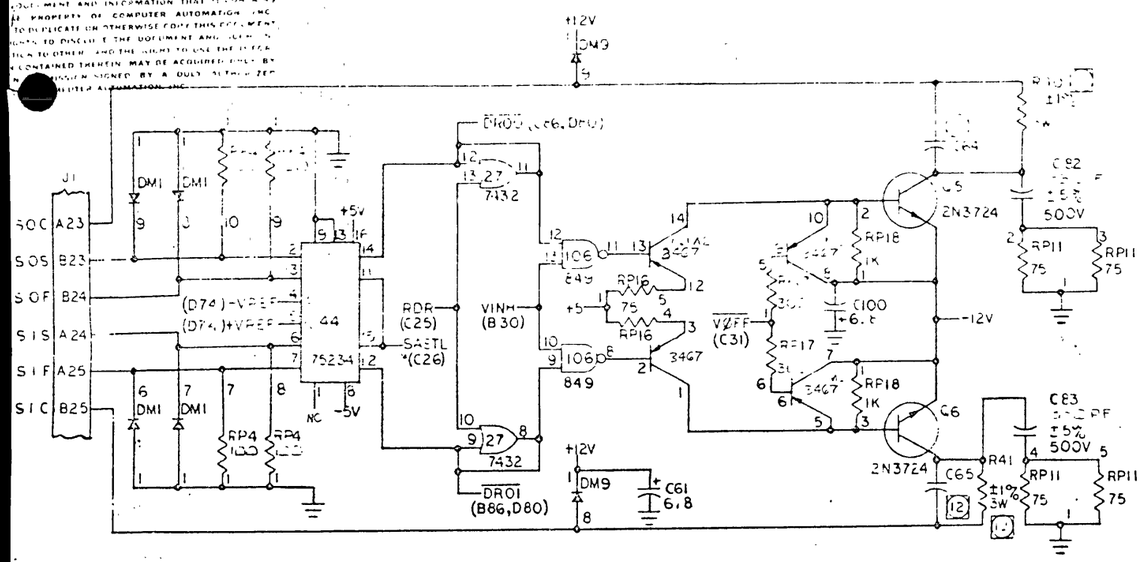

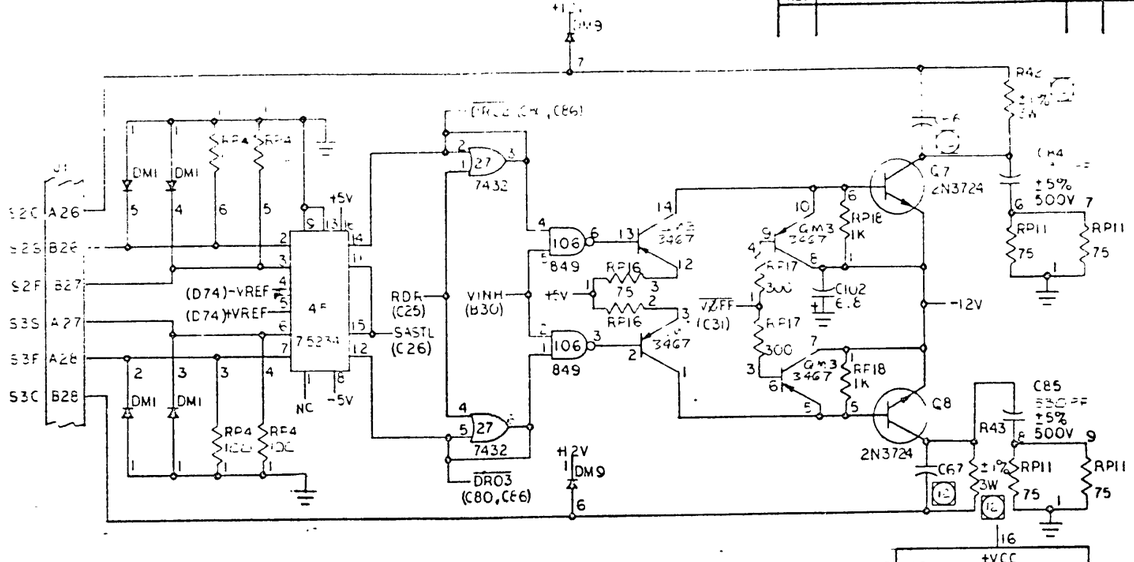

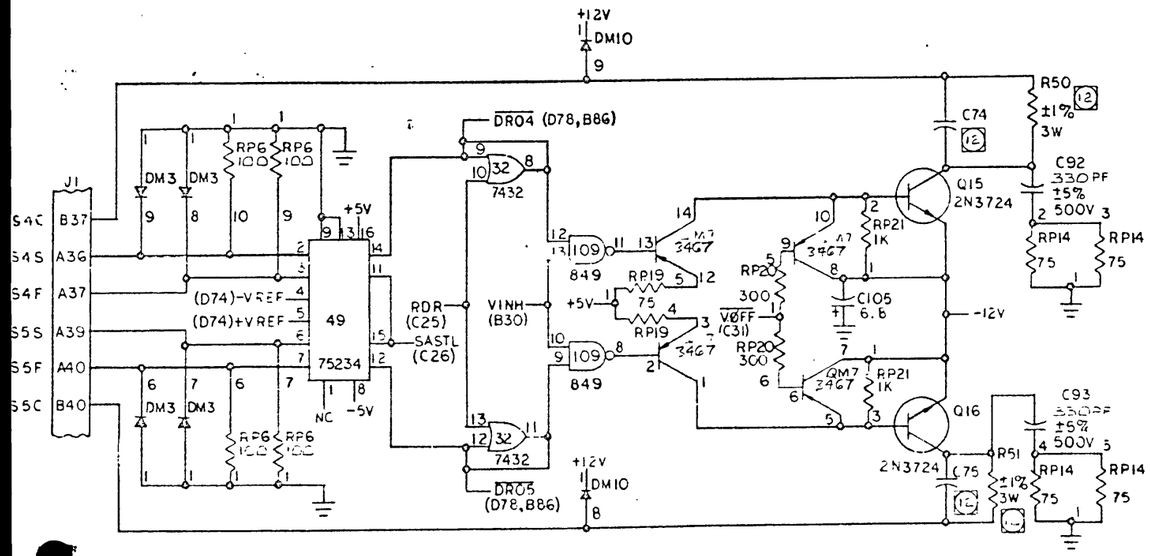

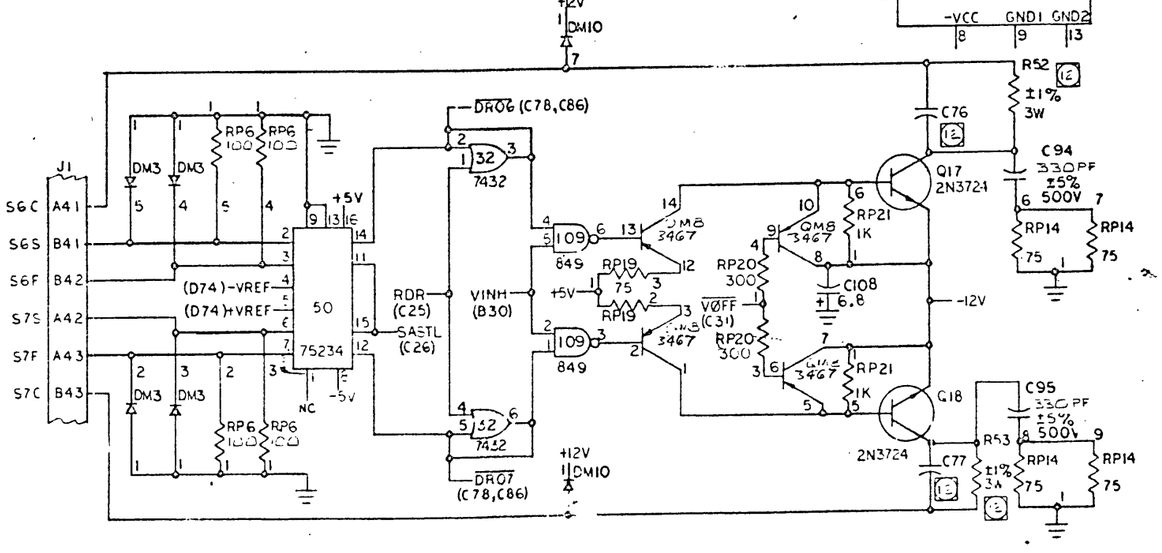

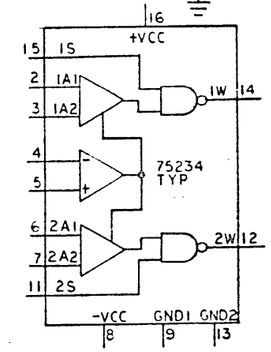

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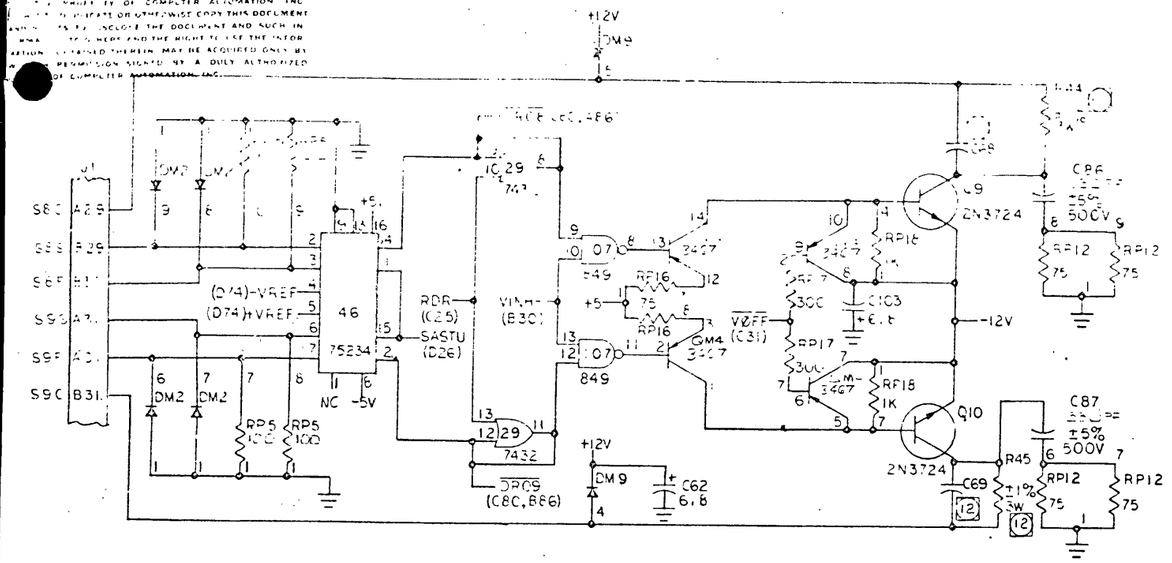
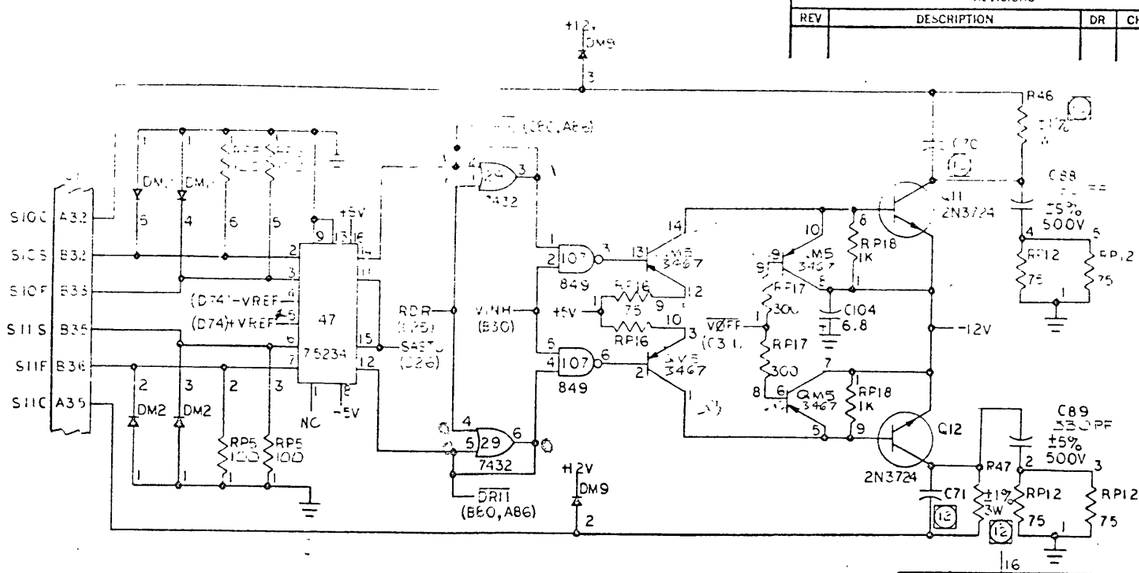
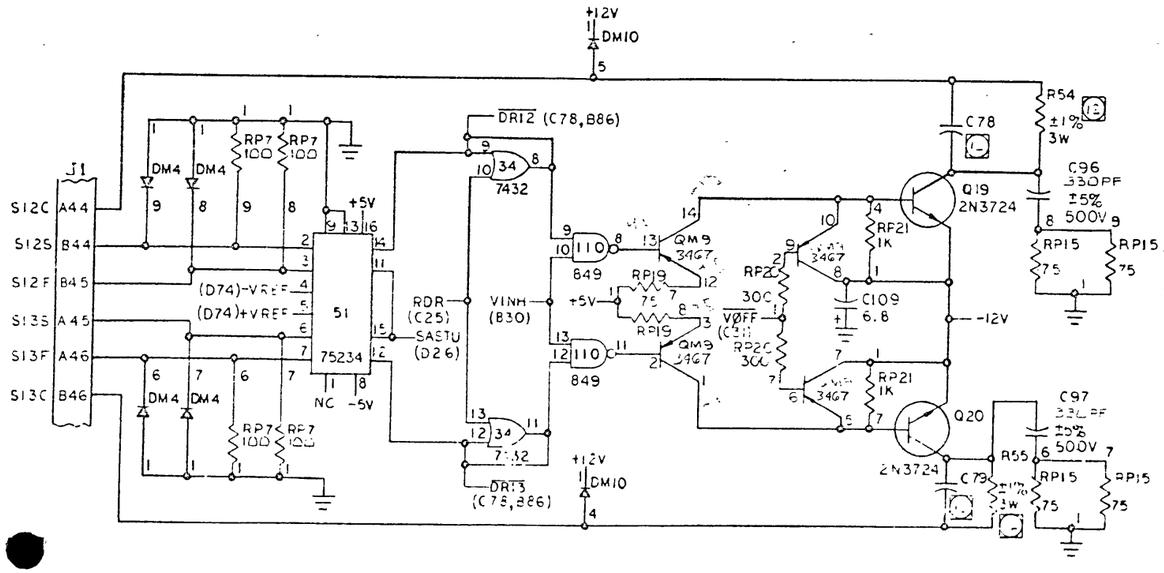
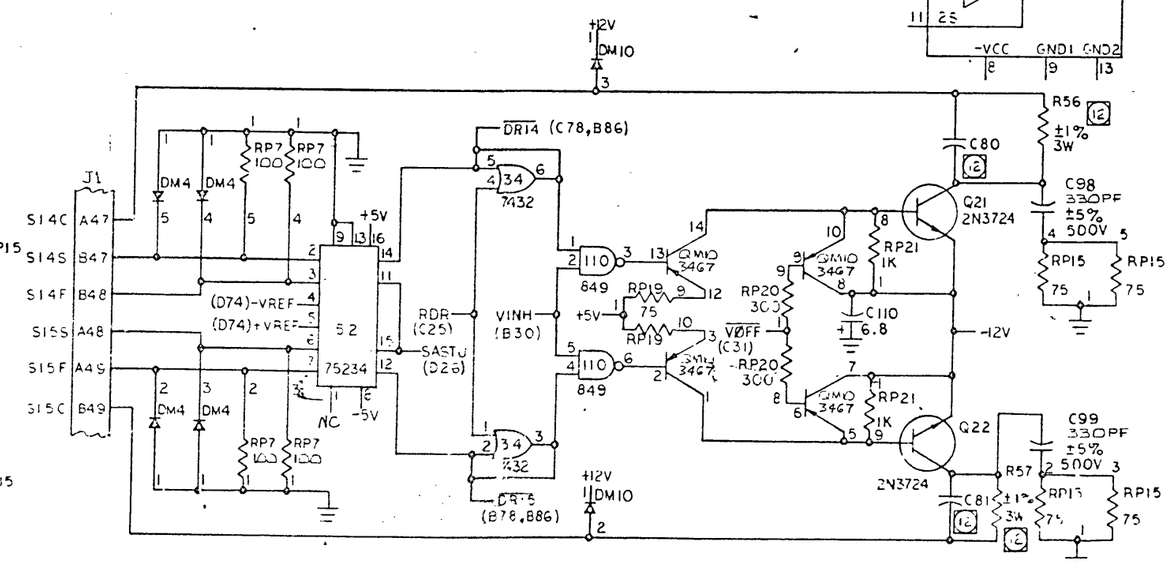
		SCALE=	SHT. 8 OF

REVISIONS					
REV	DESCRIPTION	DR	CH	DATE	APPROVAL









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REVISIONS					
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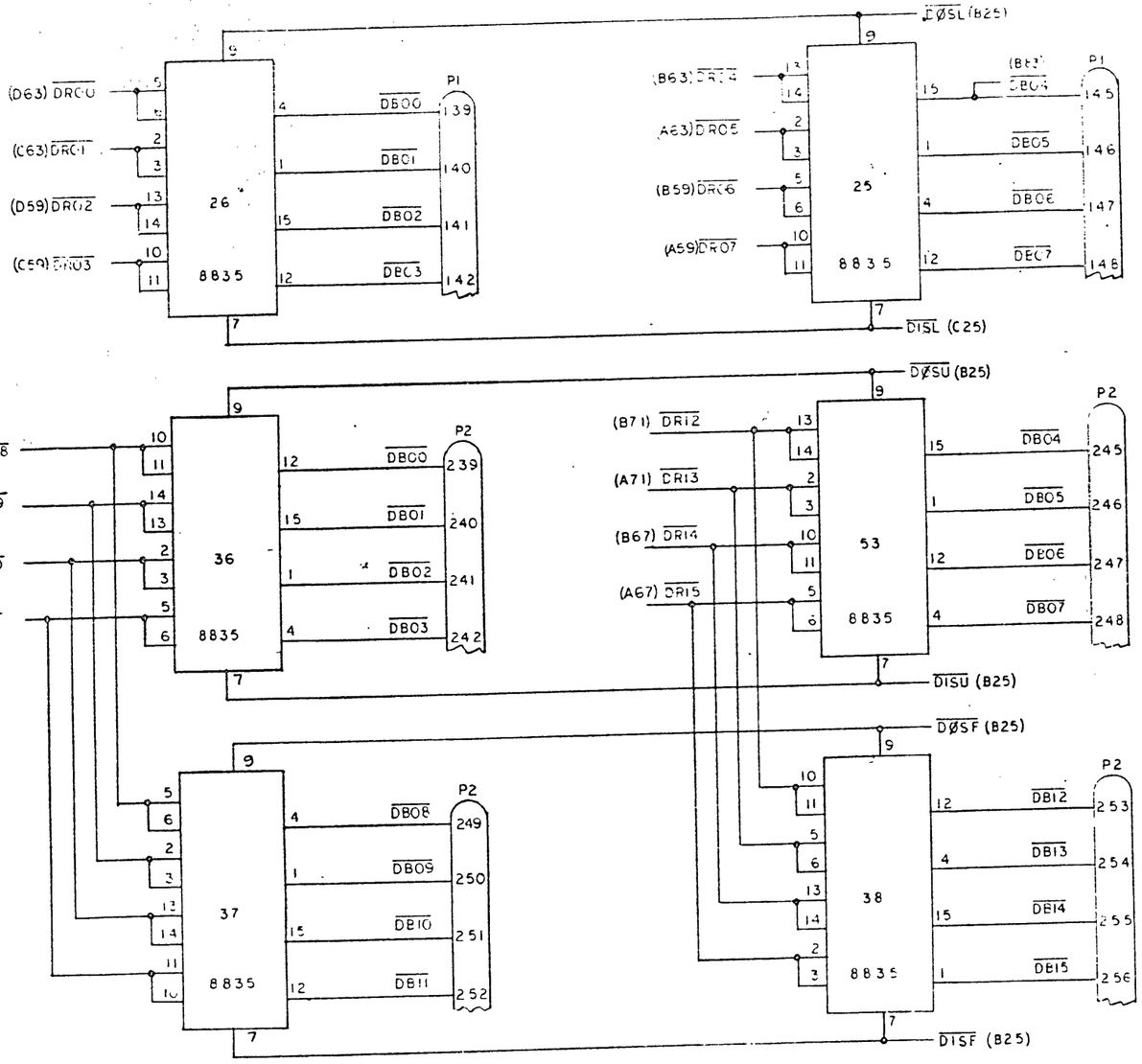

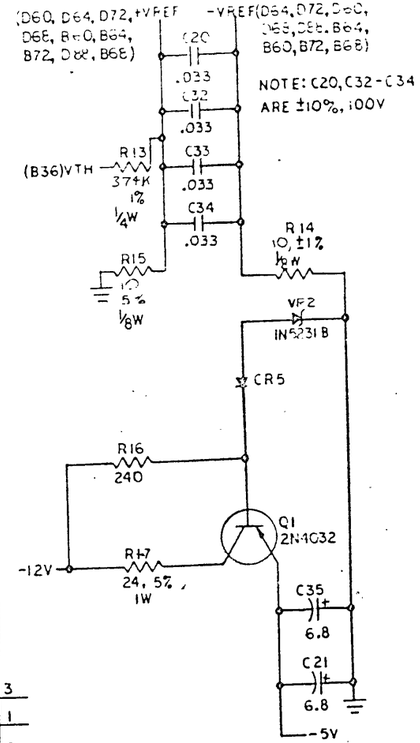

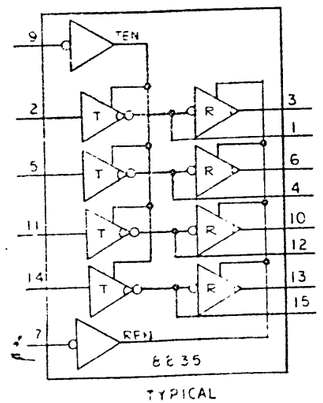

TYPICAL

SIZE		REV
D	75-53677-XX	E6
SCALE=	SHT. 10 OF	

REVISIONS

REV	DESCRIPTION	DR	CH	DATE	APPROVAL

PARITY OPTION

-24 AND -28 ONLY

SIZE		REV
D	75-53677-XX	E6
SCALE=	SHT. 11 OF	

AB00- to AB14-	ADDRESS INPUTS FROM BUSS
AB15-	BYTE MODE SELECT FROM BUSS
ABUL-	ADDRESS GREATER OR EQUAL TO UPPER LIMIT, INHIBITS MEMORY ACCESS WHEN ACTIVE
ABLL-	ADDRESS LESS THAN LOWER LIMIT, INHIBITS MEMORY ACCESS WHEN ACTIVE
ADHLD-	ADDRESS HOLD, LATCHES ADDRESS REGISTERS WHEN ACTIVE
BSEL	BYTE SELECT, INDICATES MEMORY IS IN BYTE MODE. SIGNAL IS LATCHED AB15-.
BUSY-	INDICATES MEMORY OPERATION IN PROGRESS IN 18BITS ACCESS
BYTU	BYTE UPPER, INDICATES BYTE MODE AND UPPER BYTE IS ACCESSED
BYTL	BYTE LOWER, INDICATES LOWER BYTE IS ACCESSED
CLKP-	PROCESSOR GENERATED CLOCK DRIVES THE SHIFT REGISTERS WHICH SHIFT MBIN IN AND MBOT OUT
CSTX	X CURRENT SOURCE TIMING
CSTY	Y CURRENT SOURCE TIMING
D1	READ DRIVER TIMING
D2	READ SINK TIMING
DB00- to DB18-	DATA INPUT AND OUTPUT FROM DATA BUSS
DISF-	ENABLES THE DATA TRANSCEIVERS TO TRANSMIT DATA FROM THE LOWER BYTE OF THE DATA BUSS TO THE UPPER BYTE OF MEMORY
DISL-	ENABLES THE DATA TRANSCEIVERS TO TRANSMIT DATA FROM THE LOWER BYTE OF THE DATA BUSS TO THE LOWER BYTE OF MEMORY
DISU-	ENABLES THE DATA TRANSCEIVERS TO TRANSMIT DATA FROM THE LOWER BYTE OF THE DATA BUSS TO THE UPPER BYTE OF MEMORY
DOS	DATA OUT STROBE TIMING SIGNAL GENERATED TO STROBE DATA FROM THE MEMORY
DOSF-	ENABLES THE DATA TRANSCEIVERS TO TRANSMIT DATA FROM THE UPPER BYTE OF MEMORY TO THE UPPER BYTE OF THE DATA BUSS
DOSL-	ENABLES THE DATA TRANSCEIVERS TO TRANSMIT DATA FROM THE UPPER BYTE OF MEMORY TO THE UPPER BYTE OF THE DATA BUSS
DOSU-	ENABLES DATA TRANSCEIVERS TO TRANSMIT DATA FROM THE UPPER BYTE OF MEMORY TO THE LOWER BYTE OF THE DATA BUSS
DPIN- and DPOT-	THESE LINES FOR A DMA PRIORITY CHAIN WHICH IS STRUNG SERIALLY THROUGH ALL DMA CONTROLLERS AND MEMORIES. THE MEMORY DOES NOT USE THESE LINES BUT SIMPLY PASSES THE SIGNAL FROM DPIN- TO DPOT-
DR00- to DR18-	DATA REGISTER HOLDS DATA FROM THE SENSE AMPLIFIER OR FROM THE TRANSCEIVER
EBA	EXTA BIT OF ADDRESS USED TO ALLOCATE 64K ADDRESSES
ENABLE HIGH	SIGNAL USED FOR MEMORY BANKING WILL DISABLE THE MEMORY WHEN LOW
ENABLE LOW	SIGNAL USED FOR MEMORY BANKING WILL DISABLE MEMORY WHEN HIGH
EN16	ENABLES AUTOMATIC ADDRESS ALLOCATION AS A 16K MEMORY
EN8	ENABLES AUTOMATIC ADDRESS ALLOCATION AS AN 8K MEMORY
EN4	ENABLES AUTOMATIC ADDRESS ALLOCATION AS A 4K MEMORY
J1	THIS SIGNAL USED TO CREATE THE EN SIGNALS IS NORMALLY LOW
J2	THIS SIGNAL USED TO CREATE THE EN SIGNALS IS NORMALLY HIGH
IBIT	INHIBIT BIT USED TO INHIBIT MEMORY OPERATION IN INTERLEAVED MODE WITH THE LSB.
INTER-	INTERLEAVE, USED TO SELECT INTERLEAVE MODE WHEN LOW
IUR	INTERRUPT REQUEST, MEMORY SIGNAL IS INVERSE OF MBOT
L10-L15	LOWER LIMIT OF ADDRESSES USED TO ESTABLISH ADDRESS ALLOCATION
LSB	LEAST SIGNIFICANT BIT FOR DRIVE DECODING
MA15	INVERTED EBA USED FOR ADDRESSING TO 64K
IUR-	INTERRUPT REQUEST, MEMORY SIGNAL IS INVERSE OF MBOT
MACK-	MEMORY ACKNOWLEDGE IS A MEMORY GENERATED SIGNAL THAT IS USED TO INFORM THE PROCESSOR OR DMA CONTROLLER THAT DATA IS AVAILABLE DURING A READ OPERATION OR THAT DATA HAS BEEN ACCEPTED DURING A WRITE OPERATION
MBIN	MEMORY BOUNDARY IS IS THE LINE UPON WHICH THE MEMORY RECEIVES ITS LOWER LIMIT UPON POWER UP
MBOT	MEMORY BOUNDARY OUT IS THE LINE UPON WHICH THE MEMORY MODULE TRANSMITS ITS UPPER BOUNDARY TO THE NEXT MEMORY, WHICH BECOMES THIS MEMORY'S LOWER BOUNDARY.
MDIS-	MEMORY DISABLE IS A SIGNAL BY WHICH THE PROCESSOR KEEPS THE MEMORIES FROM RESPONDING TO NOISE DURING PERIODS OF POWER TRANSMITION. THIS LINE IS ALSO USED TO RESET VARIOUS SHIFT REGISTERS AND FLIP-FLOPS UPON POWER UP.
MDISB-	MDIS BUFFERED
MLB-	LATCHED SLB
MR01 to MR13	ADDRESS REGISTER FOR AB9 - 11
MRC, MRD, MRE	SIGNALS USED FOR DRIVE DECODING
MST-	MEMORY START IS A PROCESSOR OR DMA CONTROLLER GENERATED SIGNAL WHICH IS USED TO INITIATE A MEMORY CYCLE.
PRIN- and PROT-	PRIORITY IN AND PRIORITY OUT. THESE LINES FORM AN INTERRUPT PRIORITY CHAIN WHICH IS STRUNG SERIALLY THROUGH ALL INTERFACE CONTROLLERS AND MEMORIES. THE MEMORY DOES NOT USE THESE LINES, BUT SIMPLY PASSES THE SIGNAL FROM PRIN- TO PROT-.
RDR	DATA REGISTER RESET, RESETS ALL DATA REGISTERS AT THE START OF A MEMORY CYCLE
S1	DRIVE SINK TIMING
S2Y	DRIVE TIMING
SASTU	SENSE AMP STROBE UPPER BYTE
SASTL	SENSE AMP STROBE LOWER BYTE
STRT-	SIGNAL INDICATING MST- HAS STARTED MEMORY CYCLE
T0 to T7	TIMING SIGNALS FROM SHIFT REGISTER
TEMPA, B	CORE STACK THERMISTOR OUTPUTS USED TO REGULATE CURRENT SOURCE
VINH	INHIBIT DRIVER TIMING
VOFF	INHIBIT DRIVER OFF TIMING
VTH	REFERENCE VOLTAGE
XS0 to XS15	X CURRENT SINK CONNECTION TO CORE PLANE
YCA0 to YCA7	Y COMMON ANODE CONNECTION TO CORE PLANE
YCC0 to YCC7	Y COMMON CATHODE CONNECTION TO CORE PLANE
YS0 to YS 7	Y CURRENT SINK CONNECTION TO CORE PLANE