HSD-140

Technical Reference Manual

—NOTE—

This equipment generates, uses, and can radiate radio frequency energy. If not installed and used in accordance with the installation instructions, it may interfere with radio communications. The equipment has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference, which users may be required to correct at their own expense.

Peripheral cables must be shielded in order to meet FCC and VDE emission standards and to prevent damage to the hardware from static electricity. Always use Convergent cables or equivalent shielded cables with this equipment. Cables and terminators of an inferior design may not provide the proper shielding.

Specifications Subject to Change.

First Edition (May 1988) 09—01392—01

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ABOUT THIS MANUAL

This manual describes the HSD-140 SCSI (Small Computer System Interface) Upgrade module. It is a companion manual to the SCSI Upgrades and Expansions manual, which provides information common to all SCSI device modules. This information includes host systems, configuration, installation, the physical SCSI interface, and the firmware SCSI interface (the Common Command Set).

This manual contains information specific to the HSD-140 SCSI Upgrade Module, and can be ordered separately. If you do so, you may want to place it in the same binder that you use for the SCSI Upgrades and Exansions manual.

CONVENTIONS

This section describes conventions for numbers, signal names, and special terminology.

NUMBERS

Numbers in this manual are decimal unless suffixed as follows:

- An "h" represents hexadecimal notation, for example, 15h = 21 decimal, and 0F4h = 244 decimal.
- A "B" represents binary notation, for example, 011B = 3 decimal, and 1101B = 13 decimal.

SIGNAL NAMES

In this manual, active-low signals are suffixed with a minus sign (-). Active-high signals are not suffixed. Examples of an active-high signal and an active-low signal follow:

Signal Name	Logical State	Voltage Level
RD-	0 (active)	Low
	1 (inactive)	High
RD	0 (inactive)	Low
	1 (active)	High

TERMINOLOGY

This section defines the way the manual uses the terms controller, SCSI device, SCSI Expansion, SCSI Upgrade, HSX module, and HSD module. See the SCSI Upgrades and Expansions glossary for more definitions.

Controller

In this manual, the term **controller** means the host adapter. Controller always refers to the controller for the SCSI interface. Control circuitry within the SCSI device unit is transparent to the system and is not discussed in this manual.

SCSI Device

A SCSI device is any hard disk, floppy disk, tape drive, printer, scanner, etc. that supports the SCSI interface.

SCSI Upgrade

A SCSI Upgrade is any module that contains a SCSI controller and a SCSI device. An example of a SCSI Upgrade is a module containing a SCSI controller and a SCSI hard disk drive.

SCSI Expansion

A SCSI Expansion is any module that contains a SCSI device. The module expands system capabilities for memory or performance, but requires the SCSI controller in another module. Examples of SCSI Expansions include SCSI hard disk drive modules, SCSI tape drive modules, and SCSI scanner modules.

HSD Module

An HSD-nnn module is a SCSI hard disk upgrade module.

HSX Module

An HSX-nnn module is a SCSI hard disk expansion module.

RELATED DOCUMENTATION

The documents described below provide additional information related to the contents of this manual.

For a complete list of Convergent Technologies publications, see the Convergent Publications Catalog.

Status Code Manual

Operating Systems

CTOS Operating System Manual

CTOS/VM Concepts Manual

CTOS/VM Reference Manual

Release Notices

Diagnostics

Visinostics

Hardware

NGEN Installation

Power System

Series i Hardware

Series i Installation

APPLICATIONS

Intel Microprocessor and Peripheral Handbook (Volume 1, - 1987)

Specifications

Small Computer System Interface of the American National Standard for Information Systems Committee X3T9.2, ANSI Standard X3.131 approved June 23, 1986.

Common Command Set, Revision 4.B of the Common Command Set Subcommittee of X3T9.2 approved June 23, 1986.

Introductory

The Status Codes Manual contains a complete list of all the status codes that can be generated by a CTOS workstation or a Shared Resource Processor (SRP), including bootstrap ROM error codes and CTOS initialization codes. The manual also describes and interprets error status codes.

Operating Systems

The CTOS Operating System Manual describes the CTOS operating system. It specifies services for managing processes, messages, memory, exchanges, tasks, video, disks, keyboard, printer, timer, communications, and files. In particular, it specifies the standard file access methods: SAM, the sequential access method; RSAM, the record sequential access method; and DAM, the direct access method.

The CTOS/VM Concepts Manual describes system concepts for the following versions of the CTOS operating system: the CTOS/VM protected mode system as well as the CTOS real mode system for workstations, and the CTOS/SRP real mode system for Shared Resource Processors (SRPs). Topics include parameters, I/O, memory, messages, timers, system services, virtual code, interrupts, and administration.

The CTOS/VM Reference Manual describes each operation contained in the System Image and in the object module library, CTOS.lib, for the protected mode and real mode versions of the CTOS operating system (CTOS/VM, CTOS, and CTOS/SRP). The manual also contains the format of each system structure.

Release Notices

The release notice contains instructions for installing the software and provides other information pertinent to the particular software release.

Diagnostics

The Visinostics manual contains detailed instructions for using NGEN/Series i diagnostic tests. Instructions for customizing the tests are also included.

Hardware

The NGEN Installation manual gives complete installation instructions for the NGEN workstation, from unpacking up to (but not including), software installation. This manual is intended for everyone, from the novice end user to the experienced technician.

The Power System manual describes the system power supply, which consists of the +36Vdc power supply and the dc/dc converter.

The Series i Hardware manual for the 286i and 386i contains installation instructions, a functional description, software interfaces, and I/O connector pinouts.

The Series i Installation manual gives complete installation instructions for the Series 286i or 386i workstation, from unpacking up to (but not including), software installation. This manual is intended for everyone, from the novice end user to the experienced technician.

OVERVIEW

The HSD-140 is a SCSI Upgrade Module that contains a SCSI controller (host adapter) and an intelligent 140M byte hard disk. The HSD-140 Upgrade Module provides up to 140M bytes of formatted data storage for NGEN and Series i processors. The Upgrade Module connects to an NGEN workstation system to provide host adapter functions.

In a Series i configuration, the SCSI Upgrade Module transfers data from the SCSI Bus onto the X-Bus to the host processor.

Figure 1-1 shows the HSD-140 SCSI Upgrade Module.

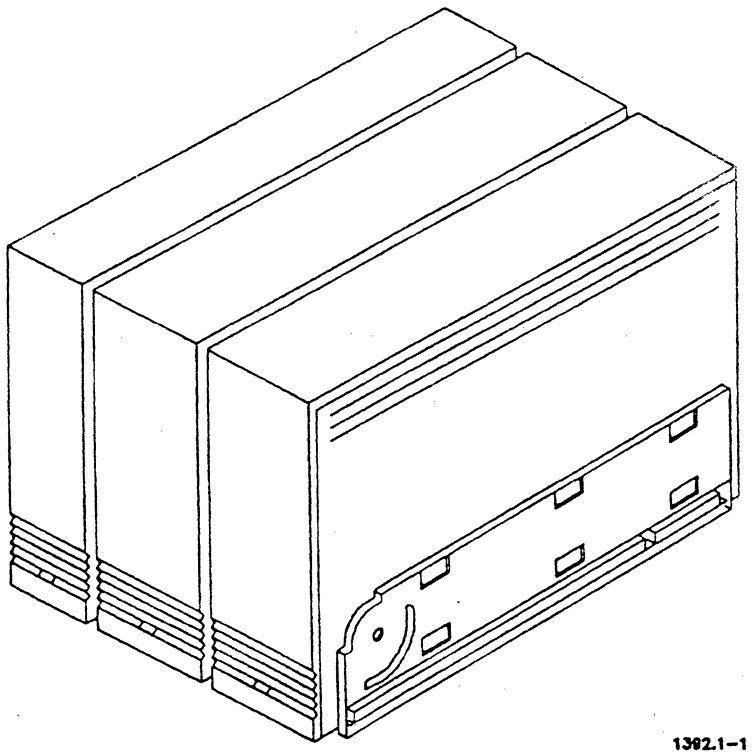


Figure 1-1. HSD-140 SCSI Upgrade Module

MAJOR COMPONENTS

The HSD-140 SCSI Upgrade Module contains the following major components:

- Enclosure
- Hard disk drive
- Controller board
- DC/DC converters
- Cooling fan

Figure 1-2 shows an internal view of some of the major components.

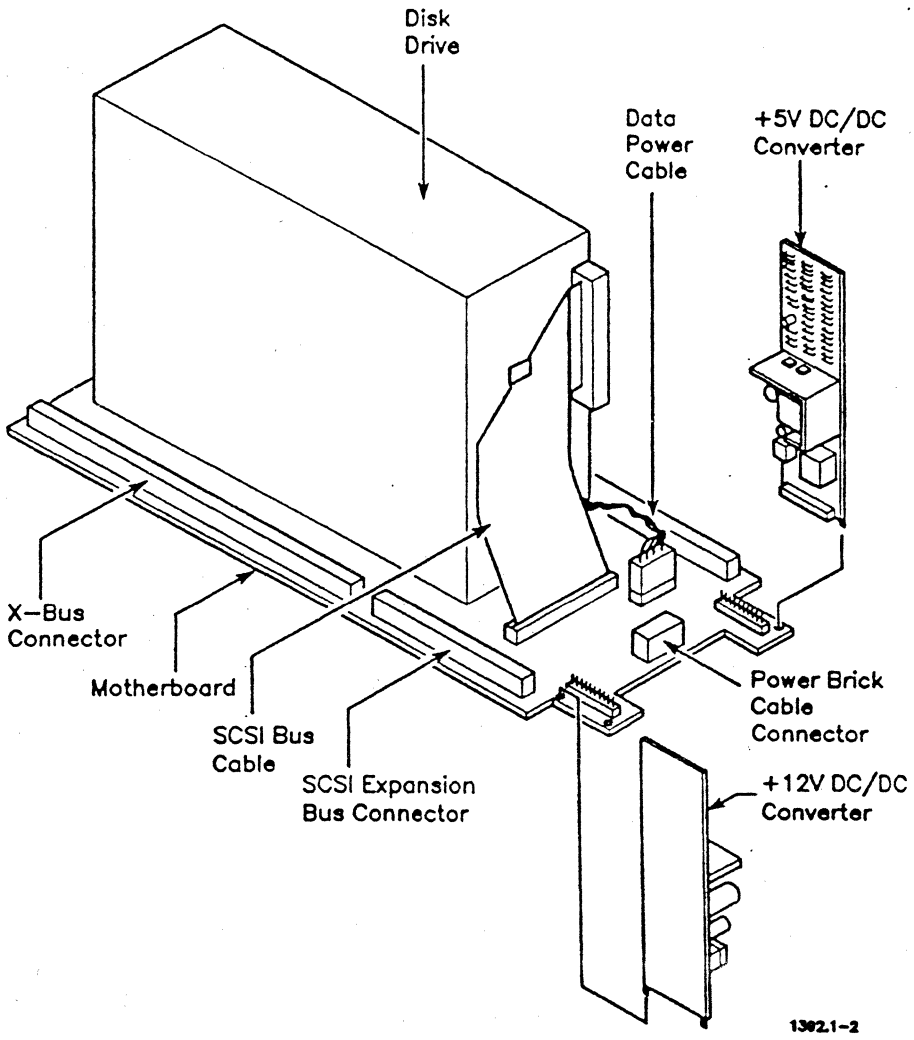


Figure 1-2. HSD-140 Major Components

ENCLOSURE

The enclosure consists of a top front cover, rear assembly, and two side panels. This enclosure contains a hard disk drive unit, the controller board, two dc/dc converters, and a cooling fan.

HARD DISK DRIVE

The disk drive unit contains a full-height Winchester drive with an average seek time of 23 ms, an average access time of 24.6 ms, and a minimum formatted capacity of 140M bytes. In addition to the drive, the unit contains support circuitry, which includes disk control logic, a data separator, the SCSI bus interface, and buffers. The buffers hold at least one track of data, so that the drive can transfer a complete track before disconnecting from the SCSI controller (host adapter).

The 140M-byte capacity is measured using 512-byte sectors and is at least 140 million bytes. Sectors used by the drive unit firmware for bad-sector sparing or other error-correction information are not counted towards the 140M-byte minimum formatted capacity.

The drive unit mounts vertically and connects to the controller board with two cables: the power cable and the SCSI bus cable.

CONTROLLER BOARD

The controller board is a multilayer PC board that contains the main logic for the Upgrade Module. The logic consists of one X-Bus Gate Array, one Interrupt/SCSI/Keyboard (I_S_K), and their supporting logic.

The X-Bus Gate Array provides the necessary signals to allow the NGEN system/Series i Processor, internal X-Bus expansion cards, and various X-Bus expansion modules to interact with each other.

The I_S_K controls the SCSI bus interface. The interface communicates through two SCSI bus connections that are wired in parallel. The first connection leads to a cable that connects the internal SCSI bus to the hard disk drive. The other connection leads outside of the Upgrade Module to external SCSI bus modules such as a SCSI hard disk-drive expansion module (HXS-nnn).

The internal cable connects to a 50-pin header specified by the SCSI specification. The external connection consists of a 44-pin connector that carries standard SCSI signals, SCSI ID information, and asynchronous signals. See Table 1 for pinout information.

DC/DC CONVERTERS

The power system for the Upgrade Module requires two internal dc/dc converters. One converter supplies +12 Vdc to the fan and the disk drive unit. The other converter supplies +5 Vdc for logic circuits on the controller board and the disk drive. For more information, see the Power System Manual.

COOLING FAN

The cooling fan mounts on brackets in the rear assembly and receives power through a power cable connected to the controller board power distribution network.

INDICATORS

Green LED: Indicates +5 Vdc to unit when lit. Located on lower-left front of module.

Green LED: Indicates SCSI activity when lit. Located on lower-center front of module.

7-Segment Display: User programmable with software register. Located on the rear assembly. See "Software Interfaces" for the register format.

SPECIFICATIONS

This section lists the following specifications:

- physical
- performance
- electrical
- safety/agency

PHYSICAL SPECIFICATIONS

Module Dimensions

Height: 8 inches

Width: 5.75 inches

Depth: 12 inches

PERFORMANCE SPECIFICATIONS

Average Access Time

24.6 ms or less. Includes average seek time, average latency, and average SCSI interface overhead.

Seek Times

Track-to-Track Seek	6 ms typical
Average Seek	23 ms typical
Full-Stroke Seek	50 ms typical
Error Recovery	2 seconds worst case

Maximum Overhead

Rotational Latency (average)	8.4 ms or less
Head Switch (sequential)	3.5 ms or less
SCSI Interface	3.3 ms or less

Media Reliability

Error rates at ambient conditions do not exceed the following:

Correctable errors	1 per 10^{12} bits read
Noncorrectable errors	1 per 10^{14} bits read
Miscorrected errors	1 per 10^{21} bits read
Misdetected errors	1 per 10^{21} bits read
Seek errors	1 per 10^{6} seeks
Media defects	1 per 10^{6} formatted bytes

Air temperature rise at the exhaust point will not exceed 14°C above ambient.

Audible noise does not exceed 51 dB at a distance of one meter.

Heat dissipation does not exceed 40 watts of heat at nominal voltages and currents when operating at 50% seek duty cycle.

During input power loss, heads are parked and locked and the spindle is stopped.

The air filter traps particles of 0.3 microns or greater.

ELECTRICAL SPECIFICATIONS

Input Power to Module

(at +36 Vdc power brick connector)

+36 Vdc nominal

+31 to +40 Vdc voltage range

2 Amps

Input Power to Drive Unit

(at dc/dc converter connector)

Voltage tolerance

+5 Vdc: +/- 5%

+12 Vdc: +/- 5%

Noise/Ripple Tolerance

+5 Vdc: 50 mVpp

+12 Vdc: 100 mVpp

Start-Up Current Load (Max)

+5 Vdc: 2.0A

+12 Vdc: 3.0A

does not exceed 15 secs

Operating Current Load (Max)

+5 Vdc: 1.5A

+12 Vdc: 1.5A

SAFETY/AGENCY SPECIFICATIONS

Underwriters Laboratories Inc.

UL 478 5th Edition, (information processing and Business Equipment).

Canadian Standards Association

C22.2 No. 154M-1983 (Data Processing Equipment)

TUV Rheinland

DIN IEC 380/VDE 0806/8.81 ZH1/618/10.81

INTERCONNECT WIRELIST

Table 1 is an interconnect wirelist for the HSD-140 Upgrade Module.

Table 1

HSD-140 INTERCONNECT WIRELIST

(Page 1 of 5)

Signal	XBUS IN (P1)	CNTRL OUT (J2)	SCSI BUS (P4)	SCSI EXP BUS (J3)	DC/DC CONV (P7,P8)
XPWREN-	5	5			15
XDACK3-	6				
XDRQ3-	7				
XDACK2-	8				
XDRQ2-	9				
XDACK1-	10				
XDRQ1-	12				

Table 1

HSD-140 INTERCONNECT WIRELIST

(Page 2 of 5)

Signal	XBUS IN (P1)	CNTRL OUT (J2)	SCSI BUS (P4)	SCSI EXP BUS (J3)	DC/DC CONV (P7,P8)
XDRQ4-	13				
XADRF-	14				
XADRE-	15				
XADRD-	16				
XADRC-	18				
XADRB-	19				
XADRA-	20				
XADR17-	21				
XADR16-	22				
XADR15-	24				
XADR14-	25				
XADR13-	26				
XADR12-	27				
XADR11-	28				
XADR10-	30				
XADR9-	31				
XADR8-	32				
XADR7-	33				
XADR6-	34				
XADR5-	36				
XADR4-	37				
XADR3-	38				

Table 1

HSD-140 INTERCONNECT WIRELIST

(Page 3 of 5)

Signal	XBUS IN (P1)	CNTRL OUT (J2)	SCSI BUS (P4)	SCSI EXP BUS (J3)	DC/DC CONV (P7,P8)
XADR2-	39				
XADR1-	40				
XADR0-	42				
XPIN	44				
XPOUT					
X33KHZSYNC	46	46			14
XINTR5-	48				
XINTR3-	49				
XINTR4-	50				
XINTR2-	51				
XINTR1-	52				
XINTRQ-	54				
XMODE3-	55				
XMEMRD-	57				
XMEMWR-	58				
XDMAEN-	60				
XMODE2-	61				
XDATF-	62				
XDATE-	63				
XDATD-	64				
XDATC-	66				
XDATB-	67				

Table 1

HSD-140 INTERCONNECT WIRELIST

(Page 4 of 5)

Signal	XBUS IN (P1)	CNTRL OUT (J2)	SCSI BUS (P4)	SCSI EXP BUS (J3)	DC/DC CONV (P7,P8)
XDATA-	68				
XDAT9-	69				
XDAT8-	70				
XDAT7-	72				
XDAT6-	73				
XDAT5-	74				
XDAT4-	75				
XDAT3-	76				
XDAT2-	78				
XDAT1-	79				
XDAT0-	80				
XSPKR-	81				
XACK-	82				
XLOCK-	84				
XBHE-	85				
XRESET-	86				
XIOWR-	91				
XIORD-	92				
XPCLK	93				
XDCLK-	95				
BSDO			2	3	
BSD1			4	5	

Table 1

HSD-140 INTERCONNECT WIRELIST

(Page 5 of 5)

Signal	XBUS IN (P1)	CNTRL OUT (J2)	SCSI BUS (P4)	SCSI EXP BUS (J3)	DC/DC CONV (P7,P8)
BSD2			6	7	
BSD3			8	9	
BSD4			10	11	
BSD5			12	13	
BSD6			14	15	
BSD7			16	17	
SCSIATTN-			32	23	
SCSIBSY-			36	25	
SCSIACK-			38	27	
SCSIRST-			50	29	
SCSI_DEVICE-			41	22	
MSG-			42	31	
SCSISEL-			44	33	
C_D			46	35	
REQ-			48	37	
I_O			50	39	
IDSCSI0-				2	
IDSCSI2-				10	
IDSCSI3-				14	
IDSCSI1-				6	
IDSCSI4-				20	

CONTROLLER BOARD

The Controller board is the main logic board in the HSD-140 SCSI Upgrade Module. The Controller contains one X-Bus gate array, one Interrupt/SCSI/Keyboard (I_S_K), and supporting logic. A functional block diagram is shown in Figure 2-1.

X-BUS GATE ARRAY

The X-Bus gate array provides the necessary signals to allow a module to interact with the NGEN system/Series i Processor, internal X-Bus expansion cards, and various X-Bus expansion modules. Local signals are received from the X-Bus.

With associated logic, the X-Bus Gate Array provides module ID code, I/O base address, I/O Read (IORD), I/O Write (IOWR), ROM Read (ROM-), X-Bus Priority Output (XPOUT) generation, X-Bus Acknowledge (XACK) generation, and supports slower modules.

Initialization/Identification

The Upgrade Module is a bootable device with its own 8K byte boot ROM. When a boot bit is set, which is unique to this module, the boot ROM is read during system booting. This ROM is mapped from the Upgrade Module, into the processor, by way of the X-Bus Gate Array.

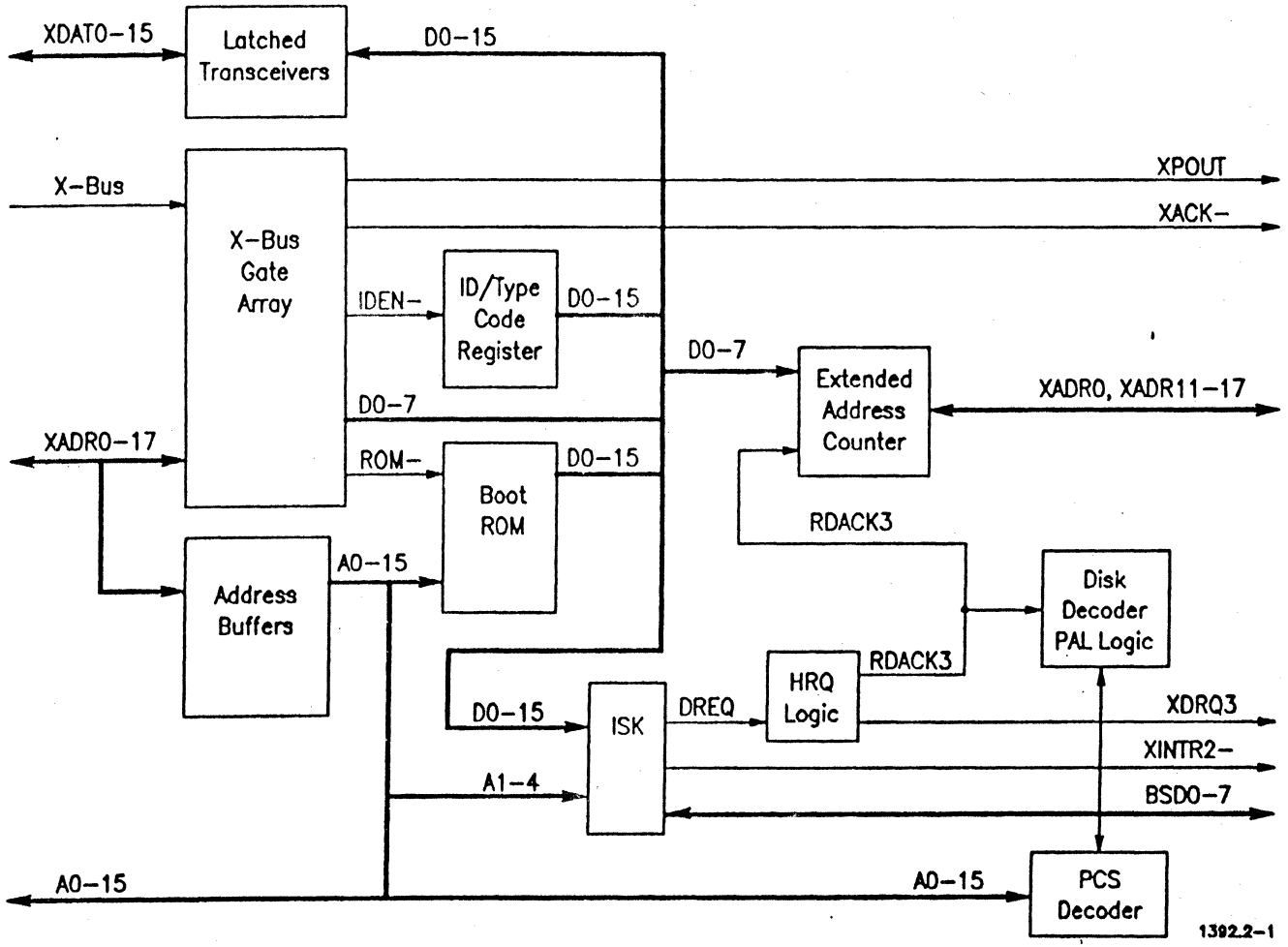


Figure 2-1. HSD-140 Functional Block Diagram

The Upgrade Module is initialized through the X-Bus interface. All modules on the X-Bus are assigned an X-Bus Priority Input (XPIN) signal line. The modules then generate an X-Bus Priority Output (XPOUT) signal line. The input signal enters a module on the left side, and the output signal exits the module on the right side (daisy-chained).

During power-up, reset, or any I/O operation, a low XPIN signal is generated to the X-Bus Gate Array. This causes the X-Bus Gate Array to reset an internal flip-flop to drive XPOUT low. The XPOUT then becomes the low XPIN for the next module down on the X-Bus. This suspends all X-Bus activity for modules farther down on the X-Bus, that is, to the right of the Upgrade Module. When XPIN is low, an I/O base address register clears.

When XPIN is high and XPOUT is low, there is no I/O base address.

An X-Bus I/O read command (XIORD-), at address 0000h, enables the Upgrade Module to generate an ID type code by way of the X-Bus. When ID is issued, a write (XIOWR-) to the module I/O base address occurs.

As shown in Figure 2-1, the X-Bus Gate Array issues IDEN- to the ID/Type Code Register when this first read occurs. The ID/Type Code Register generates the ID/Type Code onto the Data Bus (D0-15). The bidirectional latched transceivers directs D0-15 to XDAT0-15, which goes to the X-Bus.

Once the host processor receives the ID/Type Code, it writes the I/O base address for the Upgrade Module into the X-Bus Gate Array. This I/O address defines the range of addresses reserved for the HSD-140 Upgrade Module. The host processor issues an I/O address by way of the low-order data lines (XDAT0-7). The bits of this data byte become the high-order eight bits of the 64K I/O base address range for this module.

After initialization, the first Module is assigned the I/O address space between 0X00h and 0XFFh, and therefore responds to I/O operations only within this address range. Where "X" is the module position. X would be "1" for the first X-Bus to the right of a processor module.

Memory Read Operations

Memory reads on the X-Bus are performed by setting up the 4-bit Memory Base register, inside the X-Bus Gate Array, to map in one of 16M bytes of address space available on the X-Bus. Thereafter, the system controller can address the Upgrade Module by placing a 24-bit memory address on the X-Bus, with the four most significant bits pointing at the appropriate megabyte of address range.

The host processor then generates a memory read command, which activates the appropriate bus interchange logic. After accepting the data (a read operation), the Upgrade Module sends X-Bus Acknowledge (XACK-) to the host processor.

Memory reads are used to access the Boot ROM on the Upgrade Module. Memory writes are not supported.

INTERRUPT/SCSI/KEYBOARD (I_S_K)

The I_S_K is an application-specific integrated circuit (ASIC) implemented with gate array technology. The I_S_K performs interrupt control and provides an interface to the hard disk SCSI logic, the SCSI Expansion Bus, and the host processor.

The I_S_K handles the complete interface to the SCSI drive and has complete control of the amount of the host processor bus bandwidth it uses. The internal 140M-byte hard disk drive and expansion disks are controlled through the SCSI Bus. The keyboard interface is not used.

SCSI architecture uses the concept of memory blocks in the host processor for command, data, and status interchange between the host system and the SCSI device.

Interrupt Control

The host processor receives both internal and external interrupts. Internal interrupts are synchronous and respond to events detected during the execution of an instruction. External interrupts are asynchronous and are generated by devices external to the host processor.

The interrupt control section of the I_S_K consists of two cascaded 8259A Programmable Interrupt Controllers. The primary use of the 8259's is to pass the SCSI interrupt through to the host processor. When a SCSI interrupt occurs, the host processor must go through an End of Interrupt (EOI) operation. SCSI device interrupts are ORed within the I_S_K and are generated, through the 8259's, to the host processor as XINTR2-.

See Chapter 3, "Software Interfaces," for more details.

SCSI Controller

The SCSI controller within the I_S_K controls all internal and external SCSI devices. The SCSI controller section also uses one channel of the host processor DMA controller that is shared with X-Bus hard disk modules (HD-nnn). Therefore, overlapped data transfers are not supported.

The SCSI controller has three major logic blocks: SCSI bus interface logic, an arbitration/selection state machine, and a four-word data buffer.

SCSI Bus interface logic uses the host processor command and status bits to initiate data transfers to and from devices on the SCSI bus.

With systems that contain more than one I/O device on the SCSI bus, the I_S_K must arbitrate between the I/O devices and select the applicable device to transfer data. An I_S_K internal state machine performs the arbitration/selection process.

When the host processor wants to access the SCSI bus, it initializes the internal state machine. The internal state machine then polls all of the SCSI command signals and generates an Interrupt back to the host processor. This allows the host processor to access the SCSI bus.

The SCSI bus can support up to eight I/O devices. Each I/O device must have a SCSI identification (ID) number associated with it (that is, 0 through 7). The I_S_K (SCSI bus controller) has an ID of 7 (since it must access the SCSI bus). The internal hard disk drive has an ID of 0. The remaining SCSI IDs (6 through 1) are for external SCSI devices.

See the SCSI Upgrades and Expansions Manual for more information on system-wide SCSI ID numbering.

A four-word data buffer facilitates data transfers between the 16-bit data bus (D0-15) and the 8 bits of data (BSD0-7) on the SCSI bus.

The I_S_K issues a DMA Request (DREQ) to obtain DMA service. DREQ goes through the Hold Request Logic (HRQ Logic) to request control of the system bus. HRQ Logic creates X-Bus DMA Request (XDRQ3). The system responds back with DMA Acknowledge (DACK3) and goes through the synchronizer PAL logic to determine if it is RDACK3. RDACK3 indicates, to the I_S_K, that a DMA cycle has been granted.

The Peripheral Chip Select (PCS) Decoder is used with the Disk Decoder PAL logic to select the host processor DMA controller.

Since the I_S_K has only 16 bits of word address, an extended address range is required to handshake with the upper address bits of the X-Bus. The Extended Address Counter expands that boundary between word address bits 17-24.

Typical I_S_K Cycle

The I_S_K performs four distinct I/O read and write cycles for every request. A typical I_S_K cycle consists of an arbitration/selection phase that is handled by the I_S_K state machine. This is followed by a command phase.

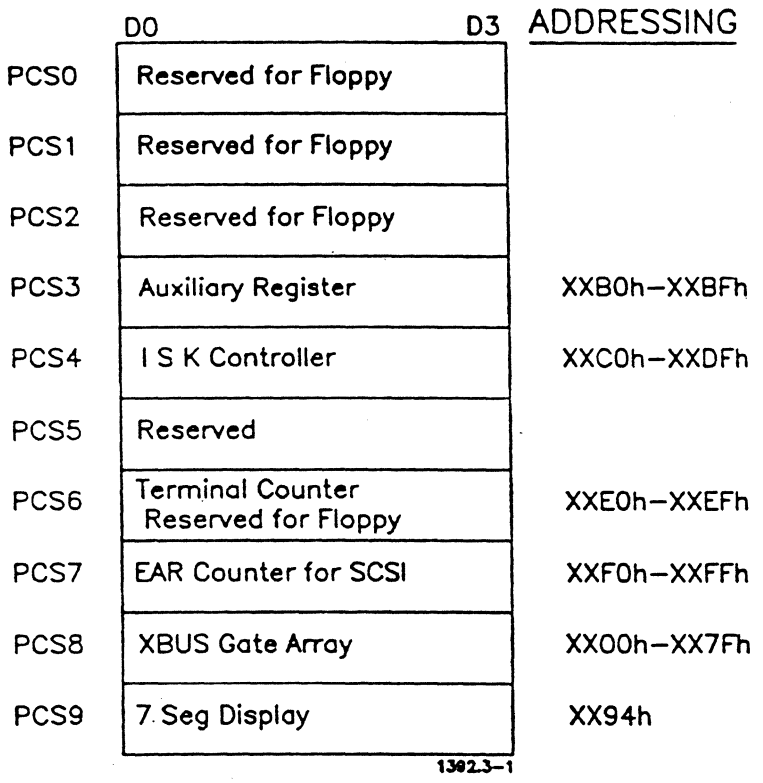
The command phase is handled by the host processor. The host processor goes through the I/O, through the I_S_K, directly to the SCSI Bus to determine what the command phase is and what the disk drive wants upon going into the data phase.

The data phase consists of data transfer, and is handled by DMA. Upon leaving data phase, an Out of Data Phase (ODP) interrupt occurs.

The ODP interrupt tells the host processor to interrogate the I_S_K again to determine what the status is. This is usually followed by a SCSI status phase or a SCSI message phase.

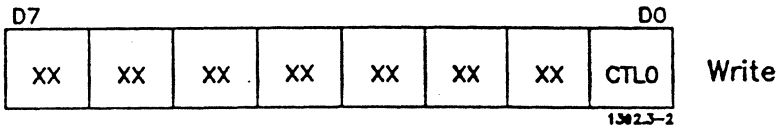
GENERAL I/O

I/O decoding is based on Peripheral Chip Select (PCS) type of decoding. All sub-address decoding is either done directly by the LSI components or custom logic locally (for specific details see the appropriate section in this chapter).



PCS3 - AUXILIARY REGISTER

The Auxiliary Register is organized as a group of single (1) bit registers. This allows the software to set individual bits without affecting the bits in the register. When reading this register, the software can determine what configuration and mode the HSD-140 Upgrade Module is being run in. The bit definitions are as follows:

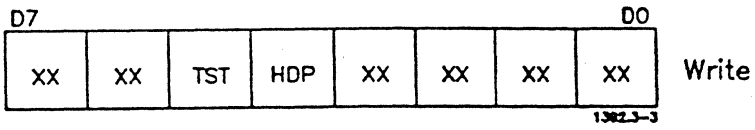


Where:

CTL0 @Adr. XXBAh; Hard Disk LED Enable (Controls LED located on lower-center front of module).
1 = LED On, 0 = LED Off

@Adr. XXBCh; I_S_K Chip Reset (must be toggled)
0 = Not Reset, 1 = Reset

[Address: XXBXh]



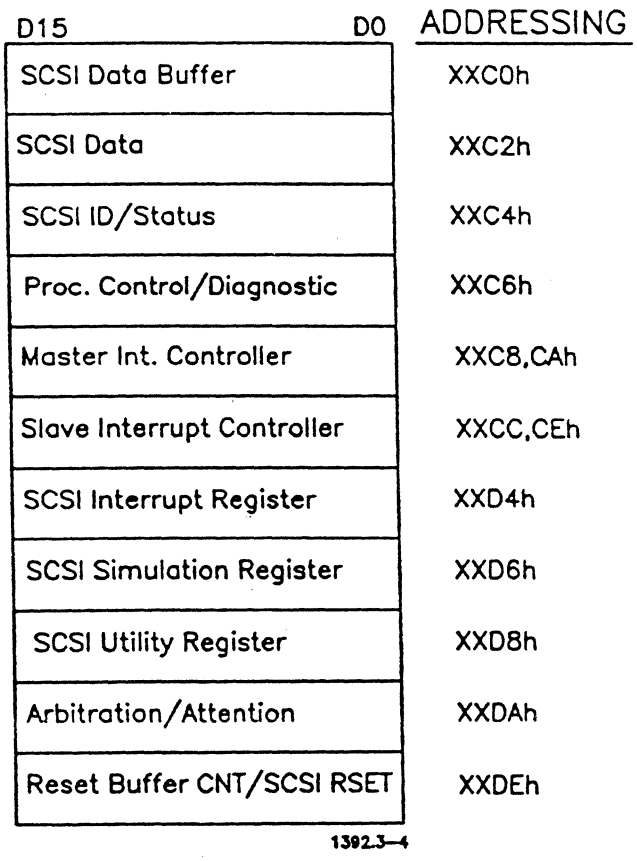
Where:

TST Test Mode Enable (NOT USED)
0 = test mode enabled, 1 = normal mode

HDP SCSI Device Present (NOT USED)
0 = present, 1 = not present

PCS4 - SCSI (I_S_K) CONTROLLER

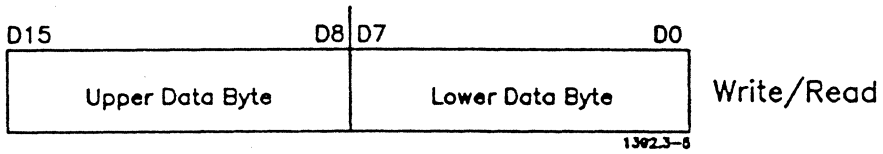
The Interrupt/SCSI interface for the HSD-140 primarily consists of a CMOS standard cell called the I_S_K (Interrupt/SCSI/Keyboard). The I_S_K is located on the HSD-140 controller board assembly. The interrupt control section of the I_S_K consists of two cascaded 8259As. The SCSI controller section utilizes one channel of an external DMA controller. This is a shared channel with the X-Bus HD-nnn modules. Thus, overlapped data transfers are not supported. There is no hardware reason to exclude overlapped seeks. The I_S_K handles the complete interface to the SCSI drive and has control of the amount of CPU bus bandwidth it uses. It has a four-word (8-byte) buffer that accumulates the bytes as they come off the disk drive and transfers them to memory as a burst of four words. The Keyboard UART section of the chip is not used.



SCSI Data Buffer

Data can be input to the SCSI bus either through a direct access or through the four-word (eight-byte) SCSI data buffer. The SCSI data buffer uses the DMA transfer mode. During a DMA transfer, the buffer is loaded/unloaded on the system side through the DMA channel, while the SCSI state machine interfaces directly to the SCSI data bus. The format for loading or unloading the buffer is as follows:

[Address: XXC0h]

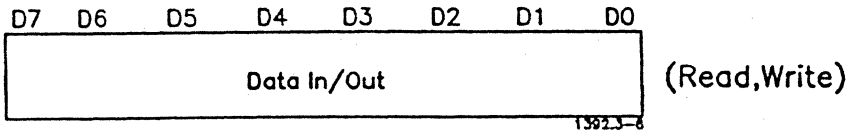


Non DMA accesses are made sequentially, and the address automatically increments within the IC. This port is used to access the eight bytes in the four-word DMA buffer.

SCSI Data

Any access to the SCSI data port allows the software to directly access the SCSI data bus through programmed I/O. Both direct reads and writes are supported. The bit allocation is as follows:

[Address: XXC2h]

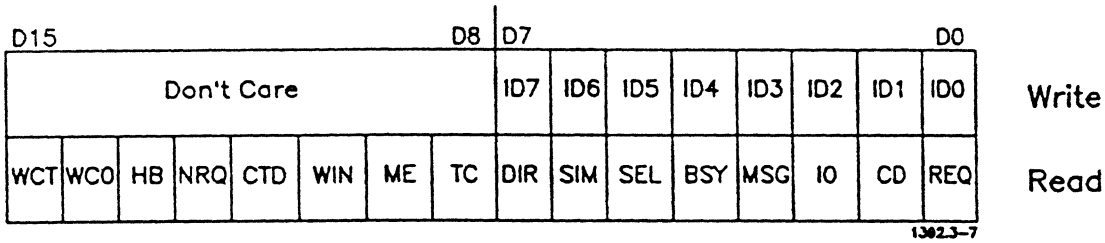


When a SCSI device is selected (CTD in port XXC4h is set), a read or write of this port generates a SCSIACK- on the SCSI bus. This is how command bytes, message bytes, and status bytes are transferred between the host controller and the SCSI device that is selected.

SCSI Identification/Status

A write to the SCSI identification register must occur before any operation can be performed on the SCSI bus. On a write operation, the SCSI initiator ID number is written into this register. The default number is 7 and is programmable on the I_S_K chip. This number is used by the I_S_K arbitration/selection state machine, during the arbitration phase. The read register for this I/O address can read all the SCSI bus status bits. The format for both the write and the read are depicted below.

[Address: XXC4h]



Where the write bits have the following meanings:

ID0-7 SCSI Device Identification Address
A single bit is set to determine the initiator ID on the bus.

Where the read bits have the following meanings:

WC1,WC0 Transfer Word Count
(index into four-word DMA buffer)
0 0 = Word 0
0 1 = Word 1
1 0 = Word 2
1 1 = Word 3

HB High Byte
0 = low byte, 1 = High byte

The bits described above are defined when the data phase is exited. The number depicts the number of bytes in the last four that were transferred (that is, bytes remaining = 4 minus the above). HB is set if an odd number of bytes are transferred in the last DMA burst. Note that, "WC1, WC0, and HB" taken as a 3-bit value, indicates the number of bytes that were transfered in the last burst.

NRQ New Request (Software must test NRQ for a true state before checking the SCSI bus phase.)
0 = Request previously issued
1 = new request

CTD SCSI Device Connected (Indicates that either selection or reselection has completed, and a SCSI device is connected to the bus and the initiator.)
0 = not connected
1 = devices connected

WIN Arbitration Win
0 = lose arbitration
1 = won arbitration

ME Local Device Operation
0 = operation select local device
1 = select external device

NOTE: ME is for diagnostic use only.

TC Transfer Complete (Indicates state of the DMA Request flip-flop.)
0 = buffer not transferred
1 = buffer transferred

DIR — SCSI Direction (Used for I_S_K testing. Indicates how the I_S_K is driving the bus.)
0 = SCSI Bus In
1 = SCSI Bus Out

SIM — Simulated Data Enable (NOTE: used for I_S_K chip diagnostics only.)
0 = Simulation Off
1 = Simulation On

The following bits are read from the SCSI Bus:

SEL — SCSI Select
0 = not asserted
1 = asserted

BSY — SCSI Bus Busy
0 = not asserted
1 = asserted

MSG — SCSI Message Bit
0 = not asserted
1 = asserted

I_O — Input/Output
0 = not asserted
1 = asserted

C_D — Command/Data
0 = not asserted
1 = asserted

REQ — SCSI Request
0 = not asserted
1 = asserted

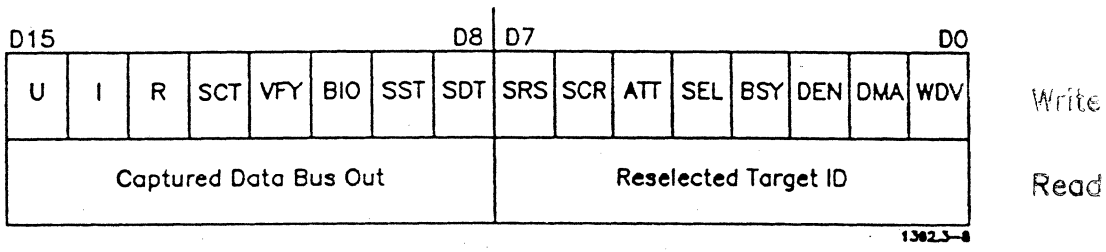
NOTE: Software should check NRQ instead of REQ to determine if the SCSI device is requesting a bus cycle.

SCSI Bus Phases are listed below (refer to address register XXC4h on Page 3-5).

MSG	I_O	C_D	REQ	HEX	PHASE
0	0	0	1	1h	DATA OUT PHASE
0	0	1	1	3h	CMD
0	1	0	1	5h	DATA IN
0	1	1	1	7h	STATUS
1	0	0	1	9h	*
1	0	1	1	Bh	MESSAGE OUT
1	1	0	1	Dh	*
1	1	1	1	Fh	MESSAGE IN

SCSI Processor Control/Diagnostic Register

[Address: XXC6h]



Where the write bits have the following meanings:

U UART Test Enable (NOT USED-set to zero)
0 = Test Mode Off, 1= Test Mode On

I Interrupt Test Enable (Used for chip testing only.)
0 = Test Mode Off, 1= Test Mode On

R UART Reset (NOT USED-set to zero)
0 = Test Mode Off, 1= Test Mode On

SCT Not Used (Must be set to zero)

VFY Not Used (Must be set to zero)

BIO Batched SCSI Input/Output
0 = direct SCSI I/O
1 = Batched SCSI I/O

SST Simulated SCSI Status (Used for chip testing only)
0 = actual SCSI status
1= diagnostic status latch

SDT Simulated SCSI Data (This is the same bit as in address XXC4h, and is used for chip testing only)
0 = actual SCSI data bus
1= diagnostic data latch

SRS Software I_S_K Reset (Must be set to enable the entire I_S_K chip)
1 = not reset, 0 = reset I_S_K

SCR SCSI Bus Reset (Must be toggled to assert SCSIRST-)
0 = not reset, 1 = reset SCSI Bus

ATT Direct I/O SCSI Attention (Asserts attention during the selection phase)
0 = attention de-asserted
1 = attention asserted

SEL Direct I/O SCSI Select (For diagnostic use only)
0 = Select de-asserted
1 = Select asserted

BSY Direct I/O SCSI Busy (For diagnostic use only)
0 = busy de-asserted
1 = busy asserted

DEN Control Clear (Must be used after selection to clear ATT on the SCSI bus)
0 = Normal operation
1 = Clears - BSY, SEL, ATT, ARB_IO (on SCSI Bus)

DMA DMA Enable (Enables the four-word (8-byte) DMA buffer control logic. Set this only during SCSI data phases.)
0 = DMA disabled, 1 = DMA enabled

WDV Write to SCSI Device (Set this during a SCSI data out phase when doing DMA)
0 = read DMA from SCSI device
1 =DMA write to SCSI device

NOTE: During normal operation, all bits except WDV, DMA, DEN, ATT, SCR, and SRS will be set to zero. SRS must always be set to zero for the I_S_K SCSI section to function.

Where the read bits have the following meaning:

The reselected ID is the ID of the target that reselected the local initiator. After reselection the software must read this port to determine the nature of the device that has re-connected itself to the system. The captured data is a diagnostic tool that captures what actually goes to the SCSI data bus. Monitoring this port gives an accurate history of what the SCSI bus received.

Master Interrupt Controller

Internal to the I_S_K there are two complete 8259A Peripheral Interrupt Controllers (PICs). The two controllers are connected in cascade mode with one being a master and one a slave. For the HSD-nnn, the master and slave PICs are programmed to generate the interrupt from the SCSI section of the I_S_K out to the single pin of the chip, and on to XINTR2- (the SCSI interrupt enters the slave PIC as interrupt number 4). The software must issue an End of Interrupt (EOI) command to the I_S_K PICs to clear the interrupt condition within the PICs.

The master PIC handles interrupt request levels 0 through 6. The I/O for the PIC is described in the Intel Microprocessor and Peripheral Handbook. A brief summary is outlined here for reference.

Address	Register Definition	Operation
XXC8h	Init Command Words	Write/Read
XXCAh	Operation Command Words	Write/read

Slave Interrupt Controller

The slave PIC handles interrupt request level 7. The I/O for the PIC is described in the Intel Microprocessor and Peripheral Handbook. A brief summary is outlined here for reference.

Address	Register Definition	Operation
XXCCh	Init. Command Words	Write/Read
XXCEh	Operation Command Words	Write/read

To program the PICs to generate the interrupt, perform the following:

SET UP MASTER PIC

Output to port:	XXC8h	this value:	19h
	XXCAh	this value:	40h
	XXCAh	this value:	80h
	XXCAh	this value:	1Dh
	XXCAh	this value:	FFh
	XXC8h	this value:	0Bh

SET UP SLAVE PIC

Output to port:	XXCCh	this value:	19h
	XXCEh	this value:	50h
	XXCEh	this value:	07h
	XXCEh	this value:	09h
	XXCEh	this value:	FFh
	XXCEh	this value:	0Bh

CLEAR SLAVE MASK

Output to port: XXCEh this value: EFh

CLEAR MASTER CASCADE MASK

Output to port: XXCAh this value: 7Fh

SCSI Interrupt Register

A SCSI interrupt can have multiple sources. The exact nature of the interrupt is stored in the SCSI interrupt register. Upon receipt of a SCSI interrupt this register should be read. The interrupt register contains all the conditions that can cause a SCSI interrupt, not just the condition that initiated the vector. Thus, more than one condition can be set in the register.

When the interrupt register is written to, the interrupt mask is set. This allows different interrupts to be masked off. Any masked-off interrupt will still show its condition when the interrupt register is read. The bit definitions are as follows.

[Address: XXD4h]

D15							D8	D7							D0	
Don't Care								X	X	SRM	RSM	MSM	ODPM	SLM	ARM	Write
X	X	RS1	RS0	AS3	AS2	AS1	AS0	X	X	SRES	RSEL	MSG	ODP	ARB	SEL	Read

1392.3-8

Where the write bits have the following meaning:

SRM — SCSI Bus Reset Interrupt Mask
0 = unmasked, 1 = masked

RSM — Reselection Interrupt Mask
0 = unmasked, 1 = masked

MSM	Message Phase Interrupt Mask 0 = unmasked, 1 = masked
OPDM	Out of Data Phase Interrupt Mask 0 = unmasked, 1 = masked
SLM	Selection Complete Interrupt Mask 0 = unmasked, 1 = masked
ARM	Arbitration Complete Interrupt Mask 0 = unmasked, 1 = masked

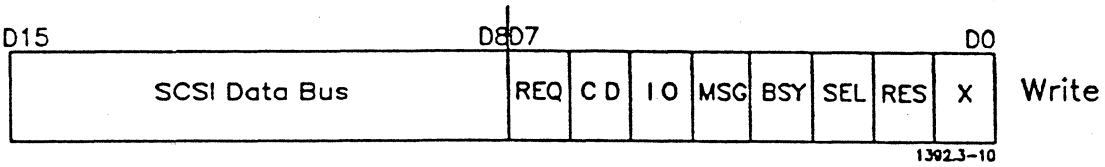
Where the read bits have the following meaning:

RS0-1	Reselection State Machine State Count (for diagnostic purposes)
AS0-3	Arbitration/Selection State Count (for diagnostic purposes)
SRES	SCSI Reset Interrupt 0 = inactive, 1 = active
RSEL	Reselection Interrupt 0 = inactive, 1 = active
MSG	Message Phase Interrupt 0 = inactive, 1 = active
ODP	Out of Data Phase Interrupt 0 = inactive, 1 = active
ARB	Arbitration Complete Interrupt 0 = inactive, 1 = active
SEL	Selection Complete Interrupt 0 = inactive, 1 = active

SCSI Simulation Register

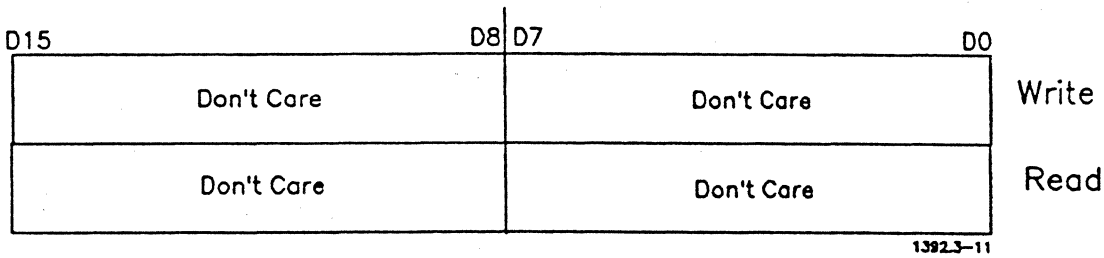
The I_S_K allows the processor to simulate (during diagnostics only) an external SCSI device in a type of intelligent loopback. The lower bits, D0-D7, have the same meanings as described in the previous section, SCSI Identification/Status.

[Address: XXD6h]



SCSI Utility Register

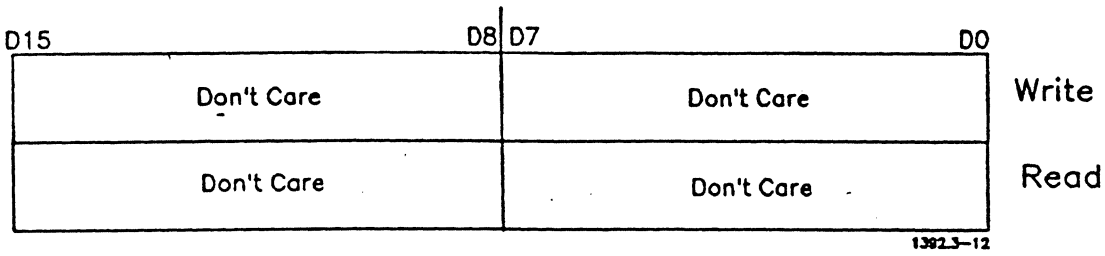
[Address: XXD8h]



Any write to the SCSI utility register sets the initial DMA request for a SCSI data out transfer. This write must be done to initiate each new block. This write is done only after WDV is set in the control register, and just before DMA is set in the control register. Any read from the utility register will clear selected SCSI interrupts.

Arbitration/Clr DREQFF Control

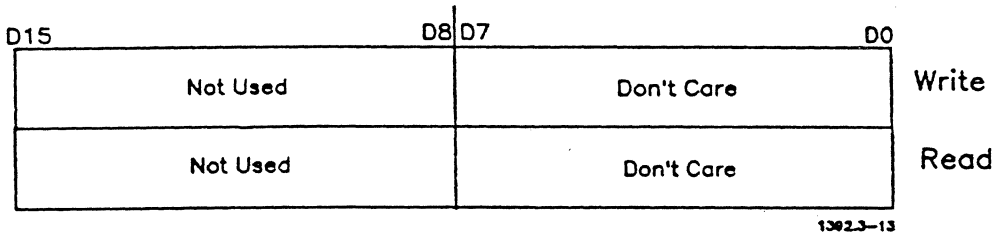
[Address: XXDAh]



A write to this register allows the I_S_K to begin to automatically arbitrate for the SCSI bus. A read from this port clears all DMA request flip-flops. The DMA flip-flops must be cleared before setting up System DMA for data phase transfers.

Reset Buffer Count/SCSI Reset

[Address: XXDEh]



A write to this register resets only the SCSI section of the device. A read from this register sets the internal SCSI buffer counter to zero. The buffer counter should be set to zero when the DMA flip-flops are cleared before DMA is started.

How to Program the I_S_K

Perform the following steps to program the I_S_K to Arbitrate and select a SCSI device:

1. Output the Host ID to port XXC4h.
2. Output the Host ID OR'd with the Target ID to port XXC2h.

3. Clear the ATT flip-flop, by toggling DEN:
   Output to port XXC6h DEN or SRS.
   Output to port XXC6h SRS.

NOTE: Leave SRS set to keep the chip enabled.

4. Output 1 to port XXDAh to start the Arbitration state machine.

5. Poll port XXD4h for SEL interrupt, or program the interrupt controller to handle the interrupt.

6. After selection, clear attention again as in Step 3.

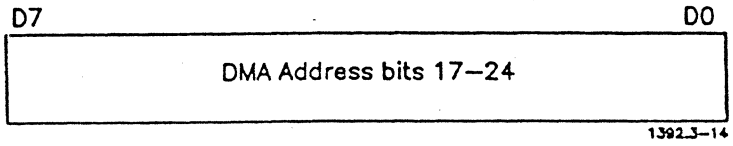
7. Output to port XXC2h the SCSI Identify message (80h), OR with the SCSI connect mode (see ANSI SCSI specifications).

8. Input from port XXD8h to clear the Arbitration/Selection interrupts.

9. The SCSI device is now connected. The software can sample NRQ and the SCSI bus phase lines to determine which phase to progress to (usually the Command phase).

PCS7 - EAR COUNTER

[Address: XXF0h]



This register is loaded with the upper 8 bits of a 24-bit DMA word address. The lower 16 bits are loaded into the host processor DMA Controller. The register is auto-incremented to allow DMA across memory boundaries.

PCS8 - X-BUS GATE ARRAY

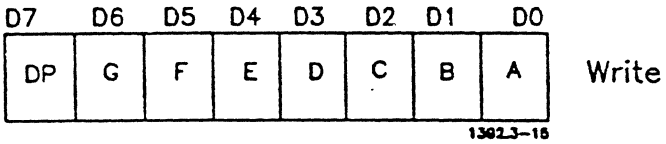
The X-Bus Gate Array provides the required interface between the X-Bus and the HSD-140. It supports ID code enabling, I/O base address processing, and memory base addressing.

Address	Register Definition	Operation
0000h	Type Code Register	Read
0000h	Module I/O Base Address	Write
XX20h	Module Mem Base Addr(ROM)	WR/RD
XX0Ah	ROM Shadow Register	Write

PCS9 - SEVEN SEGMENT DISPLAY

The Seven Segment Display is located in the back of the module. The display is available for operating system use.

[Address: XX94h]



D0-D7

0= SEGMENT ON 1= SEGMENT OFF

The Seven Segment Display is shown below.

```
 aaaaa
f    b
f    b
f    b
 ggggg
e    c
e    c
e    c
 ddddd
           dp
```