TR79-FA
DECmagtape (1600 cpi) maintenance manual

EK-TR79F-MM-001

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CONTENTS

CONTENTS (Cont)

ILLUSTRATIONS

TABLES

CHAPTER 1
INTRODUCTION

1.1 INTRODUCTION

The TR79-FA Tape Control Unit, designed and manufactured by DIGITAL, interfaces the PDP-11 family of central processors to the Hewlett Packard 7970-E, 9-track, 1600-character-per-inch (cpi), phase-encoded Magnetic Tape Transport. The protocol between the Tape Control Unit (TCU) and the Magnetic Tape Transport (MTT) conforms to ANSI standard x 3.2.1/400, REV x 3.2.1/375. The TR79-FA writes and reads industry-compatible formats. This document provides the user with the information necessary for operating and maintaining the TR79-FA. Theory of operation discussions and logic diagrams to provide an understanding of TR79-FA operation are included.

1.2 GENERAL DESCRIPTION

The TR79-FA provides the interface logic for communication between the PDP-11 Central Processor Unit (CPU) and the Magnetic Tape Transport (MTT) and operates on a Direct Memory Access, Non-Processor Request (DMA-NPR) channel. The Tape Control Unit (TCU) consists of the following functional sections (Figure 1-1):

1. Address Selection
2. 16-Bit Status Register
3. 16-Bit Control Register
4. Bus Address and Word Count Registers
5. Function Decoder
6. GAP Timing and Motion Control
7. MTT Commands Register
8. 2-Stage Read/Write Buffer
9. Buffer and NPR Control Logic
10. Bus Master and Interrupt Control
11. Read/Write Parity Check
12. Drivers and Receivers

The TR79-FA is a magnetic tape storage system capable of driving from one to four HP 7970-E transports (one master and three slaves). The TCU writes or reads digital data, in parallel, on or from magnetic tape in 9-channel, industry-compatible format. This TCU is designed to operate at transfer rates of 40,000 characters per second, but can be modified to operate at higher speeds. The TCU contains all motion and gap timing logic and generates all required MTT commands. One double-stage buffer is used for both write and read functions. Status and control registers are provided to permit communication between operator and machine.

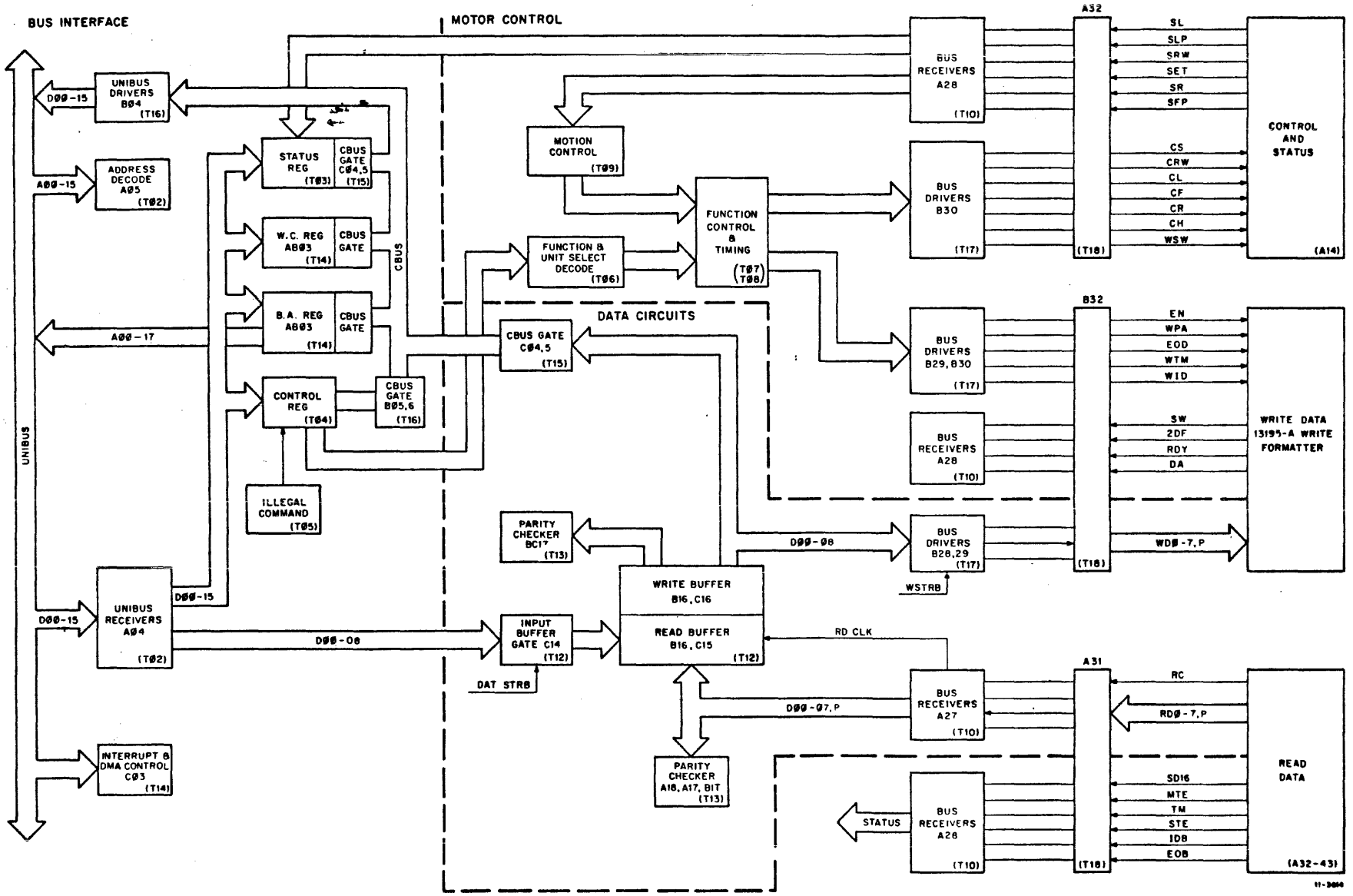


Figure 1-1 System Block Diagram

The MTT (HP 7970-E) features a 1600-cpi read-after-write, phase-encoded data capability at speed ranges of 10 to 45 ips. The MTT is available in master/slave unit combinations that are connected in a "daisy-chain" configuration when more than one transport is used. The master unit contains the following phase-encoded read functions:

1. Identification Burst (IDB) Detection
2. Detect and Strip Preamble and Postamble
3. Tape Mark Detection
4. Read Deskewing
5. Multiple Track Error (MTE) Detection
6. Single Track Error (STE) Detection
7. End of Block Detection.

Both master and slave units contain the same write and command-and-status electronics. Phase-encoded data electronics is contained only in the master unit. Slave unit read capability is accomplished through the master for multi-unit operation.

Formatting of the write data is accomplished within the Write-Formatter P.C. card (HP 13195A). This card generates the identification burst (IDB), Preamble and Postamble, and Tape Mark. The Formatter also generates the clock synchronization signal with which data is written. One Write-Formatter card is sufficient for one master and three slave tape units.

1.3 SPECIFICATIONS

The following are presented here for reference purposes only and are subject to change without notice.

1.3.1 Transport Control Unit

Mechanical	
Logic Panels	
Type	H911
Quantity	Two
Dimensions	10-3/8 in. h, 19 in. w, 6-3/4 in. d
Weight	20 lb approx
Cabinet	
Type	H961-A
Dimensions	72 in. h, 22 in. w, 30 in. d
Weight	300 lb
Electrical	
Power Control Type	H861-C
Power Supply	H720-E
Input Power	115 Vac 10%, 60 Hz ± 3 Hz
Line Current	
TCU	8 A
Fans	2 A
Power Dissipation	600 W approx
Logic Potentials	+5 V, −15 V, 0 V
Module Series	M and G series

Operational

Data	
Speed	25 ips
Transfer Rate	40,000 nine-bit char/sec
Character Rate	25 μs
Transfer Mode	DMA (NPR)
Inter-Record Gap	
Write-Write	0.662 in. approx
Write-Rev-Read-Write	0.612 in. approx
IDB Gap	2.6 in
TM Gap	0.662 in.
Data Checking	
Write	Write parity, read after write parity, Single Track Error (STE), Multiple Track Error (MTE)
Read	Read Parity, Single Track Error, Multiple Track Error
Programmable Commands	Write, Read Forward, Read Reverse, Erase, Rewind, Fast Forward, Write ID Burst Write Tape Mark
Register Addresses	
Control (CR)	764000
Status (SR)	764002
Word Count (WC)	764004
Bus Address (BA)	764006
Interrupt	
Priority Level	BR4
Vector Address	170

Environmental

Temperature	40° to 95° F
Humidity (relative)	20% to 95% (no condensation)

1.3.2 Magnetic Tape Transport

The following are presented for reference only. For current specifications, consult a Hewlett Packard representative.

Operational

Model	Hewlett Packard 7970-E
Recording Mode	Phase Encoded (ANSI/IBM compatible)
Tape	Computer Grade
Width	0.5 in.
Thickness	1.5 mils
Tape Tension	8.5 oz, nominal
Reel Diameter	Up to 10.5 in.
Tape Speed	25 ips (10 to 45 ips available)
Inst. Speed Variation	3%
Rewind Speed	160 ips
Fast Forward (or Fast Reverse)	160 ips
Fast Forward Start/Stop	
Characteristics (at 160 ips)	
Distance	Start 40 in., nominal Stop 40 in., nominal

Operational (Cont)	
Time	0.700 sec (max)
Start/Stop Times (25 ips)	15 ms
Start/Stop Tape Travel	0.187 in. ± 0.020 in.
R/W Head Separation	
Distance	150 mils ± 5%
Time (25 ips)	6 ms
Character Spacing	0.625×10^{-3}
No. of Characters Between Heads	240 ± 5%
Reel Motor Breaking	Dynamic
BOT and EOT Reflective Strip Detection	Photo-electric (IBM compatible)
Local Transport Control	Power On/Off, Reset, Rewind, On-Line, Load
Electrical	
Input Power	115 or 230 V (±10%), 48 to 66 Hz, single phase, (U.L. recognized)
Current	5 A (high line)
Dissipation	500 W max.
Mechanical	
Dimensions	24 in. h, 19 in. w, 15-3/4 in. d.
Weight	130 lb
Operating Environment	
Magnetic Tape Transport	
Ambient Temperature	32° to 131° F
Relative Humidity	20% to 80% (no condensation)
Altitude	10,000 ft
Magnetic Tape	
Storage Temperature	60° to 80° F
Humidity	60%
Cables	
CPU to TCU	Two, BC11-A-08
TCU to MTT	Two, 18 round T/P #91-7700 with M912 connectors for the TCU; cinch connectors for the MTT

1.4 OPERATION

Before attempting system operation ensure that:

1. Correct power is available to the MTT
2. The ON-LINE switch is depressed
3. The Write-Enable Ring is in position (if a write operation is desired).

Commence operation as follows:

1. Set the Word Count Register (WCR) to the 2's complement of the number of characters to be written on tape. (Do not load the WCR with zero for the write or read modes).

2. Set up the Bus Address Register to start at the desired location in memory.

3. Load the Control Register (CR) with the appropriate code for selecting the MTT to be used (bits 08 and 09).

4. Inspect the Status Register (SR). This reflects the status of both the TCU and MTT.

5. Clear the INHIBIT bit (Bit 00 in the SR).

6. Load the appropriate function into the Control Register, i.e., bits 00 through 04 and bit 06 (do not change the contents of bits 08 and 09 which selected the MTT).

The desired function (if legal) will execute automatically.

NOTE

The GO pulse should be asserted for every command by loading CR bit 00 with a 1.

CHAPTER 2
INSTALLATION

2.1 SITE CONSIDERATIONS

The cable between the TCU and the MTT should be maintained at the minimum possible length because of speed and noise considerations; therefore, the TCU must be mounted directly below the MTT (see Figure 2-1).

The H720-E power supply for the TCU mounts at the bottom, front-end of the cabinet. This arrangement ensures short dc power cables. For MTT installation, tape reel mounting, and tape threading, refer to Chapter 3 of the HP Operating and Service Manual. TCU and MTT operating temperatures are as specified in Paragraphs 1.2 and 1.3. Tape storage temperature should be in the range 60° to 80° F (relative humidity of 60%). Tape reels should be stored on edge in the original boxes. Damaged or warped reels should not be used.

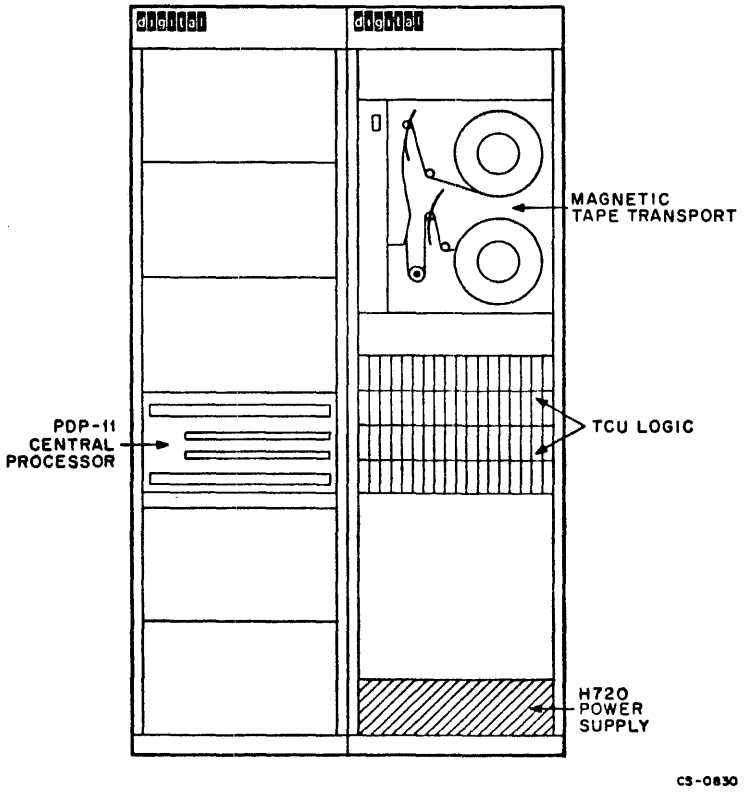


Figure 2-1 Cabinet Arrangement

2.2 CABLES

The following paragraphs describe the system cables.

2.2.1 Unibus

The Unibus connects to the TCU at slots AB01 (IN) and AB02 (OUT). Slot AB02 is used to house the M930 Unibus terminator if the TCU is the last device on the Unibus. One, 8-ft, Unibus cable BC11-08 is supplied with the TCU (see Figure 2-2).

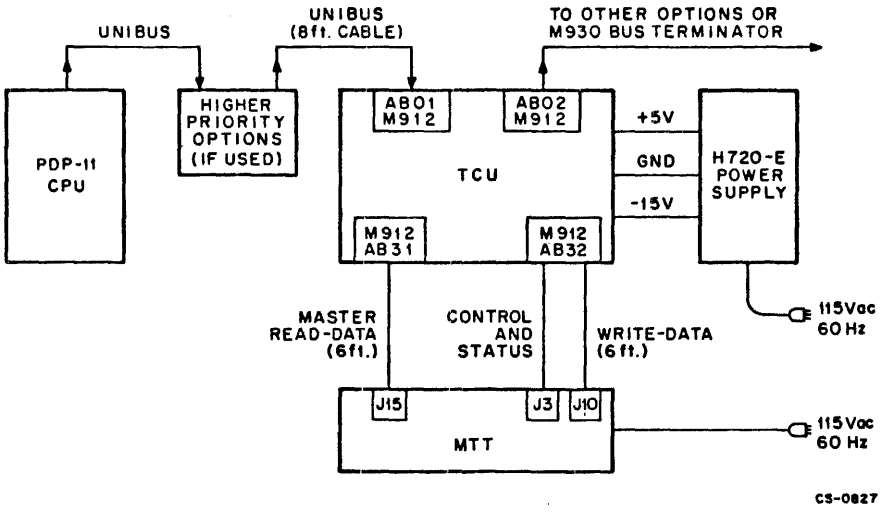


Figure 2-2 Cable Connections

2.2.2 TCU/MTT Cable

The TCU interfaces to the MTT by means of two cables. These are 6 ft long, and are round with twisted pair conductors. This is a standard telephone cable (DEC part number 91-7700). Type M912 connectors plug into the TCU at AB31 for the Master Read-Data cable and AB32 for the Write-Data and Control and Status cables.

The MTT ends of the cables connect to 48-pin cinch connectors (HP part number 1251-0335). Three of these connectors are used and are located at J3, J10, and J15.

2.3 GROUNDING

The grounds of the TCU power supply and the MTT should be connected together. This is achieved by bolting the two devices to the cabinet rails. A copper braid must connect the MTT cabinet with the PDP-11 system to which it is connected.

2.4 INITIAL OPERATION

The following paragraphs discuss the checkout and acceptance procedures performed in-house prior to shipment. These tests can also be used as an initial on-site turn-on procedure.

The heads and all tape paths should be cleaned before beginning the tests procedures and every 8 hours thereafter. A fresh reel of tape should be used.

2.4.1 Acceptance Procedure

To perform the acceptance procedure, load the diagnostic, MAINDEC-11-DZTRA, and run the following five tests:

NOTE

Manual Operation test should be run first. Refer to MAINDEC listing for instructions.

2.4.1.1 Test 1 - Run this test for ten passes. No errors are permitted. This test checks the control logic with minimum tape motion.

2.4.1.2 Test 2 - Run this test for ten passes. No errors are permitted. This test checks the ability of the logic to write the IDB from the load point and verifies that some illegal commands cannot be executed at the load point.

2.4.1.3 Test 3 - Run this test for a complete reel of tape. Allowable errors are as follows:

1. 4 MTE
2. 10 STE

This is a reliability test with continuous tape motion over the entire reel.

2.4.1.4 Test 4 - Run this test for one pass over a complete reel of tape. Allowable errors are as follows:

1. 4 MTE
2. 10 STE

This is a read compatibility test which reads tapes written by Test 3.

2.4.1.5 Test 5 - Run this test once. No errors are acceptable. This is a manual operation test for the TCU logic where the operator responds to commands from the program via the teletypewriter.

2.5 RELATED LITERATURE

The following documents contain information that supplements the material in this option description:

1. DEC Publications
    a. Logic Handbook
    b. PDP-11 Peripherals Handbook
2. Hewlett Packard Publications
    a. 7970-E, Operating and Service Manual
    b. 13195 A, Write Formatter Accessory Kit for the 7970-E.

CHAPTER 3
OPERATION AND PROGRAMMING

3.1 GENERAL

This chapter presents the TR79-FA transfer functions and codes. Included are detailed descriptions of the Status and Control Registers. Illegal commands, interrupts, and some programming limitations are also discussed.

3.2 REGISTER FORMATS

The TR79-FA registers are described below. Bus addresses associated with these registers are determined by jumpers on the M105 Address Module.

Register	Address
Control (CR)	764000
Status (SR)	764002
Word Count (WCR)	764004
Bus Address (BAR)	764006

The functional symbols used in Tables 3-1 and 3-2 have the following meanings:

W = Write (can be set by writing a 1 and cleared by writing a 0)
R = Read
S = Set by the Status
P = Cleared by PWR CLR or INIT
T = Cleared by INIT only
G = Cleared by GOP (GO Pulse)
C = Clears itself after a delay
Z = Cleared by GOP, PWR CLR, or INIT
E = Sets the ERROR bit, CR15
I = Causes an interrupt

3.2.1 Control Register (764000)

The Control Register (CR) provides the means by which the PDP-11 issues control functions and commands to the magnetic tape transport and its formatter. The CR is organized as shown in Figure 3-1. The function of each bit is explained in Table 3-1.

3.2.2 Status Register (764002)

The Status Register (SR) provides the means by which the TCU and MTT can be monitored by the program. The SR is organized as shown in Figure 3-2. The function of each bit is explained in Table 3-2.

Table 3-1
Control Register

Bit	Mnemonic	*	Function
00	GO BIT	W,Z	Produces GOP which causes the function to be executed into a command.
01 02 03 04	FNB 00 01 02 03	W,R	Function Bits. Contain the code of the command to be executed at GOP time. The codes are as follows: Code — Function 00 — Illegal 01 — Write 02 — Read Forward 03 — Illegal 04 — Space Reverse 05 — Illegal 06 — Illegal 07 — Erase 10 — Rewind 11 — Illegal 12 — Illegal 13 — Fast Forward 14 — Illegal 15 — Write IDB 16 — Write Tape Mark 17 — Offline
05	BUSY	R,P	Set with GOP when a legal function is executed into a command. Reset when the command and gap are done.
06	INT ENB	W,R,T	Interrupt Enable. Must be set to permit interrupts. Not cleared by PWR CLR.
07	CURDY	R,G	Control Unit Ready. Set when any of the following occurs: 1. End-of-Operation 2. MTT is put ON-LINE 3. PWR CLR is cleared (if ON-LINE) Reset with any of the following: 1. GOP is issued 2. PWR CLR is issued 3. OFF-LINE command is issued.

Table 3-1 (Cont)
Control Register

Bit	Mnemonic	*	Function
08 09	S Bit 8 S Bit 9	R,P	MTT Select Bits. Select one of four transports as follows: MTT 09 08 0 0 0 1 0 1 2 1 0 3 1 1 In some applications, all four select lines are OR'ed together to one transport.
10	MTRDY	S,R	READY Status of the selected MTT.
11	PWR CLR	W,R	POWER CLEAR. Clears the interface except INT ENB. Clears itself after 900 ms.
12 13	XBA16 XBA17	W,R,S,P	Extended Memory Address Bits. Allow addressing of memory banks over 32K as follows: Memory Range — Bit (XBA17) — Bit (XBA16) 0–32K — 0 — 0 32K–64K — 0 — 1 64K–96K — 1 — 0 96K–128K — 1 — 1
14	ILCMD	R,P,I	Set for any of the following illegal commands or functions: 1. Illegal functions 00, 03, 05, 06, 11, 12, 14. 2. If a command is issued while INHBT is set. 3. If a command is issued while CURDY is reset. 4. If a command is issued while MTT is not READY. 5. If WRITE data when Write Enable Ring is OFF. 6. If Write IDB command at other than load point. 7. If WRITE data from load point. 8. If Write TAPE MARK at load point. 9. If REVERSE from load point. 10. If REWIND from load point.

Table 3-1 (Cont)
Control Register

Bit	Mnemonic	*	Function
15	ERR	R,S,Z	Error Bit. Set when any of the following error conditions occur: 1. ABORT 2. ILLEGAL 3. BUS GRANT LATE 4. READ CNT 5. WT PARITY ERR 6. RD PARITY ERR 7. NON EXISTENT MEMORY 8. STE 9. MTE 10. MTT GOING OFF-LINE RESET by GOP or RESET.

*See Paragraph 3.2 for a description of the symbols used in this column.

Table 3-2
Status Register

Bit	Mnemonic	*	Function
00	INHBT	W,R	Inhibit Bit. Inhibits GOP. Must be cleared before a new command is issued. Set: At End-of-Operation Cleared: By writing a zero.
01	RWDS	R,S	Rewind Status. The selected MTT is rewinding.
02	FPTS	R,S	File Protect Status. Asserted when Write Enable is missing.
03	EOFF	W,R,S,Z	Tape Mark Status. Asserted when writing or reading a tape mark at EOB time.
04	IDBF	W,R,S,Z	Identification Burst Status. Asserted when writing or reading IDB at EOB time.
05	LDPS	R,S	Load Point Status. The selected MTT is at load point.
06	NXMF	R,S,Z,E	Non-Existent Memory Status. The TCU attempted to access a non-existent memory location.
07	EOTS	R,S,P	End-of-Tape Status. The selected MTT is at end of tape. Cleared also by REWIND or RD REV.

Table 3-2 (Cont)
Status Register

Bit	Mnemonic	*	Function
08	TMOUT	W,R,S,Z, E,I	TIME OUT. Set when an ABORT condition occurs in either of the following: 1. When any write operation is issued and the write status is not received back from the MTT 40 μs later. 2. When any write or read operation is issued and no EOB is received back from the MTT 1.5 sec later.
09	RDCNT	R,S,Z,E	Read Count. During a READ operation, the length of the record was *longer* or *shorter* than the value in the WCR.
10	ONLNS	R,S,I	ON-LINE Status. The selected MTT is ON-LINE.
11	BGL	W,R,S,Z	Bus Grant Late. In the read mode, a new character has arrived from the MTT before the previous character was accepted by the bus. In the write mode, a new character was not received from the bus by the time the Formatter indicated its acceptance of the previous character.
12	STEF	R,S,Z,E	SINGLE TRACK ERROR Flag. Set at EOB time when a single track error status is received from the MTT.
13	MTEF	R,S,Z,E	MULTIPLE TRACK ERROR Flag. Set at EOB time when a multiple track error status is received from the MTT. Indicates that an uncorrectable error has occurred and that the record must be rewritten on a new section of tape.
14	WPEF	R,S,Z,E	WRITE PARITY ERROR Flag. Set by the first write parity error in a record.
15	RPEF	R,S,Z,E	READ PARITY ERROR Flag. Set by the first read or read-after-write parity error in a record.

*See Paragraph 3.2 for a description of the symbols used in this column.

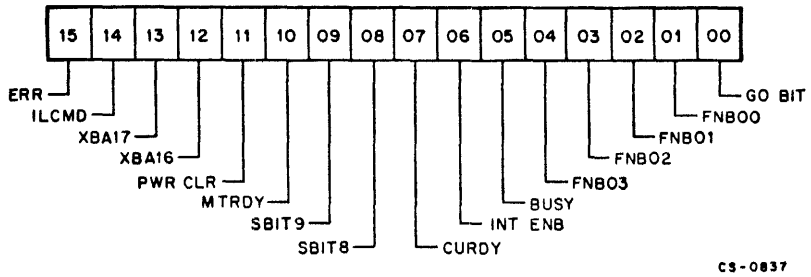


Figure 3-1 Control Register Format

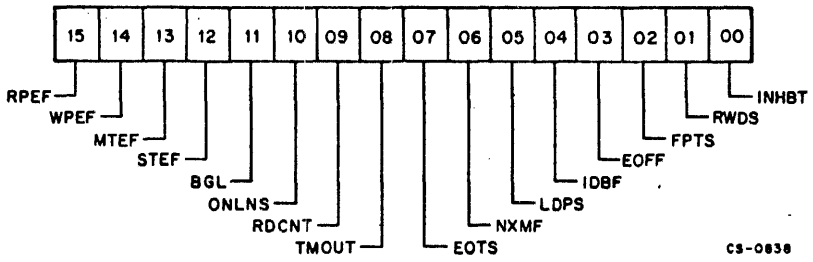


Figure 3-2 Status Register Format

3.3 INTERRUPTS

The TR79-FA interrupts the CPU on BR level 4 and causes it to trap to vector location 170 if INT ENB is set and any one of the following conditions occur:

1. ABORT
2. ILLEGAL
3. ON-LINE Status is asserted
4. ON-LINE Status is negated
5. When PWR CLR function ends
6. At the completion of any legal operation.

3.4 PROGRAMMING TECHNIQUES

The following are guides for programming the TR79-FA controller. After a power-up, the following must be accomplished in all instances:

1. Load the Control Register with all zeros; this selects the MTT.

2. Check the Status and Control Registers and verify that the following flags are set: MT RDY; ONLNS; CURDY; and LDPS (if starting from BOT).

3. Clear the INHBT bit in the Status Register.

To Write the IDB or TAPE MARK:

1. Load the Control Register with the code for IDB or WTM and set a one in the GO BIT.

2. Check if IDBF (or EOFF) is set when done. Also, keep testing CURDY for a set status. When this occurs, inspect BUSY. If BUSY is reset, the operation is complete.

NOTE
IDB may be written at load point only.

To Write, READ or ERASE:

1. Load Word Count Register and Bus Address Register with desired values.

2. Specify the desired function and set the GO BIT to a 1.

3. Keep testing CURDY for a set status. When CURDY sets and BUSY is reset, the operation is complete.

4. Inspect the ERROR Flag (CR bit 15). If bit 15 is set, investigate the appropriate error flag in the Status and Control Registers.

CHAPTER 4
THEORY OF OPERATION

4.1 GENERAL

This chapter must be read in conjunction with the MTT documentation: *HP Interface Guide, HP 13195A Write Formatter Accessory Kit Manual,* and the *HP Operating and Service Manual.* All three documents relate to the HP 7970-E phase-encoded Magnetic Tape Transport.

4.2 STATUS REGISTER (SR)

The Status Register is shown on Engineering Drawing TR79-T03. The SR is loaded from the bus by LDSR and read back into the bus by SR TO BUS. These two pulses are produced from the address selection logic on Drawing T02. Table 4-1 lists the SR bits with the significance of each. The content of the various Status Register lists is described in Chapter 3.

4.3 CONTROL REGISTER (CR)

The Control Register logic is shown on Drawing TR79-T04. This register is loaded from the bus by LD CR and its contents are placed on the bus by CR TO BUS. Table 4-2 lists the CR bits with the significance of each.

4.4 RECORDING FORMAT

The recording format (Figure 4-1) is ANSI/IBM compatible and is described briefly in the following paragraphs.

4.4.1 Format Architecture

The recording format for a phase-encoded 9-track magnetic tape contains the following:

1. Identification Burst (IDB)
2. Preamble
3. Data Record
4. Postamble
5. Tape Mark (TM)
6. Inter-Record Gaps (IBG)
7. Beginning-of-Tape Marker (BOT)
8. End-of-Tape (EOT)

Table 4-1
Status Register Bit Assignments

SR Bit	Significance
00	INHBT: Inhibit. Sets at completion of any valid operation and resets only under program control by writing a zero into the register bit. This bit must be cleared before loading the CR and issuing the GOP pulse. End of operation conditions that set INHBT include: STOP and RWDS.
01	RWDS: Rewind Status. This status is true so long as the MTT is rewinding and becomes false when the MTT is at load point.
02	FPTS: File Protect Status. This status is true when Write Enable Ring is not in use and becomes false when the Write Enable Ring is mounted on the reel.
03	EOFF: Tape Mark Status. Sets when EOFS and EOB coincide. Cleared by GOP or RESET.
04	IDBF: Identification Burst. Set at EOB time when the ID burst has just been written.
05	LDPS: Load Point Status from MTT. This status is true as long as the MTT is at load point and becomes false when no longer at load point.
06	NXMF: Non-Existent Memory Flag. Set when the NXM flip-flop on the M796 sets. Produces a 50 ns pulse through an M606 Pulse Generator to clear NXM.
07	EOTF: End-Of-Tape Status. Set when End-Of-Tape Status (EOTS) is asserted while in forward motion at normal or high speed. EOTS is asserted or negated when the leading edge of the EOT marker is detected by the photosense head assembly. This bit (EOTF) is reset under any of the following conditions: 1. If the tape leaves the reel in the forward direction. 2. When EOTS is negated during a rewind or RD reverse, if FAST FWD is not asserted. 3. If RESET is issued and EOTS is false. 4. When tape motion finally ceases during a FAST FWD command, the photosense head assembly stops about 0.187 in. before the leading edge of the EOT marker. EOTS becomes negated under these conditions but EOTF remains set. The bit, therefore, is cleared in this case if a rewind or RD reverse command is issued.
08	TMOUT: Timeout. Set when an ABORT condition occurs. The ABORT signal is produced for either of the following conditions: 1. When any write function (ANY WT) is executed into a command at GOP time and the write status level WRTS is not received back from the MTT after 40 μs delay. 2. If the MTT does not respond with an EOB within 1.5 sec after any of the following commands is issued: WRITE WID READ EOFC SP REV

Table 4-1 (Cont)
Status Register Bit Assignments

SR Bit	Significance
09	RDCNT: Read Count. Represents record length discrepancy as compared with word count when in read mode. This bit sets for a short record (actual record shorter than word count), or long record (actual record longer than word count).
10	ONLNS: On-Line Status. The selected MTT is on-line.
11	BGL: Bus Grant Late. In write mode, BGL sets whenever the Input Buffer Flag (IBFLG) remains reset (new character not received from the bus), when Data Accepted (DAT ACPT) is received from the MTT (for the previous character) if the WCR did not overflow. In read mode, BGL sets when REQ BUS remains set and a new RD CLK pulse is received from the MTT.
12	STEF: Single Track Error Flag. Sets at EOB time when a single track error is received from the MTT. This also causes the ERROR bit in the Control Register to set.
13	MTEF: Multiple Track Error Flag. Sets at EOB time when a multiple track error is received from the MTT. This also causes the ERROR bit in the CR to set. MTE specifies that an uncorrectable error has occurred and the block must be re-written on a new section of tape (or re-read). The control for this operation is not included in the hardware and must therefore be accomplished by the software.
14	WPEF: Write Parity Error Flag. Sets when a write parity error is received from the parity check logic. Write parity is generated and checked while data is being transferred from the first to the second buffer stage. This bit is set only by the first error detected in a record. Setting this bit causes the ERROR bit in the CR to set.
15	RPEF: Read Parity Error Flag. Sets when a read parity error is detected. Read parity is generated and checked for read-after-write and read-only modes. Only the first read parity error in a record is reported.

4.4.2 Definitions

Before data is written on tape, the tape is erased to a specified magnetic flux polarity. Erasure is achieved by passing the tape across a dc erase head before writing.

1. Erase: The erase function magnetizes the entire width of tape so that the physical beginning of tape (rim end near the BOT) becomes a north-seeking pole. Tape is fully saturated in the erased direction in the initial gap and interblock gap area.
2. When writing phase-encoded tape, magnetic flux reversals are written for both 1 and 0 bits. A 1 data bit is defined as a flux reversal to the polarity of the inter-block gap (IBG), when reading in the forward direction. The IBG itself is a dc erased section of tape.
3. A 0 data bit is defined as a flux reversal to the polarity opposite that of the IBG, when reading in the forward direction.
4. A flux reversal is written at the nominal midpoint between successive 1 bits or 0 bits, to establish proper polarity. This is known as phase flux reversal. See Figure 4-2.

The recording density is 1600 characters per inch (cpi). The nominal character spacing exclusive of phase flux reversals, is 0.625×10^{-3} in. It is important to note that density statements in cpi are always exclusive of phase flux reversals.

Table 4-2
Control Register Bit Assignments

Bit	Significance
00	GO BIT: Must be issued with each command. When a command is issued with GO BIT set, a 1 μs waiting period elapses before the GO Pulse (GOP) is generated. GOP (T06) causes the command, if legal, to be executed in the TCU. Commands are investigated for validity during the 1 μs period. When an illegal command is detected, the following occurs: 1. The command is not executed. 2. The Illegal Command bit (ILCMD) in the CR sets. 3. INTF flag sets causing an interrupt to be generated.
01, 02, 03, 04	FUNCTION BITS: These bits define the command functions. These bits are changed only by writing 1s or 0s. Of the 16 possible combinations, only 9 are valid; all others are illegal. See Table 4-3.
05	BUSY: The TCU BUSY flag sets when one of the nine valid commands listed in Table 4-3 is issued. This flag is reset as a result of any of the following terminal conditions: SET SDE, STOP, RWDS, CLR OFL, and RESET.
06	INT ENB: Interrupt Enable. This bit must be set or interrupts are inhibited.
07	CU RDY: Control Unit Ready. This flag, when set, specifies that the TCU is ready to receive a command. When a legal command is issued, the CU RDY flip-flop resets specifying that the TCU is busy (executing a command). Illegal commands do not reset CU RDY as GOP is not generated. This flag is set by any of the following conditions: 1. When EOPF is set at the end of an operation, if the MTT is ON-LINE and the TCU is not in a PWR CLR mode. 2. When the MTT is switched ON-LINE by depressing the pushbutton switch at the front of the MTT housing. 3. When the PWR CLR flip-flop is reset (900 ms after being set) provided the MTT is ON-LINE. The CU RDY flag is reset (TCU busy) under the following conditions: 1. When the OFLIN command is issued (the MTT is turned off-line). 2. When the PWR CLR flip-flop is set (i.e., the TCU is in PWR CLR mode). 3. When a legal command is issued (GOP is produced).
08, 09	S BITS: Select Bits. These bits select one of four tape transports as listed in Table 4-4. In certain applications all four decodes are OR'ed to address the same transport. In such configurations it is not necessary to load bits 08 and 09.

Table 4-2 (Cont)
Control Register Bit Assignments

Bit	Significance
10	MTRDY: Magnetic Tape Ready. This bit reflects the MTT Ready Status. It is set whenever the MTT is in the ready condition.
11	PWR CLR: This is the power clear bit used to clear the TCU. When this bit is set under program control, it performs the following: 1. Produces a 20 ms pulse which is OR'ed with BUS INIT to produce RESET. 2. Reset the CY RDY flag in the Control Register signifying that the TCU is busy while PWR CLR flip-flop is set. 3. It triggers a 900 ms delay at the end of which PWR CLR is cleared and CU RDY is set.
12, 13	EXTENDED BUS ADDRESS BITS: These are the extended bus address bits that provide A (17-16) for extended memory transfers. When BAOVFL (Bus Address Overflow) becomes true, the first 32K memory block is full and A16 sets allowing transfers to memory in the 32K–64K range. The next BAOVFL resets XBA16 and set XBA17, to permit access to locations between 64K and 96K. When both XBA17 and XBA16 are set, access is allowed between 96K–128K. To summarize: Memory Range — XBA17 — XBA16 0–32K — 0 — 0 32K–64K — 0 — 1 64K–96K — 1 — 0 96K–128K — 1 — 1
14	ILCMD: Illegal Command. This bit (T05) sets when an illegal command is issued as defined in Table 3-1, bit 14.
15	ERR: Error. This bit sets when any of the following error conditions occur: 1. BGL; Bus Grant Late for either write or read NPR's. 2. RD CNT; during a READ operation when the record length is shorter than the word count or longer than the word count. 3. WPEF; when the WRITE PARITY ERROR flag is set. 4. RPEF; when the READ PARITY ERROR flag is set.

Table 4-2 (Cont)
Control Register Bit Assignments

Bit	Significance
15 (Cont)	5. STE; when a Single Track Error is detected. 6. MTE; when a Multiple Track Error is detected, (this includes errors in the Parity Channel). 7. OFLNP; when the MTT is commanded to go Off-Line or goes Off-Line accidently. 8. ABORT 9. ILP; Illegal Pulse produced when ILLEGAL is asserted.

4.4.3 Track Identification

The ANSI and IBM tracks are configured in Figure 4-1* as follows:

ANSI Track	1	2	3	4	5	6	7	8	9
IBM Track	5	7	3	P	2	1	0	6	4
Binary Weight	2^2	2^0	2^4	P	2^5	2^6	2^7	2^1	2^3
ASCII Bits	b_3	b_1	b_5	P	b_6	b_7	Z	b_2	b_4

*P = Parity bit (odd), Z = Zero bit.
b_1-b_7 correspond to the bit assignments in the ASCII code.

4.4.4 Parity

Only character parity is used in phase encoded recording. Character parity is odd.

4.4.5 Identification Burst (IDB)

The phase-encoded recording is identified by a burst of recording at the BOT marker. This burst consists of 5600 bits of alternate 1 bits and 0 bits in track P; all other tracks are erased. The IDB begins a minimum of 1.7 in. before the trailing edge of the BOT marker, but ends at 0.5 in. before the first block. For the TR79-FA, the IDB begins 2.425 in., nominal, before the trailing edge of the BOT, and ends 2.6 in., nominal, before the first data block. The IDB is written automatically by the Formatter upon command from the TCU. No IDB data is transferred from or to the TCU when the WID (Write IDB) command is issued to the MTT.

4.4.6 Preamble

Preceding data in each block is a preamble consisting of 41 characters. Forty of these characters contain 0 bits in all tracks followed by a single character containing 1 bits in all tracks (see Figure 4-1).

The Preamble synchronizes the detection logic so that 1s and 0s are identified correctly when reading the data bytes that follow. The Preamble is written automatically by the MTT upon receipt of the WPA command from the TCU. No data is exchanged between the TCU and the MTT when writing or reading the Preamble.

4.4.7 Postamble

A Postamble follows the data in each block. The Postamble consists of 41 characters, the first of which contains 1 bits in all tracks followed by 40 characters containing 0 bits in all tracks. The Postamble, therefore, is a mirror image of the Preamble (Figure 4-1). The Postamble is provided for accomplishing electronic synchronization and is written automatically by the MTT upon receipt of the EOD (End-of-Data) command from the TCU. No data is exchanged between the TCU and MTT during writing or reading of the Postamble.

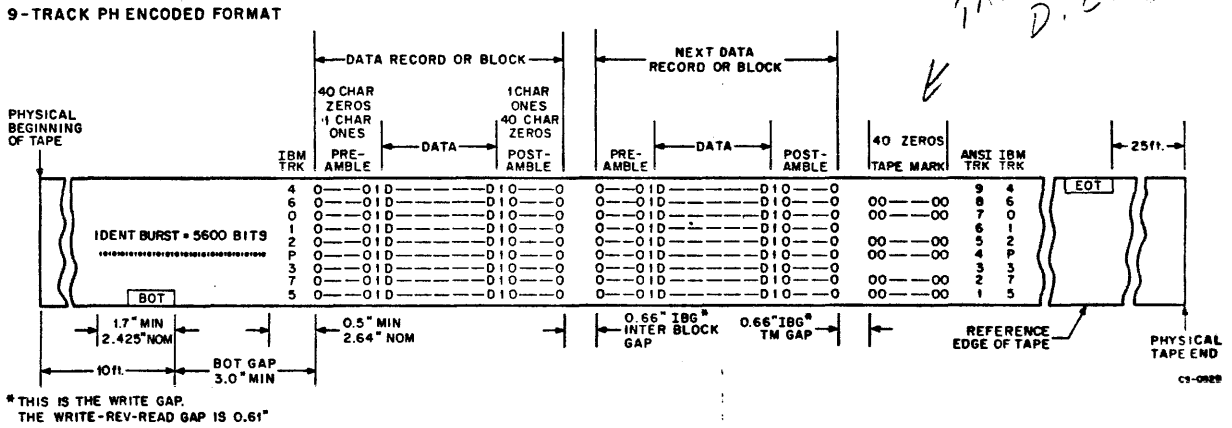


Figure 4-1 9-Track PH-Encoded Format

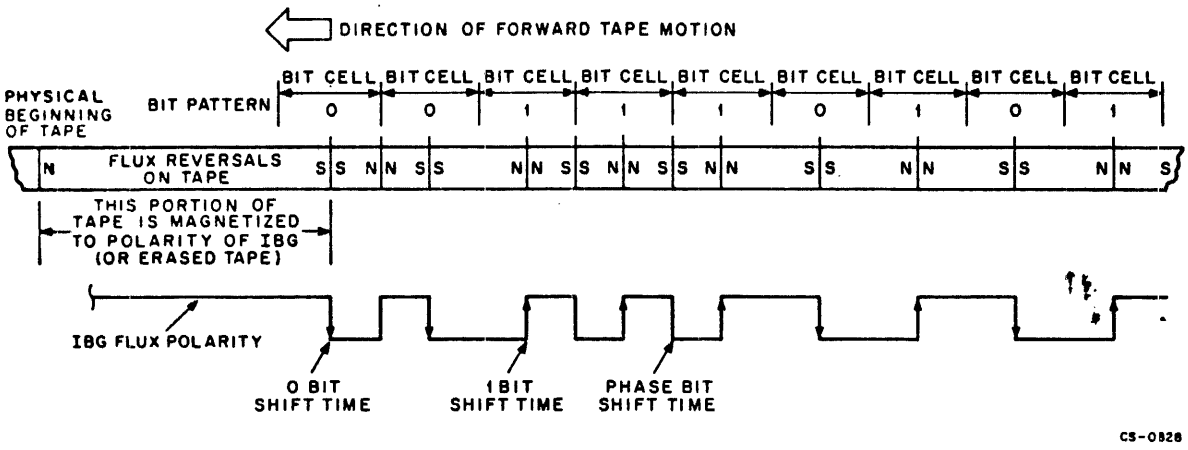


Figure 4-2 Phase-Encoded Write Waveforms

Table 4-3
Command Function Decoding

Command	Octal Code	D04	D03	D02	D01
ILC 00	00	L	L	L	L
WRT	01	L	L	L	H
RD FWD	02	L	L	H	L
ILC 03	03	L	L	H	H
SP REV	04	L	H	L	L
ILC 05	05	L	H	L	H
ILC 06	06	L	H	H	L
ERS EN	07	L	H	H	H
RWD EN	10	H	L	L	L
ILC 11	11	H	L	L	H
ILC 12	12	H	L	H	L
FAST FWD	13	H	L	H	H
ILC 14	14	H	H	L	L
WID B	15	H	H	L	H
WEOF	16	H	H	H	L
OFLIN	17	H	H	H	H

Table 4-4
Transport Selection Decoding

MTT	Octal Code	D09	D08
0	00	L	L
1	01	L	H
2	02	H	L
3	03	H	H

4.4.8 Data Record

Information is recorded on tape between the Preamble and Postamble. The combination of Preamble-Data-Postamble makes up the data block. The ANSI specifications for phase-encoded tapes stipulates that the data portion of a block shall contain a minimum of 18 characters and a maximum of 2048 characters.

4.4.9 Tape Mark (TM)

A Tape Mark is a special control block consisting of at least 40 zero bits written in tracks 1, 2, 4, 5, 7, and 8 (ANSI). Tracks 3, 6, and 9 are dc erased. The TM is preceded by a normal IBG (of 0.66 in.).

4.4.10 Inter-Block Gap (IBG)

The ANSI specification stipulates the following measurements for the IBG:

Minimum	0.5 in.
Nominal	0.6 in.
Maximum	25 ft

In the TR79-FA, the IBG for WRITE-WRITE is about 0.66 in. while for WRITE-BACK SPACE-READ the IBG is about 0.61 in.

The gap between the last bit in the IDB and the first recorded character is 2.6 in. nominal for the TR79-FA.

IBG generation and checking logic is shown on Drawing TR79-T08 and T09. The basis of the operation is a two-stage counter that is started and stopped when a time measurement is required.

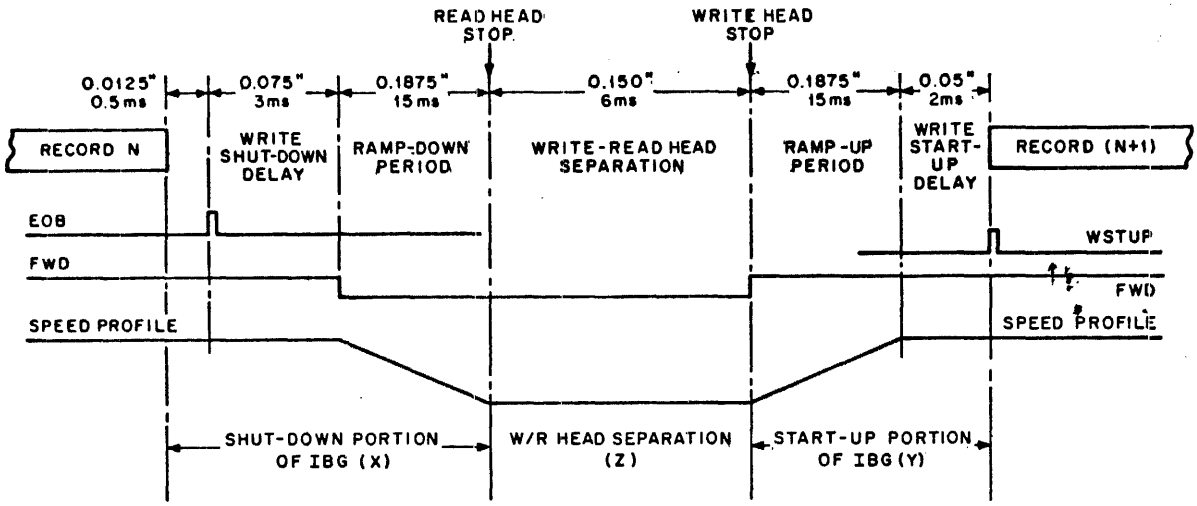
4.5 GAP COMPOSITIONS

Normally, the gap between two blocks comprises two sections. The first section is generated at completion (the shut-down stage) of the block just completed; the second section is generated while starting-up to write a new block or record. The size of the gap obtained during the write operation depends on whether a block that has just been written is followed by another written block or the written block is followed by a Space Reverse-Read Forward operation. The IBG corresponding to the latter is slightly shorter than the IBG produced in the former case. The reason for this is as follows: If the record just written is to be read, a SPACE REV function must be produced. Issuing this command causes the write current to be turned off in the Write-and-Erase Heads, thus producing a footprint of unwanted information on tape; this is commonly referred to as CIG or glitch. When SPACE REV and READ FWD are completed, the Read-Write Heads are brought to a halt slightly before the previous stopping position of the heads. This new positioning allows the Write-and-Erase Heads to go over the footprint and erase it before the new block is written, thereby producing a clean gap that is slightly shorter than the gap obtained normally. See Paragraphs 4.5.2.1 and 4.5.2.2.

4.5.1 Gap Shutdown

When in the start/stop mode of operation, the tape stops after writing the last character in the block. The position of the Read Head determines the size of the Write or Read Shut-Down portion of the gap, Figure 4-3. The position of the Read Head can be determined as described in the following paragraphs.

4.5.1.1 Write Shut-Down – When the last character and the Postamble of a particular block are written on tape, the MTT responds with EOB which produces BLK END (T09). This signal (BLK END) causes the COUNT ENB flip-flop to set, allowing the 2-stage gap timing counter (Sheet T08) to start counting. The first stage of the counter is a divide by 40 and is driven by clock pulse 2DF, (2DF clock is produced in the MTT and runs continuously). The output pin of gate B13 (T08) issues a pulse every 0.5 ms; therefore, the desired delay, in half milliseconds, can be obtained by decoding counter stage TC0 through TC7. Signal BLK END also generates SET SDE (Sheet T09) which sets SHDWN ENB (T08). This flip-flop enables WGDLY to be generated 3 ms following BLK END. Signal WGDLY causes SHDWN to be produced.



DELAY LIST

COMMAND	START-UP DELAY (ms)	SHUT-DOWN DELAY (ms)
WRITE	2	3
READ	0	1
RD REV	0	1
WIDB	–	3
WTM	2	3
ERASE	–	3

TOTAL GAP LENGTH = X+Y+Z

CS-0831

Figure 4-3 Write Gap Timing

Signal SHDWN performs the following:

1. Clears the SHDWN ENB flip-flop, thus terminating the Write Shut-Down Delay WGDLY.

2. Clears the Command Register which includes the clearing of FWD, thus causing the MTT Capstan Motors to ramp-down.

3. Sets BUSY once more during the current block to imply that the TCU is still busy while shut-down is in process.

Further, the clearing of FWD qualifies pin F1 of gate A23 (T09). This gate asserts 17 ms after FWD is cleared, thereby clearing the MOTION flip-flop and producing STOP. This short pulse is used to:

1. Clear the COUNT ENB flip-flop, thus stopping the 2-stage counter.

2. Clear BUSY, thus signaling the completion of the current block and its associated portion of the gap.

The Read and Write Heads are now at a standstill near the middle of the gap (Figure 4-3).

4.5.1.2 Read Forward Shut-Down – The Read Gap Delay pulse RGDLY (T08) is produced in much the same manner as described in Paragraph 4.5.1.1 except that the delay is only 1 ms rather than 3 ms. The purpose of this arrangement allows the CIG (or footprint) left on tape during a Write-Back Space-Read to be erased if a new block is being written; see Paragraph 4.5 for more detail.

4.5.1.3 Identification Burst Shut-Down – An EOB is transmitted from the MTT to signify writing of the ID BURST. Signal BLK END is generated from EOB and is used to initiate the proper IDB gap to be followed by the shut-down sequence (Figure 4-4).

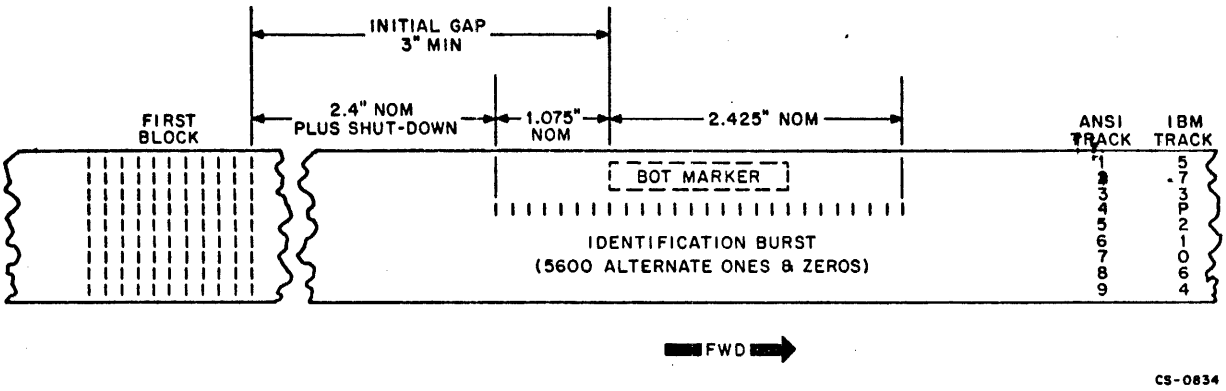


Figure 4-4 Identification Burst Positioning

Signal BLK END sets COUNT ENB which starts the counter. Gate E09-N1 (Sheet T08) qualifies when TC6 and TC7 and WIDB EN are true. This occurs 96 ms following EOB and corresponds to 2.4 in. of tape (at 25 ips). Signal LDP GAP is also produced and performs the following:

1. Generates CLR TC (T09) which clears the counter momentarily and allows it to restart.
2. Generates SET SDE which sets the SHDWIN ENB flip-flop.
3. Clears the BUSY flip-flop.

With the counter starting a new count cycle and SHDWN ENB set, Gate A13-P2 (Sheet T08) qualifies when TC1 and TC2 are true, i.e., after a 2 ms delay at which time WGDLY is produced.

Signal WGDLY produces SHDWN (because BUSY is reset). Once SHDWN is produced, the sequence of events that follows is exactly the same as described in Paragraph 4.5.2.1.

No attempt is made to produce a standard start-up procedure when the WIDB command is issued from load point because no gap is required before the IDB.

4.5.2 Gap Start-Up

When in the Start/Stop mode of operation, tape motion start-up from the middle of a gap, ramp-up, and start-up delays are determined as a function of Read Head and Write Head positions (Figure 4-5).

4.5.2.1 Write Start-Up – When the write command is asserted, FWD, WSWC, and WT ENB are also produced. FWD causes the MOTION flip-flop to be set, and this in turn enables the 2-stage counter. Also, GOP, which was used to clock the MTT Command Register, causes COUNT ENB to set allowing a count cycle to occur. Gate B13 pin P2 (T08) is qualified when a count of 34 has been achieved. This represents 17 ms; therefore, WSTUP is asserted 17 ms after the WRITE command is selected and, as a result, WSTUP produces GAP END which clears COUNT ENB. This causes the counter to stop which signals the end of the ramp-up period and start-up delays and is, therefore, the end of the gap (Figure 4-3). WSTUP is also used to cause the Preamble to be written on tape by setting the WPAMB flip-flop (T11). The start-up portion of the gap is determined from the stop position of the Write Head, the Write Head (W Head) being 0.150 in. ahead of the Read Head (R Head).

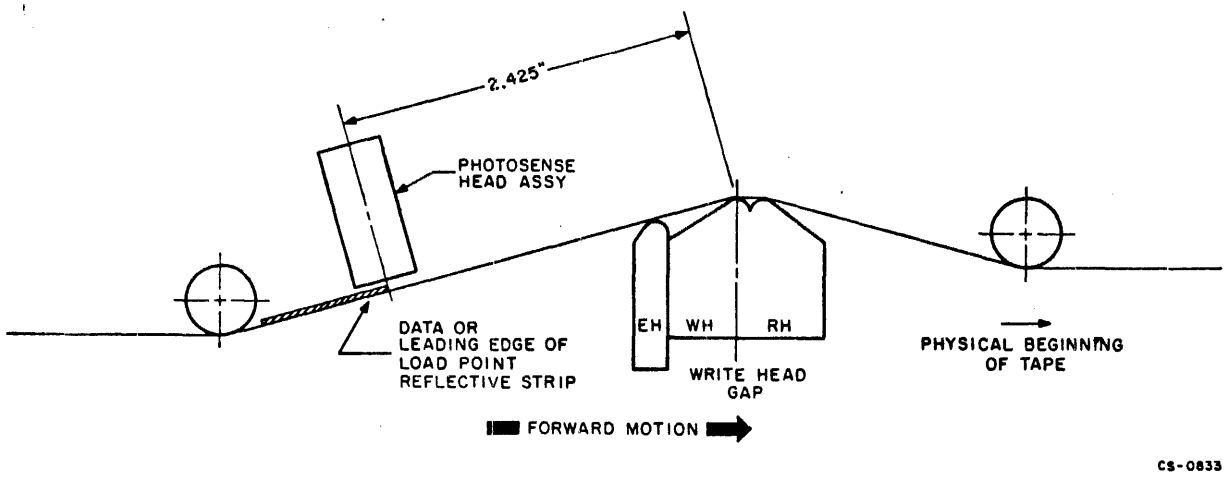


Figure 4-5 Head Positioning

The total size of the IBG when writing is the sum of three quantities:

SHUT-DOWN Portion = 0.2750 in.
Write-Read Head Separation = 0.1500 in.
START-UP Portion = 0.2375 in.
Write IBG = 0.6625 in.

4.5.2.2 Read Start-Up – When a READ FWD command is issued, the sequence of events that follows is much the same as that for a WRITE except that RSTUP is produced in place of WSTUP, and the Read Start-Up delay is 12 ms. Therefore, for a READ FWD operation, the TCU starts looking for data while the Read Head is still in the gap. However, if it desired to read a block immediately after it is written, i.e., if the operation is WRITE-BACK SPACE-READ, then the size of the IBG is calculated as follows (see Figure 4-3).

SHUT-DOWN Portion = 0.2250 in.
Write-Read Head Separation = 0.1500 in.
START-UP Portion = 0.2375 in.
Read IBG = 0.6125 in.

4.5.3 Tape Mark Gap
Operations for Tape Mark Shut-Down and Start-Up are shown in Figure 4-6 and described in the following paragraphs.

4.5.3.1 Tape Mark Shut-Down – When TAPE MARK is written by the Formatter, the MTT issues EOB signifying that TAPE MARK has been completed. Signal EOB produces BLK END which is used on drawings TR79-T08 and T09 to produce gap shut-down in exactly the same manner as described for Write Shut-Down in Paragraph 4.5.1.1. Refer also to the timing diagram, Figure 4-3.

4.5.3.2 Tape Mark Start-Up – When the command WEOF to write TAPE MARK is issued, WEOF EN and COUNT ENB are both set. The latter allows the counter to start a time cycle and the former allows Gate B13-P2 to qualify when TC1 and TC5 are true, thus producing WSTUP. The sequence of events that follow is exactly the same as described for Write Start-Up. See Paragraph 4.5.2.1 and Figure 4-3.

4.5.4 Erase Gap
Operations for Erase Gap Shut-Down and Start-Up are discussed in the following paragraphs.

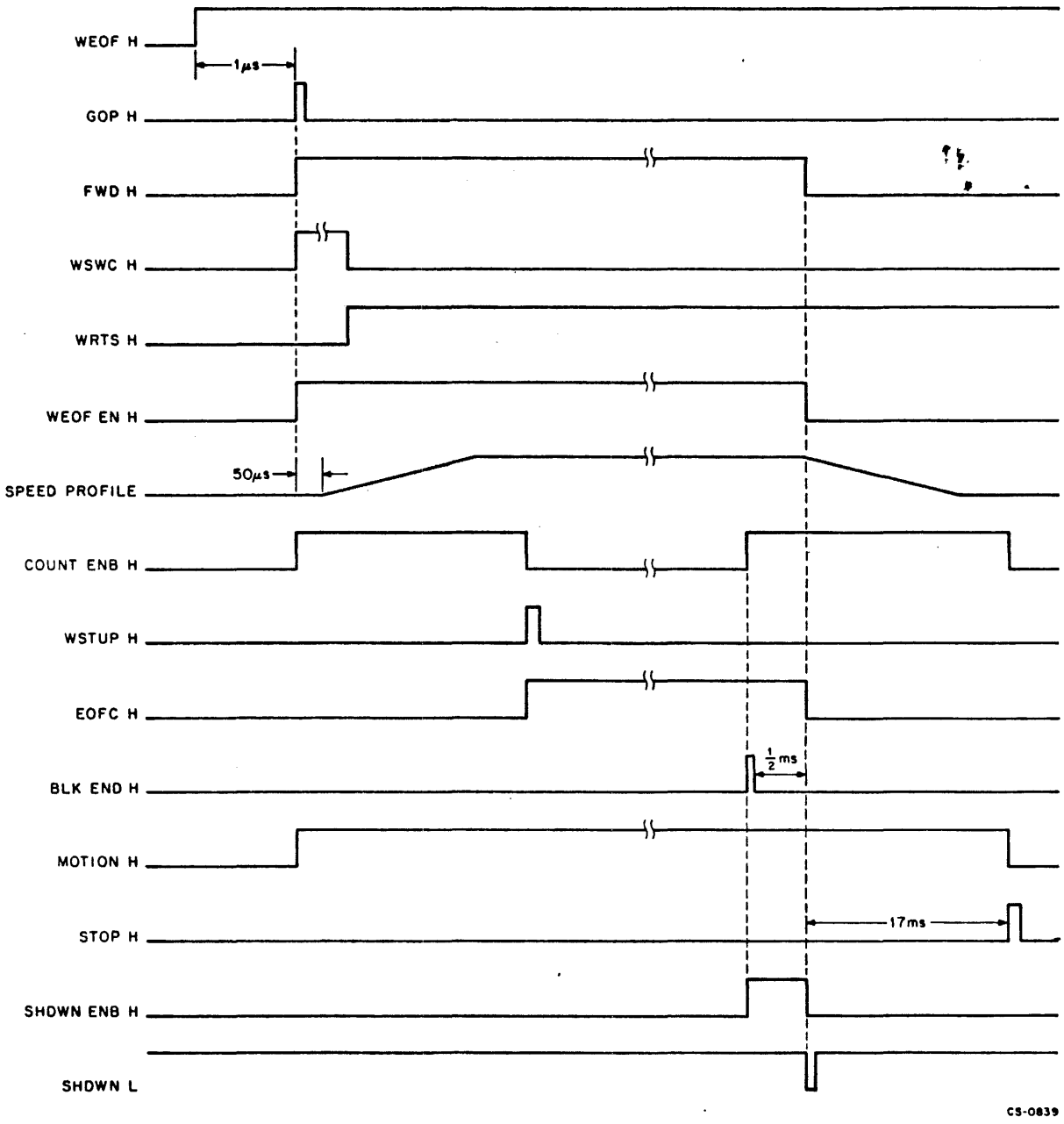


Figure 4-6 Write Tape Mark Timing

4.5.4.1 Erase Shut-Down – When an ERASE command is completed, it is necessary to produce an orderly shut-down. The MTT does not produce an EOB in this case; therefore, BLK END (T09) was forced at end of the erase operation by CLR ERS (produced on Drawing TR79F-T07 when WCR overflows). Once BLK END is produced, the shut-down sequence follows the same sequence as the Write Shut-Down. See Paragraph 4.5.1.1 and Figure 4-3.

4.5.4.2 Erase Start-Up – No attempt is made to obtain a standard start-up when erasing. In fact the erase operation starts in the middle of the gap as soon as motion starts.

4.5.5 Read Reverse Gap

Both SP SHUT-DOWN and SP REV START-UP are accomplished exactly the same way as for the READ FWD case; see Paragraphs 4.5.1.2 and 4.5.2.2 respectively.

4.6 MTT COMMANDS

The commands issued to the MTT are shown on sheets T07 and T11 and are listed in Table 4-5. All commands are transmitted to the MTT via TTL drivers (T17) over a twisted pair cable (T20).

Table 4-5
TCU to MTT Commands

TCU Command	Command Destination		Function
	MTT	Formatter	
FWD	CF		Forward Motion
REV	CR		Reverse Motion
FAST	CH		High Speed Forward
RWND	CRW		Rewind
LOCAL	CL		Off-Line Command
WT ENB		EN	Write Enable
WSWC	WSW		Write Command
WID		WIDB	Write IDB
EOFC		WTM	Write Tape Mark
WPAMB		WPA	Write Preamble
EODAT		EOD	Generates Write Postamble

Another set of commands are produced for use in the TCU only and are not issued to the MTT. These include:

WRITE
READ
SP REV
ERASE.

4.6.1 FWD

This command is produced when any of the following control functions is issued:

WRT
WEOF
WIDB EN
ERS EN
RD FWD
FAST FWD.

The above six functions are OR'ed at gate B13-F1 to produce FWD EN which enables the FWD flip-flop and causes it to be set at GOP time. Signal GOP is produced 1 μs after the assertion of any function. The FWD command causes the MTT to move forward at 25 ips. The FWD command is cleared under the following conditions:

1. CLR CMD. This is produced from any of the following:

   SHDWN
   SET BACK
   CLR ERS
   RESET

2. ABORT. This is produced either when any write or any read command is issued and no EOB is produced 1.5 sec later, or when ANY WT is issued and WRTS (Write Status) is not received from the formatter 40 μs later.

4.6.2 REV

This command is produced when the SP REV function is issued. The REV flip-flop is set at GOP time. The REV command is transmitted to the MTT and causes it to move in reverse at 25 ips. The REV command is cleared under the same conditions as the FWD command described in Paragraph 4.6.1.

4.6.3 FAST

This command is produced at GOP time when the program issues the function FAST FWD. It causes the transport to move forward at 160 ips. This command is cleared when the End-of-Tape Status (EOTS) is asserted.

4.6.4 RWND

This command is produced at GOP time when the program issues the function RWD EN. The command causes the transport to rewind back to the load point at 160 ips.

4.6.5 LOCAL

This command is produced at GOP time when the program issues the function OFLIN. It causes the transport to go off-line. The LOCAL command is also unconditionally produced whenever the PWR CLR signal is generated by the program while the MTT is rewinding. This also causes the transport to go off-line. The LOCAL command is cleared by the assertion of the ONLNS status when the MTT is placed on-line by manually depressing the ON-LINE button at the MTT front panel.

4.6.6 WT ENB

This command is asserted at GOP time whtn the ANY WT signal is true. Signal ANY WT is produced as an OR function of WRT, WEOF, WIDB EN, or ERS EN.

The WT ENB command is produced and used in the TCU for all write and erase operations. It is transmitted to the Formatter card in the MTT for all write operations, i.e., Write, WTM, WPA, and EOD together with the WSW command. WT ENB is inhibited from being transmitted to the Formatter during an erase operation.

4.6.7 WSWC

This is the SET WRITE command produced at GOP time when WSW EN is asserted. This command is used to produce the WSW signal to the formatter when the Write Enable Ring is in position. Signal WSW must be asserted for all write and erase operations. The WSWC command is reset when the Write Status (WRTS) level is received back from the Formatter 20 μs after assertion of WSWC.

4.6.8 WID

This command is issued when the IDB is to be written while the tape is positioned at load point. The program produces the function WIDB EN which performs the following:

1. Places a true signal on the D-input of the WID flip-flop
2. Causes FWD EN to be produced.

When GOP is issued, the FWD command is generated causing the tape to move forward from load point. When the data edge of the load point (Figure 4-5) clears the Photosense Head asembly, the WID flip-flop is triggered with the negation of the Load Point Status (LDPS) signal and writing the IDB commences. The dimensions of IDB and its associated gap are shown in Figure 4-4. The WID command is cleared by BLK END which is produced 20 bit times after completion of the IDB.

4.6.9 EOFC

This command is produced when it is desired that the Tape Mark be written anywhere on tape except load point. Refer to Figure 4-6 for timing. The program produces the function WEOF which performs the following:

1. Produces FWD EN
2. Places a true signal at the D-input of the EOFC flip-flop.

When GOP is generated (GOP appears 1 μs after WEOF is issued), the FWD command is asserted and tape motion begins, the Gap Start-Up sequence is initiated; when WSTUP is produced, the EOFC command is asserted, and the Write TAPE MARK operation begins. (See Paragraph 4.5.4.) When the Tape Mark is written, EOB is produced by the MTT 20 bit times later and is used to produce Gap Shut-Down.

4.6.10 WPAMB

When it is desired that a record be written and the WRITE command is issued by the program, the TCU hardware generates WPAMB which causes the Formatter to write the Preamble at the start of every record. Forty characters (all 0s) followed by one character (all 1s) are written automatically by the Formatter when its WPA input is asserted. The WPAMB command is produced when both WRITE and WRTS are true. This places a high level at the D-input of the WPAMB flip-flop. When the start-up portion of the gap is completed, the pulse WSTUP is generated. This pulse performs the following:

1. Sets the WPAMB flip-flop, thus causing the formatter to start writing the preamble, which lasts for about 1 ms

2. Generates a 100 μs delay at the expiration of which a pulse, FRST WREQ, is produced. This pulse generates the first NPR request for writing data on tape.

Approximately two formatter clock pulses following assertion of WPA, the FRDY signal is negated. The change in level of FRDY triggers a pulse generator (B19-R2) which clears WPAMB.

4.6.11 EODAT

This command (EODAT) is issued by the TCU to the Formatter during a WRITE operation. The command is issued when the last character has been taken by the Formatter from the output buffer and causes the Postamble to be written. See Figure 4-7.

The conditions for producing this command are as follows:

1. When gate B25-V1 qualifies, it places a high at the D-input of the EODAT flip-flop.

2. The last character received by the Formatter produces a DAT ACPT pulse which is delayed 18.5 μs and clocks the EODAT flip-flop to the set state. This causes the Formatter to first start writing the Postamble and to then produce a final DAT ACPT pulse that clears the EODAT flip-flop. Flip-flop EODAT can also be unconditionally set when in the WRITE mode if either NXM or BGL occur. Either of these two Unibus errors termintes the writing of a record and causes an orderly shut-down.

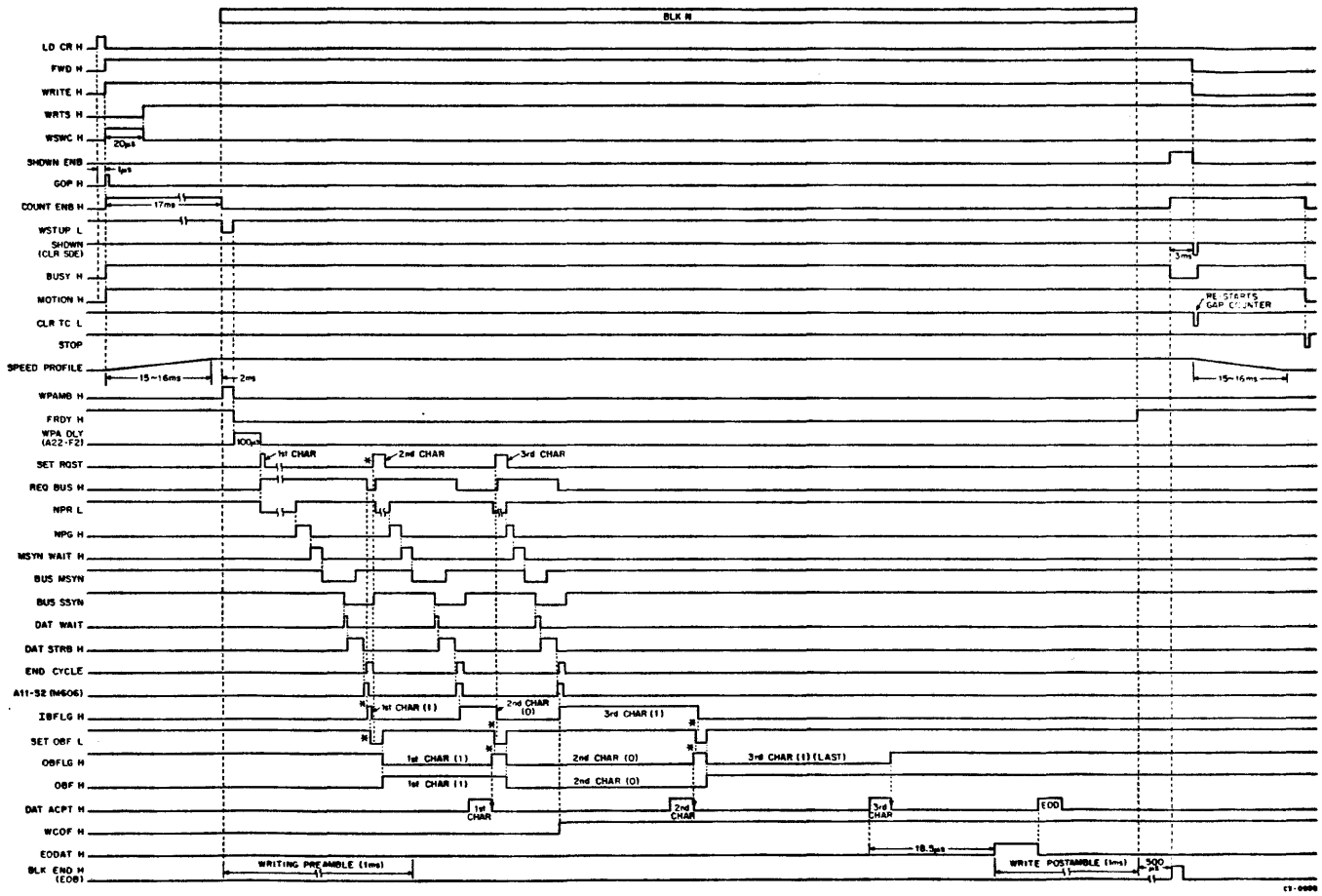


Figure 4-7 Write Timing

4.6.12 WRITE

This command is produced when the function WRT is issued by the program and GOP becomes asserted. The command is used internally in the TCU and is not transmitted directly to the MTT. When this command is generated, the following signals are produced: ANY WT, FWD EN, WSW EN, and WT ENB. In addition, this command is used throughout the TCU to perform such tasks as write gap generation, enable for NPR requests, and buffer control.

When the WRITE command is asserted, the write operation is carried out as described in the following paragraphs. Refer to the write timing diagram, Figure 4-7.

1. *First Character:* When the start-up phase of the Write Gap is completed, pulse WTSUP is produced to generate the WPAMB command and, after a 100 μs delay, FRST WREQ. FRST WREQ is OR'ed with Write NPR request and Read NPR request (T11) to produce SET REQ which sets REQ BUS and thus produces the first NPR request (T14). When NPG is produced, the DMA cycle that follows results in generation of DAT STRB and END CYCLE. END CYCLE increments the WCR and BAR registers and terminates the DMA cycle. (See the *PDP-11 Interface Manual* for further information on the DMA cycle.) The DAT STRB pulse performs two tasks: (1) it direct sets the nine bits of the input buffer with the first character from the Unibus, and (2) the trailing edge of DAT STRB produces a 50 ns pulse which sets the Input Buffer flag, IBFLG. Because the Output Buffer is empty, OBFLG is in a set state, (in this case this flag was set by the GOP of the WRITE command). With both IBFLG and OBFLG in a set state, gate A11-V2 (T11) is qualified and the M304 single-shot (B18-K1) produces the 1 μs pulse SET OBF, which performs the following:

   a. Transfers the character from the input buffer to the output buffer (at the trailing edge of the pulse).

   b. Causes the OBFLG to be reset, indicating that the output buffer is full.

   c. Causes the IBFLG to be reset indicating that the input buffer is empty.

   d. Produces SET REQ which results in a Write NPR request for a new character.

2. *Second and Subsequent Characters:* The first character is now held in the output buffer waiting for the Formatter to accept it. Step d above produces a new NPR cycle resulting in generation of END CYCLE AND DAT STRB which performs the same functions as described in Step 1 above with the following exception: DAT STRB loads the input buffer and sets the IBFLG. If the output buffer is still loaded with the previous character, OBFLG remains reset, thus inhibiting qualification of gate A11-V2. The following conditions are true at this time:

   a. The output buffer is still loaded with the previous character and OBFLG is still reset.

   b. The input buffer is now loaded with a new character and IBLFG is set. When the Formatter finally accepts the first character, it issues DA (DAT ACPT) back to the TCU. Signal DAT ACPT performs a number of functions in the TCU, but in the case of buffer control it sets OBFLG indicating that the output buffer is waiting for a new character. The change in level of OBFLG enables gate A11-V2 and causes the M304 (B18-K1) to again produce SET OBF, which performs the same tasks as described in Step 1, above. This sequence of events continues until the WCR overflows at which time the last character is written and EODAT is generated. See Paragraph 4.6.12 for details.

      If either NXMF or BGL are asserted during the WRITE operation, NPR requests are inhibited, EODAT is produced, and the ERR is set.

4.6.13 READ

This command is produced when the function RD FWD is issued by the program and GOP become asserted. The command is used internally in the TCU and is not transmitted directly to the MTT. When READ is asserted, the following functions are initiated:

1. Forward Motion
2. Read-Gap Generation
3. NPR Requests
4. Buffer Control.

When the READ command is issued, the read operation is carried out as described in the following paragraph. Refer to the read timing diagram, Figure 4-8. As the MTT starts in motion and the Read Head is just about to leave the gap and commence going over data characters, the buffer is in the following state:

1. The IBFLG flag is reset (empty).
2. The OBFLG flag is set (empty).

The first Read Clock Pulse (RD CLK) received from the MTT (indicating that the Read Head has just passed over the first character) causes the IBFLG to set and the input buffer to become loaded. Gate A11-V2 (Sheet T11) qualifies and causes the M304 one-shot multivibrator (B18-K1) to produce SET OBF. This pulse performs the following tasks:

1. Shifts the character from the input buffer to the output buffer.
2. Resets OBFLG, indicating that the output buffer is full.
3. Resets IBFLG, indicating that the input buffer is empty.

As OBFLG is reset, the M606 pulse generator in location A20-D2 (T11) produces a 50 ns pulse that generates SET REQ and then REQ BUS (if WCOF is not set). This causes a Read NPR request to be generated. A DMA cycle follows when NPG is asserted by the bus. At the trailing edge of NPG, DAT TO BUS is produced to strobe the data from the output buffer onto the Unibus (T15). END CYCLE is then produced and used to:

1. Clear the DMA Cycle
2. Set the OBFLG Flag (output buffer is empty)
3. Increment the WCR and BAR.

As the Read-Head goes over the next character, a new RD CLK pulse is produced and transmitted to the TCU in the manner described in the foregoing. This sequence continues until WCOF is set, at which time the last character should have been read. In instances where the value in the Word Count Register (WCR) and the record length are not the same, the error logic in the TCU will function as follows:

1. If the record length is greater than the value in the WCR, when WCOF is set, no more data will be taken into memory but the tape will continue moving forward until all surplus data characters have passed under the heads (but not input to memory). Finally, when EOB appears, a normal stop will take place in the gap.

2. If the record is shorter than the value of the WCR, RD CLK pulses will ease and therefore no further NPR requests will be generated. When EOB arrives, the TCU will cause the MTT to stop in the gap as normal, but the WCR will still be non-zero.

Steps 1 and 2 above are also described under RD CNT in Table 4-1, bit 09. If either NMF or BGL is asserted during the READ operation, NPR requests are inhibited, and the ERR bit is set.

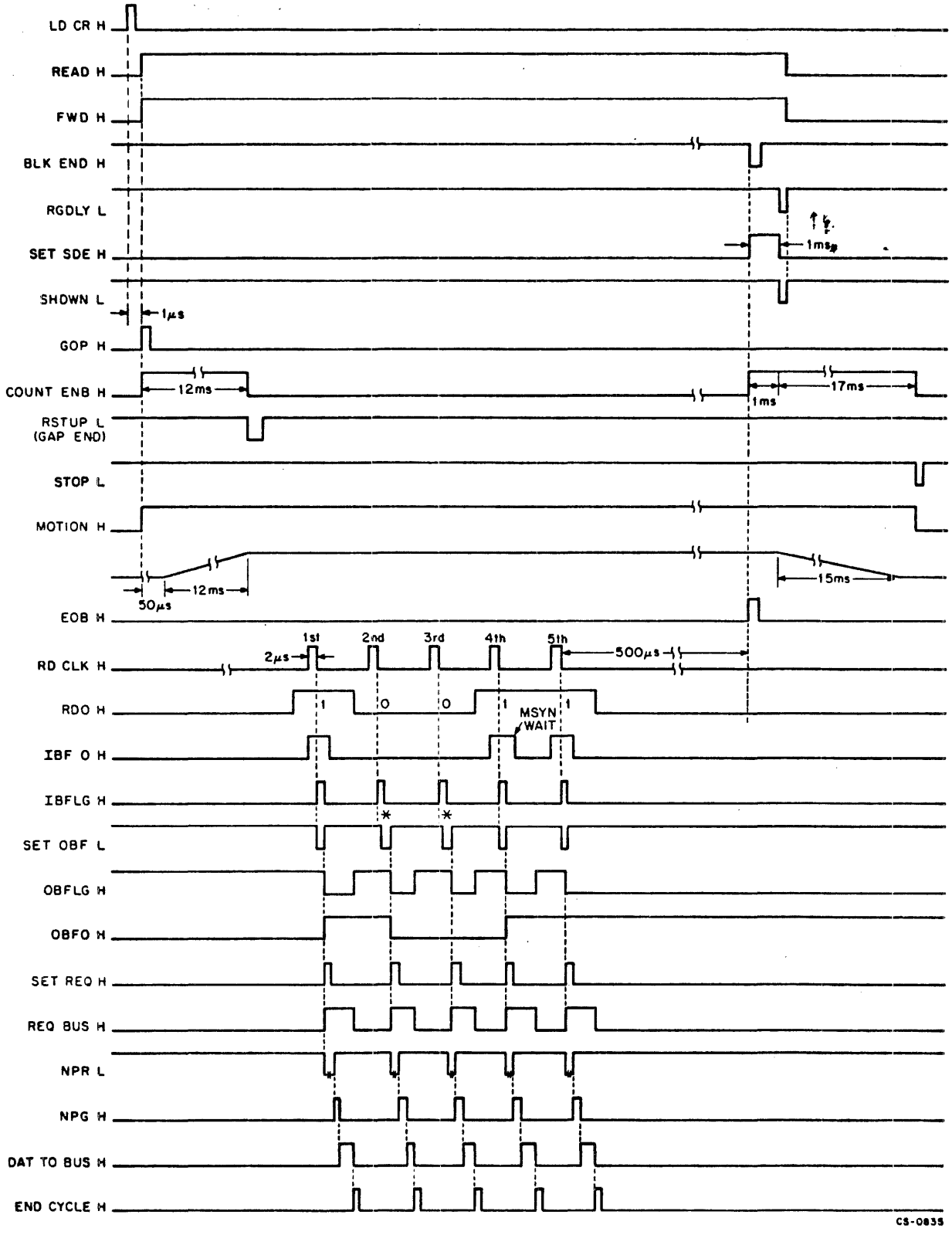


Figure 4-8 Read Timing

4.6.14 ERASE

This command is produced when the function ERS EN is issued by the program and GOP becomes asserted. The command is used internally in the TCU and is not transmitted directly to the MTT. When the ERASE command is issued the following functions are initiated: FWD EN, WSW EN, and WT ENB. The latter signal, WT ENB is inhibited from being issued to the Formatter in this instance. The parameters required for erasing tape are:

1. The write current should be flowing in the Write and Erase Heads (WSW is true)
2. WT ENB to the Formatter should be disabled.

When erasure is required, the length of tape to be erased is determined by loading a suitable number in the WCR and then incrementing WCR until it overflows. The WCR is incremented by means of a 6-stage, divide-by-32, Erase Counter (T10). When the ERASE command is issued, the Erase Counter increments the WCR at 800 μs intervals, producing a tape movement of 0.02 in. (at 25 ips, the tape travels 0.025 in. each millisecond). The length of erased section of tape is, therefore, the product of the number loaded in the WCR and 0.02. The Erase Counter is driven by 2DF clock. When the counter times out, it triggers a pair of one-shot multivibrators (C08-D2 and B18-M1) which produces INC WC. This pulse increments the WCR (T14) and the sequence is repeated until WCR overflows and WCOF is set, causing CLR ERS to be produced (T07). Signal CLR ERS performs the following:

1. Clears the ERASE command thus disabling the Erase Counter
2. Causes CLR CMD to be generated which clears FWD and WT ENB.

When stopping from an Erase operation, the MTT goes through the Write Shut-Down sequence. This is achieved by producing a pseudo BLK-END pulse from CLR ERS (T09). For a full description of Write Shut-Down, refer to Paragraph 4.5.2.

4.6.15 SP REV

This command is produced by the program and is used to cause tape motion in the reverse direction one block at a time.

No NPR requests are generated for SP REV and no data transaction to memory takes place. Data is reaching the buffer, however, and parity is being generated and checked.

4.7 TCU AND MTT TROUBLESHOOTING

The signals listed in Table 4-6 are provided to aid in troubleshooting between the TCU and MTT.

Table 4-6
TCU to MTT Signal Cross Reference

Controller to Drive		Function
Sel UNT 1 L	CS L	Command Select
RWND L	CRW L	Command Rewind
Local L	CL L	Command Local
FWD L	CF L	Command Forward
REV L	CR L	Command Reverse
FAST L	CH L	Command High Speed
WSWC L	WSW L	Set Write
WT ENB L	EN	Write Forward Enable
WPAMB	WPA	Write Preamble
WID	WID	Write ID Burst
(WRT·EOFC)	WTM	Write Tape Mark
EODAT L	EOD L	End of Data (Start Postamble)
WDAT0 L	WD0 L	Write Bit 0
WDAT1 L	WD1 L	Write Bit 1
WDAT2 L	WD2 L	Write Bit 2
WDAT3 L	WD3 L	Write Bit 3
WDAT4 L	WD4 L	Write Bit 4
WDAT5 L	WD5 L	Write Bit 5
WDAT6 L	WD6 L	Write Bit 6
WDAT7 L	WD7 L	Write Bit 7
WDATP L	WDP L	Write Parity Bit
Drive to Controller		**Function**
SL L	ONLNS H	Selected Drive ON-LINE
SR L	MTRDY H	Ready Status
SLP L	LDPS H	Load Point Status (BOT)
SRW L	RWDS H	Rewind Status
SFP L	FPTS H	File Protect Status
SET L	EOTS H	End of Tape Status
SD16 L	SD16 H	Density=1600 bpi (PE)
EOB L	EOB H	End of Block
TM L	EOFS H	Tape Mark Detected
IDBL	IDBS H	ID Burst Detected
MTE L	MTE H	Multiple Tracks in Error
STE L	STE H	Single Track Error
RDY L	FRDY H	Ready (Write Done)
2DF L	2DF H	2X Data Frequency (Clock)
SW L	WRTS H	Write Status
DA L	DAT ACPT H	Data Word Accepted
RC L	RD CLK H	Read Clock
RDP L	RDP H	Read Parity Bit
RD0–7 L	RD0–7 H	Read Bit 0 Through 7

4.8 LIST OF MNEMONICS

The following is a list of the mnemonic signal indicators and terms used in this manual.

Mnemonic	Definition
2DF	80 kHz clock from the formatter card of the MTT. This clock is equal to Twice Data Frequency (2DF).
ABORT	Clears FWD or REV motion flip-flops if the MTT did not respond to a legal command. Causes SR bit 08 to set. See Table 4-1, bit 08.
ADDR TO BUS	Produced by the M796 Master Control Module. Gates the address of the slave onto BUS A <17:00>.
ANY WT	Any Write. An OR function of WRT, WEOF, WIDB EN, or ERS EN.
BA CARRY OUT	Bus Address Carry: produced when the first four bits of the BA counter overflow.
BACK	This flip-flop sets when the EOTS status is asserted while the tape is moving forward at high speed and is reset when the EOT is reversed back to the photosense head assembly.
BAOVFL	Bus Address Overflow occurs when the contents of the BAR counter become all ones.
BA TO BUS	Gating strobe gates BAR to the Unibus by program.
BAR	Bus Address Register.
BG OUT	Bus Grant Line outlet from the TCU.
BG IN	Bus Grant Line into the TCU.
BG 4, 5, 6, 7 IN	Bus Grant level x in.
BG 4, 5, 6, 7 OUT	Bus Grant level x out.
BLK END	BLOCK END. Produced from EOB during a WRITE, WEOF, WIDB, or READ. Appears 20 character times after the last character has been read or check-read.
B OUT LO	OUT LO gates with SSYN INH to limit the width of the pulse. Gates the SELECT lines to the TCU.
B SSYN	BUS SSYN inverted for use in the TCU.
BUS A00 through BUS A17	Bus Address lines A00 through A17
BUS AC LO	This pulse is asserted when ac power is failing. When this occurs, power is available for 2 ms at full load.

Mnemonic	Definition
BUS B BSY	Unibus Busy. Asserted when the device becomes bus master.
BUS BR 4, 5, 6, and 7	Bus Request levels 4 through 7.
BUS C0, BUS C1	Bus Control Lines. Coded by the master device to control the slave in one of four possible data transfer operations. See the Unibus Interface Manual.
BUS D00 through BUS D15	Sixteen data lines used to transfer data between master and slave.
BUS DC LO	Asserted when ac or dc power is failing. When this occurs, a few more milliseconds of full load dc power are available.
BUS INIT	Used to clear or initialize the CPU and peripheral devices on the bus. Asserted when (1) the START key on the console is depressed, (2) when a RESET instruction is executed, and (3) when power fail sequence occurs.
BUS INTR	This signal is asserted by the bus master to initiate a program interrupt in the CPU.
BUS MSYN	Master Synchronization signal, used by the master to indicate to the slave that address and control information is present.
BUS NPG OUT, BUS NPG IN	Non-Processor Grant outlet and inlet lines from and to the TCU, respectively.
BUS NPR	Non-Processor Request. A bus request signal from a peripheral device to the CPU. Asserted when a DMA cycle is required.
BUS SACK	Selection Acknowledge. Asserted by a bus requesting device when it has received a bus grant.
BUS SSYN	Slave Synchronization signal. The slave's response to the master (MSYN).
BUSY	The TCU Busy status. Asserted when a legal command is being executed. Reset when the gap is completed.
C BUS 00 through C BUS 15	Common data bits 00 through 15. These bits are inverted through a bus driver to produce BUS D00 through BUS D15.
CF	Forward command; an MTT signal. Connects with FWD in the TCU.
CH	High Speed command; an MTT signal. Connects with FAST in the TCU.
CL	Off-Line command; an MTT signal. Connects with LOCAL in the TCU.

Mnemonic	Definition
CLR FLG	Clear Flag. Sets the OBFLG under the following conditions: GOP or Reset END CYCLE when Reading DAT ACPT when Writing
CLR BACK	Clears the BACK flip-flop when the EOT has been repositioned under the photosense head assembly after a reverse from the High Speed Forward overshoot.
CLR CMD	Clear command. Clears MTT commands just before the gap shut-down sequence starts.
CLR ERS	Clear Erase. Clears the ERASE command when the WCR overflows.
CLR FF	Clear flip-flop. Clears WID and EOFC when FRDY is negated, i.e., when the command is accepted by the Formatter.
CLR GO	Clear GO. Clears the GOBIT flip-flop.
CLR MF	Clear Motion Forward. Clears MOTION flip-flop.
CLR NEX	Clear Non-Existent Memory. Clears the NXM flip-flop in M796 Master Control Module.
CLR OFL	Clear Off Line. Clears the LOCAL flip-flop.
CLR SDE	Clear Shut Down Enable. Used to clear SHDWN ENB and to produce CLR TC.
CLR TC	Clear Time Count. Momentarily clears the 2-stage Gap Counter, causing it to start a new count cycle.
COUNT ENB	Count Enable. When set permits the 2-stage Gap Counter to start a count cycle. When reset, stops the counter.
CR	Reverse command, an MTT signal. Links with REV in the TCU.
CR TO BUS	Control Register TO BUS. Strobes the contents of CR to the Unibus with Address 764000.
CRW	Rewind command; an MTT signal. Links with RWND in the TCU.
CS	Select Unit command; an MTT signal. Links with SEL UNIT 1 in the TCU.
CU RDY	Control Unit Ready. Set when the TCU is ready to receive a new command. Reset when GOP is issued, PWR CLR is set or when the MTT goes off-line.

Mnemonic	Definition
DA	Data Accepted; a Formatter signal. Links with DAT ACPT in the TCU. Asserted when the Formatter has accepted the data from the TCU buffer.
DAT ACPT	Data Accepted; a TCU signal. Derived from DA.
DATA TO BUS	Strobes the Read data from the output buffer to the Unibus. This signal is produced by the M796 Master Control Module during a DATO cycle.
DAT WAIT	A delay produced during a DATI cycle before DAT STRB is asserted.
DAT STRB	DATA STROBE. Strobes data from the bus to the buffer during a DATI cycle. Produced by the M796 Master Control Module.
DIV00 through DIV05	Divide stages of the first stage of the Gap Counter.
D00 through D15	Data lines after inversion through bus receivers in the TCU.
EC0	Erase Counter stage zero (MSB stage).
END COUNT	One of the pulses that clears COUNT ENB.
END CYCLE	Pulse produced by the M796 Master Control and used to terminate the DMA cycle.
EOB	End-Of-Block; an MTT signal. Produced during a WRITE, WEOF, WIDB, or READ. Appears 20 bit times after the last character has been read or check read.
EOD	End-of-Data; a Formatter signal. When received by the Formatter, causes it to write the Postamble.
EODAT	End-of-Data: produced by the TCU when the last character is issued to the Formatter and causes latter to write the Postamble. Links with EOD.
EOFC	End-of-File command. Produced by the TCU and links with WTM in the Formatter causing it to write TAPE MARK.
EOFF	End-of-File Flag. Status Register bit 04. Sets when Tape Mark is being written or read.
EOFS	End-of-File Status. Links with TM in the MTT. Asserted when Tape Mark is being written or read.
EOP	End-of-Operation Pulse. Produced when the tape stops in the gap on the completion of a legal command or on the completion of rewind.
EOTF	End-of-Tape Flag. Status Register bit 07. Set when EOT marker is detected.

Mnemonic	Definition
EOTS	End-of-Tape Status. Links with SET in the MTT. Set when the tape is at EOT marker.
EOXFER	End-of-Transfer. Pulse produced when the last DAT ACPT is received from the Formatter. Used to clear EO DAT.
ERASE	Erase command.
ERR	ERROR. Bit 15 of the Control Register. Sets when one of a group of errors occurs. See Table 3-1, bit 15.
ERS EN	ERASE ENABLE. A function issued by the program. Enables the ERASE command to be set at GOP time.
FAST	FAST FORWARD command. When issued, the tape moves forward at 160 ips to the EOT.
FAST FWD	FAST FORWARD function. Issued by the program. Enables the FAST command to be set at GOP time.
FNB00 through FNB03	FUNCTION BITS 00, 01, 02, and 03. The combination of these bits determines the function being issued by the program.
FPTS	File Protect Status. This status is true if the Write Enable Ring is absent.
FRDY	Formatter Ready. When true, indicates that the Formatter is ready to accept a command. When false, the Formatter is busy.
FRST WREQ	First Write Request. Generated 100 μs after the WPAMB command is issued.
FWD	FORWARD command. When issued, the tape moves forward at standard speed.
FWD EN	FORWARD ENABLE. A function issued by the program. Enables the FWD command to be set at GOP time.
FWD + REV	Forward or Reverse. This signal is asserted when either FWD or REV is asserted.
FWEN	Formatter Write Enable (EN). This is a Formatter signal. Must be asserted externally when a Write operation is required. Disabled when erasing. Links with WT EN in the TCU.
GAP END	Produced at completion of gap during start-up.
GO BIT	Bit 00 of the Control Register. Set every time a command is issued.
GOP	GO PULSE. Derived from GO BIT with 1 μs delay. Clocks the legal commands into the Command Register.

Mnemonic	Definition
GOP + RESET	GOP or RESET. Signal used for clearing the TCU.
GOPF	GO PULSE flip-flop. Used to generate GOP.
IBF 0 through 7	Input Buffer Bits 0 through 7.
IBFLG	Input Buffer Flag. Set when input stage of buffer is FULL, reset when input buffer is EMPTY.
IBF P	Input Buffer Parity bit (bit 9)
IDB	Identification Burst; an MTT signal. Links with IDBS in the TCU.
IDB BE	EOB produced at end of writing or reading of IDB.
IDBF	Identification Burst Flag in the Status Register. Set at EOB time when the IDB status (IDBS) is true.
IDBS	Identification Burst Status; a TCU signal. Links with IDB in the MTT.
ILC00 ILC03 ILC05 ILC06 ILC11 ILC12 ILC14	Illegal functions. If issued by the program, CR bits 14 and 15 are set and an interrupt is produced. GOP is not generated.
ILCMD	Bit 14 of the Control Register. Set when an illegal command is issued. See Table 3-1, bits 01 through 04 for illegal commands.
ILLEGAL	A pulse produced when an illegal command is issued.
ILP	A 100 ns pulse produced from the leading edge of ILLEGAL.
IN	A strobe produced by the M105 Address Module. Used for gating onto the bus in the program mode.
INC WC	Increment Word Count. 50 ns pulse (average) used for incrementing WCR and BAR.
INHBT	INHIBIT. Bit 00 of Status Register. Sets at end of operation. Must be cleared by program before new command is executed. Inhibits GOP if not cleared.
INT ENB	Interrupt Enable. CR bit 06. Must be set to allow interrupts. This bit is not cleared when PWR CLR is issued.

Mnemonic	Definition
INTF	Interrupt Flag. Sets when a hardware interrupt condition is produced.
INTR DONE	A pulse produced by the M7821 interrupt module when the interupt is serviced on BR level 4.
LD BA	Load Bus Address. Address 764006, used to load the BAR from the bus.
LD CR	Load Control Register. Address 764000, used to load the Control Register from the bus.
LDP GAP	LOAD POINT GAP. This pulse is produced when the 2.4 in. gap following the IDB is completed.
LDPS	Load Point Status. Asserted while the tape is stationary at load point. Links with SLP in the MTT.
LD SR	Load Status Register. Address 764002, used to load the Status Register from the bus.
LD WC	Load Word Count Register. Address 764004, used to load the WCR from the bus.
LOCAL	This command is issued by the TCU and causes the MTT to go offline. This command links with CL in the MTT.
LONG	Indicates that the record being read now is longer than the value in the WCR. Causes RD CNT flag to be set (an error condition).
MASR A	MASTER A. Generated by the M7821 interrupt module when the TCU becomes bus master during NPR transactions.
MASR B	MASTER B. Generated by the M7821 interrupt module when the TCU becomes bus master during an interrupt routine.
MOTION	Motion flip-flop. Set when FWD or REV commands are asserted. Remains set until all motion ceases including ramp-down.
MSYN WAIT	Delay before MSYN is asserted. Generated by M796 Master Control Module.
MTE	Multiple Track Error; an MTT signal. Causes MTEF to be set. Also known as hard or permanent error.
MTEF	Multiple Track Error Flag. Set at EOB time when MTE is asserted.
MTRDY	Magnetic Tape Ready. Links with SR in the MTT. Set when the MTT is ON-LINE and not REWINDING.
MTT	Magnetic Tape Transport.

Mnemonic	Definition
NXM	Non-Existent Memory flip-flop (in the M796 Master Control Module). Set when the master issues MSYN and the slave does not respond with SSYN within 20 μs.
NXMF	Non-Existent Memory Flag. SR bit 06. Set when NXM is asserted. When set, causes NXM to be cleared.
OBFLG	Output Buffer Flag. Set when output buffer is EMPTY, reset when output buffer is FULL.
OFLIN	OFF LINE command. Causes the MTT to go off-line.
OFLNP	OFF LINE PULSE. Produced when the ONLNS is negated.
ONLNS	ON-LINE STATUS. Received from the MTT where it is referred to as SL.
OUT HI, OUT LO	Byte Gating Control signals generated in the M105 Address Module.
PCLR	Power Clear Pulse, 20 ms pulse generated when PWR CLR is set. Causes CURDY to be reset.
PCOFF	Power Clear Off. 50 ns pulse produced after 900 ms delay, used to clear PWR CLR and to produce SET RDY.
PWR CLR	POWER CLEAR. Bit 11 of the Control Register. When set by the program, produces a 20 ms initialize pulse that clears the TCU (except INT ENB). Clears itself after a 900 ms delay and sets CURDY.
RC	READ CLOCK. A 2 μs MTT pulse. Indicates that a character has been read and is present and settled on the Read Data Lines of the MTT.
RD 0 through RD 7	Read Data Lines of the MTT. These lines are settled when Read Clock (RC) pulse is issued and remain settled until 1 μs before the next RC.
RD	Read Block End. The EOB pulse produced during a READ operation.
RD CLK	Read Clock. A TCU signal derived from RC.
RD CNT	READ COUNT. Bit 09 of the SR. Set when the length of the record being read is longer or shorter than the Word Count.
RD FWD	Read Forward function. Issued by the program when a READ operation is required.
RD P	Read Data Line 8 or Parity. An MTT signal. See RD 0 through RD 7.
READ	Read Command in the TCU. Produced from RD FWD at GOP time.

Mnemonic	Definition
READY	A Formatter status. Set when the Formatter can accept a command. Links with FRDY in the TCU.
REQ BUS	Request Bus flip-flop in the M796 Master Control Module. Set when an NPR has been made.
RESET	This is an OR of BUS INIT or PWR CLR. Clears the TCU.
REV	REVERSE command in the TCU. Causes the MTT to move in the reverse direction. Links with CR in the MTT.
REV EN	Reverse Enable function. When issued by the program causes REV to be produced.
RDGLY	Read Gap Delay. A pulse produced at the end of the Read Shut-Down delay (of 1 ms).
RPEF	Read Parity Error Flag. Bit 15 of SR. Sets when the first Read or Read-after-Write parity error appears in a block.
RPODD	Read Parity Odd. Asserted when the Read or Read-after-Write character parity is odd.
RSTUP	Read Start-Up. This pulse is produced at the completion of Read Start-Up portion of the IBG.
RWD EN	Rewind Enable function. When issued by the program causes RWND command to be produced.
RWDS	Rewind Status. Bit 01 of SR. Asserted while MTT is rewinding. Links with SRW in the MTT.
RWND	REWIND command issued by the TCU. Causes the MTT to rewind. Links with CRW in the MTT.
S BIT 8 and 9	Select Bits 08 and 09 in the Control Register. Coded to select one of four transport.
SD 16	Select Density 1600 bpi. Assertion signifies that the selected MTT is on-line and can operate on 1600 bpi phase encoded. This is an MTT signal.
SELECT 0, 2, 4, and 6	Select Address lines from the M105 module.
SELT 0, 1, 2, and 3	Select MTT units 0, 1, 2, or 3. These TCU signals link with CS0, CS1, CS2, CS3 in the MTT, respectively.
SEL UNT 1	The OR-function of SELT 0, 1, 2, and 3. Any combination of SBIT8 and SBIT9 will select the same MTT (optional signal).

Mnemonic	Definition
SET	End-of-Tape Status. An MTT signal. Links with EOTS in the TCU.
SET BACK	A 50 ns pulse produced when EOTS is asserted when moving at high speed forward. Causes BACK flip-flop to be set.
SET GO	A 1 μs pulse produced when the GO BIT is set. Used to set the GOPF flip-flop and hence produce GOP.
SET OBF	SET OUTPUT BUFFER FLAG. A 1 μs pulse produced as a result of a transition in the states of IBFLG and OBFLG. Resets both IBFLG and OBLFG.
SET RDY	SET READY. Produced at EOP, or when ONLNS is asserted, or PWR CLR flip-flop is reset. Used to set CU RDY.
SET REQ	SET REQUEST. Causes the BUS REQ flip-flop to be set when a Write or Read NPR is required.
SET REV	SET REVERSE. Causes the REV command to be set at the end of 900 ms delay following a stop from high speed forward.
SET SDE	SET SHUT-DOWN ENABLE. Causes the SHDWN ENB flip-flop to become set during the shut-down stage of the IBG.
SFP	File Protect Status. This is an MTT signal. Links with FPTS in the TCU.
SHDWN	SHUT-DOWN. A TCU pulse produced at the end of WRITE- or READ Shut-Down delay just before ramp-down begins.
SHDWN ENB	SHUT-DOWN ENABLE. This flip-flop enables WRITE- and READ Shut-Down delays to be produced, WGDLY, and RGDLY.
SHORT	Indicates that the record being read now is shorter than the number of words in the WCR. Causes RD CNT flag to be set (an error condition).
SL	ON-LINE STATUS. This is an MTT signal linking with ONLNS in the TCU. Asserted as long as the MTT is ON-LINE.
SLP	LOAD POINT STATUS. This is an MTT signal linking with LDPS in the TCU. Asserted while the MTT is at the load point.
SP FWD	SPACE FORWARD function. Causes the tape to move forward one block at a time (optional).
SP REV	Space Reverse function. Issued by the program to the TCU. Causes tape motion to reverse direction one block at a time.

Mnemonic	Definition
SR	READY STATUS. This is an MTT signal linking with MTRDY in the TCU. Asserted as long as the MTT is selected, on-line and not rewinding.
SR TO BUS	Status Register To Bus. Loads the contents of the SR to the bus with address 764002.
SRW	REWIND STATUS. This is an MTT signal linking with RWDS in the TCU. Asserted while the MTT is rewinding.
STE	Single Track Error. This is an MTT signal. Used to set the STEF flag at EOB time.
STEF	Single Track Error Flag. Set at EOB time if STE is asserted (an error condition).
STOP	The pulse appears at the end of the shut-down stage in a WRITE or READ operation when tape motion has ceased.
SW	WRITE STATUS. This is a Formatter signal linking with WRTS in the TCU. Asserted 20 μs after issuing the WSWC command in the TCU. Clears WSWC.
TC0 through TC7	Time Count stages 0 through 7 in the Gap Counter. The binary weight value of each stage represents the number of half milliseconds of delay.
TCU	Tape Control Unit, TR79-FA.
TM	Tape Mark Status. This is an MTT signal linking with EOFS in the TCU. Asserted while the MTT is reading, or check-reading a Tape Mark. Causes SR bit 03 to set at EOB time.
TMOUT	TIME OUT. SR bit 08. Set when an ABORT condition occurs.
WCOF	Word Count Overflow Flag. Set when WCR overflows.
WCOVFL	Word Count Overflow pulse from the M795 W/C module.
WCR	Word Count Register.
WC TO BUS	Word Count To Bus. Loads the contents of the WCR to the bus with address 764004.
WD0 through WD7	Write Data lines from the TCU to the MTT. Link with WDAT0 through WDAT7 in the TCU.
WDP	Write Data line 8 or Parity to the MTT. Links with WDATP in the TCU.
WDAT0 through WDAT7	Write Data 0 through 7. Write data bits from the output buffer for writing on tape. Link with WD0 through WD7 in the MTT.

Mnemonic	Definition
WDATP	Write Data 8 or Parity. Write data bit from the output buffer. Links with WDP in the MTT.
WEOF	Write End-of-File funetion. Issued by the program when an EOFC (WTM) command is required.
WGDLY	Write Gap Delay. A pulse produced at the end of Write Shut-Down just before ramp-down starts.
WID	Write Identification Burst command. Set at the trailing edge of the LDPS status if WIDB EN was selected by the program.
WIDB EN	Write Identification Burst function. Issued by the program when the WID command is required.
WPA	Write Preamble. This is a Formatter command linking with WPAMB in the TCU. Causes the Formatter to write the Preamble.
WPAMB	Write Preamble. This command is produced by the TCU hardware when the WRITE command is issued causing the Preamble to be written by the Formatter before issuing write data from the TCU. Links with WPA in the Formatter.
WPEF	Write Parity Error Flag. Bit 14 of SR. Sets when the first write parity error appears in a block.
WPODD	Write Parity Odd. Asserted when the write character parity is odd.
WRITE	Write command in the TCU. Produced from WRT at GOP time.
WRT	Write function. Issued by the program when a WRITE operation is required.
WRTS	Write Status. Links with SW in the Formatter. Asserts 20 μs after issuing the WSWC command in the TCU. Clears WSWC.
WSTRB	Write Strobe. Produced from an AND condition of Write parameters and used to gate the WDAT lines to the cable leading to the MTT.
WSTUP	Write Start-Up. This pulse is produced at the completion of the Write Start-Up portion of the IBG.
WSW	Set Write Command. This is an MTT signal, linking with WSWC in the TCU. Assertion of this signal enables the setting of the MTT's write condition. Turns the current on in the Write and Erase heads.
WSWC	Set Write Command. Links with WSW in the MTT. Required for writing and erasing. This command is asserted at GOP time when the program selects any write (ANY WT) operation, including erase.

Mnemonic	Definition
WSW EN	Set Write Enable function. Produced when the program selects any write function, e.g., WRT, WEOF, WIDB EN, ERS EN.
WT ENB	Write Enable. This is a TCU command produced at GOP time when ANY WT is asserted. Required for all Write commands except erase. Links with EN in the Formatter.
XBA16 and XBA17	Extended bus address bits 16 and 17. Allow addressing of memory banks above 32K. See Table 3-1.

CHAPTER 5
MAINTENANCE

5.1 SPECIAL TEST EQUIPMENT

The following special equipment is required for performing maintenance:

1. Dual beam oscilloscope
2. Multimeter
3. Fresh reel of tape
4. Special fluid for developing written tape
5. Isopropyl alcohol (91% pure)
6. Cotton swabs.

5.2 PREVENTIVE MAINTENANCE

All general preventive maintenance procedures specified for the PDP-11 processor also apply to the TR79-FA. The proper sequence for powering up this system is to turn on the processor first and then the TR79-FA. The reverse of this procedure is followed when powering down. The transport maintenance procedures as specified in Section 3 of the HP Operating and Service Manual should be observed.

5.2.1 TR79-FA Magtape Controller Monthly Field Service Preventive Maintenance

1. Check that the fan in the H720E power supply is not obstructed and that it turns freely when power is applied.

5.2.2 TR79-FA Magtape Controller Quarterly Field Service Preventive Maintenance

1. Review the ECO status of the TR79-FA Magtape Controller, and plan the installation of appropriate F-coded ECOs.

2. With power OFF, ensure that all of the mounting screws securing the TR79-FA backplane are tight.

NOTE
Power should remain OFF for steps 3 through 7, below.

3. Ensure that each module is securely seated in its connector.

4. Visually inspect the backplane for broken wires, worn insulation, and bent pins. Repair or replace any defective items.

5. Inspect all wiring and cables for cuts, breaks, frays, deterioration, kinks, strain, and mechanical security. Repair or replace defective wiring or cables.

6. Inspect all connectors for mechanical security and defects. Repair or replace connectors as required.

7. Check that all crimp lugs are secure, and that all lugs are properly inserted in their mating connectors.

8. Turn power ON; check the +5 V device logic voltage.

Reference Point = A5A2
Nominal Value = +5 Vdc
Max Peak-to-Peak Ripple = 0.2 V

Adjust R38 in the associated H720E power supply. If the power supply cannot be adjusted to meet specifications, repair or replace it.

9. Load the TR79 Subsystem Diagnostic MAINDEC-11-DZTRA with ~~all switches set to 0~~. 3 w lo

   a. Specify and run tests 1, 2, and 3 with tape loaded and drive on-line.

   b. If any errors are observed, correct the problem and rerun the failing test.

5.2.3 TR79-FA Magtape Controller Annual Field Service Preventive Maintenance

1. While running the diagnostic specified in step 9 of the quarterly PM procedure, check the one-shot outputs shown in the table below. Compare the observed value of each with that shown in the following table to discover any major discrepancies. Repair or replace defective circuitry.

Location/Module	Input	Output	Time
C6	H2	F2	20 ms
M302	M2	T2	900 ms
C10	H2	F2	200 μs
M302	M2	T2	40 μs
B18	E1	J1	1 μs
M304	R1	P1	100 μs
	D1	H1	1 μs
	S1	M1	1 μs
A16	H2	F2	17 ms
M302	M2	T2	18 μs
D13	H2	F2	75 ms
M302			
A22	M2	T2	900 ms
M302	H2	F2	100 μs
A25	H2	T2	1.5 sec
M302			

NOTE

The drawings in this PM procedure are reprinted with the permission of Hewlett-Packard Company.

5.2.4 HP7970E Magtape Drive Quarterly Field Service Preventive Maintenance

1. Check all indicator lamps (LOAD, RESET, REWIND, ON LINE, EOT/BOT SENSOR, and WRITE ENABLE); replace any that are burned out.

2. Inspect the tape path, including the areas listed below, for wear, scratches, and mechanical security. Repair or replace defective items as required.

   - Roller guides
   - Tape guides
   - Capstan
   - Write lock assembly

3. Using a wipe moistened with trichlorethylene, clean the capstan wheel.

4. Verify that the reel hold-down assembly correctly secures the reel to the hub. If not, adjust according to the following procedure:

   a. Release the locking lever (item 1 in Figure 5-1).

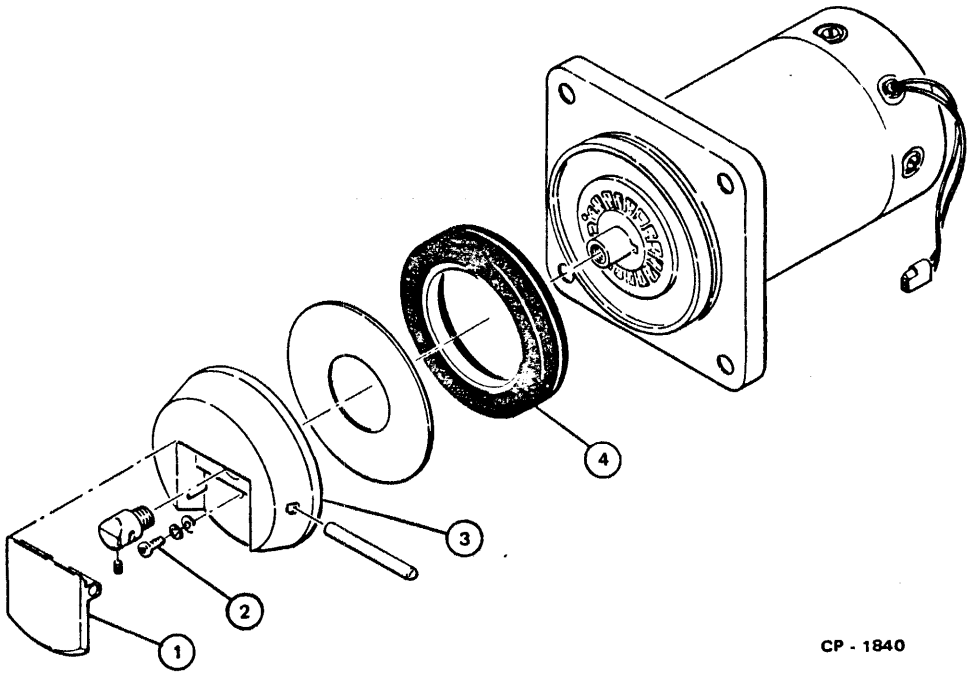


Figure 5-1 Reel Motor Assembly

   b. Loosen the lock screw (item 2).

   c. Tighten the reel knob (item 3) one-eighth turn.

   d. Tighten the lock screw, and check for slippage.

e. Repeat steps a through d until the tape reel mounts smoothly and without slipping.

NOTE
As the rubber ring (item 4) ages, adjustment may become impossible; in that case, the ring should be replaced.

5. Clean (using a clean, dry cloth) or vacuum the drive cabinet and logic racks.

6. Ensure that all logic modules and connectors are mounted securely.

7. Turn power ON; check the +5 Vdc logic voltage at the power regulator board.

   Reference Point = +5 V test point on regulator
   Nominal Value = +5 Vdc ± 0.05 V

   Using a precision DVM, adjust R4 on the power regulator board to obtain the correct voltage.

8. Check +12 Vdc and -12 Vdc supplies.

   Reference Point = +12 Vdc and -12 Vdc test points, respectively
   Nominal Value = +12 Vdc ± 0.36 V and -12 Vdc ± 0.36 V

   +5 V is used as a reference voltage. No adjustment is possible. If voltage values are significantly out of tolerance, repair or replace the regulator.

NOTE
If an annual PM is scheduled, proceed to step 1 of that PM; if not, continue with step 9, below.

9. Check tape positioning according to the following procedure:

   a. Using the high-speed forward (+160) switch on the capstan servo amplifier, space the tape forward several feet.

   b. Initiate a rewind function.

   c. Observe that the tension arms position themselves approximately in the middle of their travel, and that no limit switches are contacted during start-up or shut-down.

   d. Ensure that the tape stops and spaces forward to the load point when the rewind is complete.

   e. If step c discloses positioning problems, adjust as follows:

      (1) Mount a scratch tape on the drive.

      (2) Rotate R106 (upper potentiometer on the reel servo control board, 62173) fully counterclockwise.

      (3) Initiate forward motion, using the FWD switch on the capstan servo board (62172).

      (4) Adjust R106 clockwise to allow the upper servo control arm to deflect over the top of the first upper drilled alignment mark while tape is moving.

(5) Reset FWD switch in step 3, above, and set REV switch on same module.

(6) Visually verify that the tension arm deflects the same distance in the opposite direction. If not, adjust asymmetry (due to nonlinearity of the tension arm transducer) by turning the tension arm mask so that deflection is symmetrical. R106 should be readjusted for proper deflecton.

NOTE

The tension arm may not be centered when there is no tape motion; this is not relevant, as long as the swing is symmetrical.

(7) Repeat the above procedure for the lower tension arm; using R104 for the adjustment.

NOTE

If a 2-year PM is scheduled for this device, proceed to step 1 of that PM at this time; if not, continue with step 1 of the semiannual PM procedure for this device.

5.2.5 HP7970E Magtape Drive Semiannual Field Service Preventive Maintenance

1. Check the capstan offset current by either of the methods described below. (An incorrect setting will result in the capstan motor creeping when tape motion is supposed to be stopped.)

Method A

a. Connect a precision voltmeter across the large 3-ohm resistors (R21, R22) located on the capstan servo heat sink (62172).

CAUTION

Do not connect the common side of the resistors to ground, as this will cause damage to the tachometer; the meter should have its ground isolated.

b. With a tape loaded and stopped, measure the voltage across the resistors. (The voltage should be 0 V ± 0.05 V.)

Method B

a. Scope the preamp test point on the capstan servo board (62172).

b. With a tape loaded and stopped, check the voltage at the test point. (The voltage should be 0 V ± 0.7 V.)

If adjustment is necessary, use the OFFSET (O/S) potentiometer on the capstan servo board.

2. Check the capstan servo drive speed adjustment before performing capstan servo ramp time, read preamp gain, and write skew delay adjustments.

NOTE

Because the required test equipment (frequency meter, speed tape, etc.) is not generally available to Field Service personnel, this portion of the semiannual PM procedure should be scheduled in conjunction with a representative of Hewlett Packard.

3. Check the capstan servo ramp time according to the following procedure:

NOTE
This procedure requires that the control and status tester module (13191) be installed.

a. Load a scratch tape on the drive.

b. Connect an oscilloscope to the FWD/REV test point on the capstan servo board (62171); sync on the forward drive command test point (TP9) on the control and status module (62062).

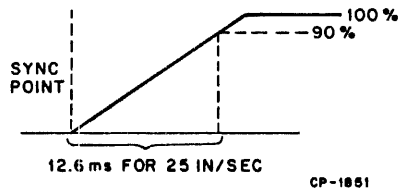
c. Set the control and status test board to provide alternate Forward/Stop commands:

(1) Program mode

(2) Forward command (CF)

(3) Maximum rep rate (PCF control fully counterclockwise)

d. Observe the waveform, and compare it with the following:



In this figure, 90% of the waveform should be set at 12.6 ms for a drive tape speed of 25 in./sec.

e. Adjust the ramp potentiometer on the capstan servo board to obtain the correct timing.

f. Verify the setting according to the following procedure:

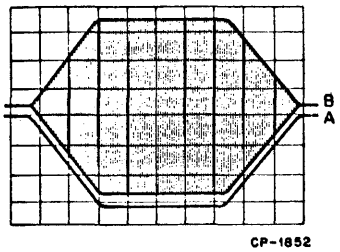
(1) Connect the Channel A probe of the oscilloscope to the tachometer output on the capstan servo board; connect the Channel B probe to any preamp output test point on the preamp board (62034).

(2) Mount a tape that has previously been recorded with all 1s.

(3) Trigger the oscilloscope on a forward drive command, and use the control and status test module to produce alternating Forward/Stop commands:

Program mode
Forward command (CF)
Maximum rep rate (PCF control fully counterclockwise)

(4) When reading the all-1s tape, the oscilloscope should display a waveform like the one in the following figure.



Channel B = Preamp Output 0.1 V/cm
Channel A = Tachometer Output 0.2 V/cm
5 ms/cm

Tachometer and Data Envelope

4. Check the read preamp gain according to the following procedure:

   a. Install the control and status test board (13191) and write formatter test board (13196).

   b. Clean the read/write head.

   c. Load a scratch tape.

   d. Connect the oscilloscope to the DIFF test point on the parity channel of the preamp module (62034).

   e. Perform a continuous write of alternating 1s, using the two test boards set up as follows:

      (1) Control and status test board

CH	OFF
WSW	ON
CR	OFF
CF	ON
PROG/MAN	MAN
CRW/OFF/SET CRW	SET CRW

      (2) Write Formatter test board

DATA SELECT	1600 FRPI
END OF BLOCK	OFF
WRITE	DATA BLOCKS (This should be the last switch set.)

   f. Measure the average peak-to-peak amplitude of the signal. If the signal is not within the specified range (4.5 V ± 0.3 V), adjust the associated gain potentiometer on the preamp module (62034) to obtain a peak-to-peak amplitude of 4.5 V ± 0.1 V.

   g. Repeat this procedure for each of the remaining eight channels.

5. Check the write skew delay according to the following procedure:

   a. Install the control and status tester (13191) and write formatter tester (13196).

   b. Load master skew tape.

c. Set the control and status tester to perform a read function.

CF	ON
PROG/MAN	MAN
CR	OFF
WSW	OFF
CH	OFF
CRW/OFF/SET CRW	OFF

d. Connect Channel A of the oscilloscope to DAT test point on the read decoder module (62041) of the reference track (track 5, Channel 2).

e. Set the oscilloscope controls to ALT mode, 5 μs sweep, and connect Channel B to DAT test point of the other eight read decoder modules.

f. Observe and record the time displacement of the positive-going edge of each track with respect to the reference track. Displacements of more than 12 μs (at 25 in./sec) from the reference track may be caused by head wear or electronic failure of the preamp or decoder. No adjustment is possible; repair or replace defective items.

g. Remove the skew tape, and load a blank reel of scratch tape.

h. Initiate a write operation, using the test modules set as follows:

(1) Control and status tester

CH	OFF
WSW	ON
CR	OFF
CF	ON
PROG/MAN	MAN
CRW/OFF/SET CRW	SET CRW

(2) Write formatter tester

DATA SELECT	1600 FRPI
END OF BLOCK	OFF
WRITE	DATA BLOCK (This should be the last switch set.)

i. Measure the skew delay at the DAT test point of each decoder module and compare the time of each with the reference track. If all tracks are within 50 ms of the reference track, no adjustment is necessary. If not, set the write skew according to the following procedure:

(1) Set all of the skew delay variable resistors (the exposed resistors on the write data modules 62049 and 62050) for minimum delay (fully counterclockwise).

(2) Adjust the delay resistor for Channel 2 clockwise to ensure that the trailing edge of that channel will occur slightly later than the trailing edge of the remaining channels.

(3) Adjust each delay resistor for no delay with respect to the reference channel.

6. Replace the load point bulb (part no. 29-10204); refer to Figure 5-2.

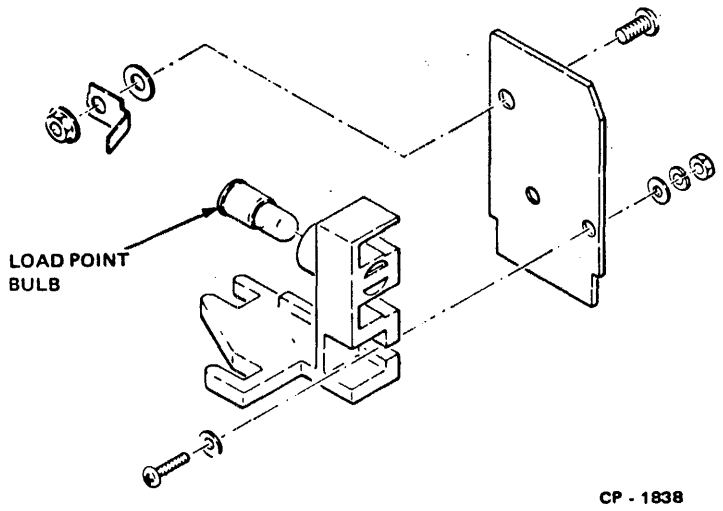


Figure 5-2 Load Point Bulb Assembly

5.2.6 HP7970E Magtape Drive Annual Field Service Preventive Maintenance

1. Replace both tension arm sensors; refer to Figure 5-3.

NOTE
Return to step 9 of the quarterly PM procedures at this time.

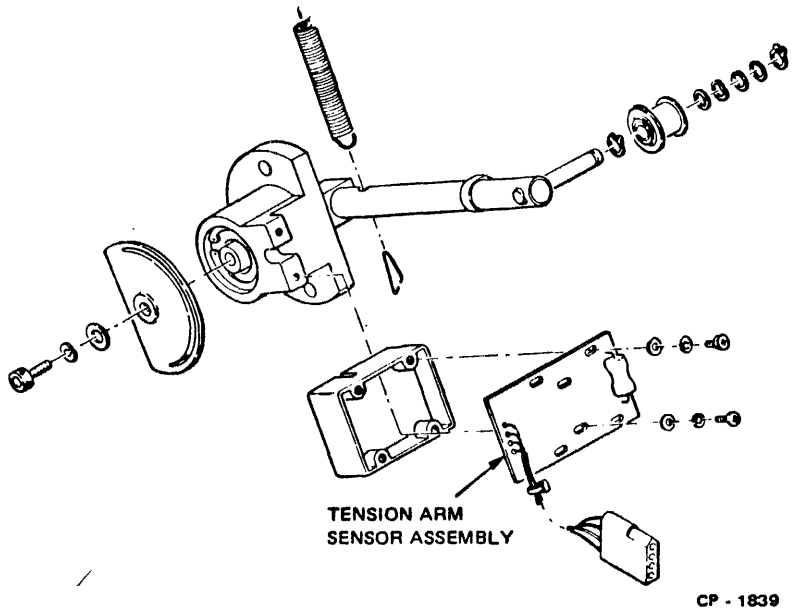


Figure 5-3 Tension Arm Sensor

5.2.7 HP7970E Magtape Drive Two-Year Field Service Preventive Maintenance

1. Replace the capstan wheel. Ensure that the wheel is positioned correctly by verifying that the tape is centered on the wheel while tape is in motion.

2. Replace the four tape roller guides.

NOTE

Return to step 1 of the semiannual PM procedure at this time.

5.3 CORRECTIVE MAINTENANCE TECHNIQUES

If a failure occurs, running the special diagnostic program, Test 6, should aid in isolating the problem. Should the diagnostic fail to run completely, the proper approach is to load suitable subroutines as outlined in Paragraph 3.5. Tests in this case should follow a systematic sequence, investigating some of the basic functions in the following order:

1. Control Register (T04)
2. GO BIT and GOP logic (T06)
3. Function Decoder (T06)
4. MTT commands (T07)
5. Gap Timing (T08)
6. Buffer Control (T11)

If the foregoing sections are operational, it should be possible to run the special diagnostic and investigate any remaining problems. Test 6 of the diagnostic program contains some useful subsets that can be used for solving most problems.

CHAPTER 6
SPARE PARTS

6.1 MODULES

Table 6-1 lists the module complement of the TR79-FA by type, quantity, and function. For maximum maintainability, it is suggested that a spare level of at least one of each module type be maintained at all times. Refer to the Module Utilization sheet (TR79-F-T01) in the TR79-FA Engineering Drawing Set for module slot locations.

Table 6-1
TR79-FA Module Complement

Module	Description	Quantity
M105	Address Selector	1
M111	Inverter	5
M112	2-Input NOR	4
M113	2-Input NAND	8
M115	3-Input NAND	3
M117	4-Input NAND	3
M119	8-Input NAND	2
M121	AND-NOR GATE	1
M149	9X2 NAND WIRED OR	2
M162	Parity Circuit	3
M163	Binary to Decimal Decoder	1
M203	R/S Flip-Flop	2
M204	J/K Flip-Flop (Gates)	1
M205	D-Type Flip-Flop	8
M206	D-Type Flip-Flop (Common CLEAR)	9
M207	J/K Flip-Flop	1
M302	Delay Multivibrator (3 input)	5
M304	Delay Multivibrator (2 input)	1
M306	Integrating One Shot	2
M606	Pulse Generator	5
M617	4-Input Power NAND	1
M622	2-Input Bus Driver	3
M783	Unibus Driver	2
M784	Unibus Receiver	2
M795	Word Count-Bus Address Registers	1
M796	Master Control	1
M798	Unibus Driver	1
M906	Cable Terminator	2
M912	Cable Connector	2
M930	Bus Terminator	1
M1103	2-Input AND	2
M1307	4-Input AND	1
M7821	Interrupt Control	1
G736	Jumper Card	1

APPENDIX A
TR79-FA TEST PROGRAM DESCRIPTION

A.1 ABSTRACT TR79-FA TEST (MAINDEC-11-DZTRA)

1. Test One – Logic test having minimum tape motion.
2. Test Two – Logic test with tape motion near load point.
3. Test Three – Reliability test with continuous tape motion over the entire tape.
4. Test Four – Read portion of the Compatibility Test which reads tapes written by test three.
5. Test Five – Maintenance test which allows the operator to select any subtest and execute these in any desired order. Also manual operations test.

A.2 REQUIREMENTS

Minimum requirements for running this program follow:

1. PDP-11 Computer
2. Magnetic tape transport control interface
3. 12K words of memory
4. Console teleprinter
5. Paper tape reader

A.3 LOADING PROCEDURE

The program is in Absolute Binary Format and is loaded using the Absolute Loader.

A.4 STARTING PROCEDURE

```
;STARTING PROCEDURE
;LOAD PROGRAM
;LOAD ADDRESS 000200
;PRESS START
;PROGRAM WILL TYPE "MAINDEC-11-DZTRAA /<377>/TR79F CHECKOUT TESTS"
;PROGRAM WILL TYPE "RUNNING" TO INDICATE THAT TESTING HAS STARTED
;AT THE END OF A PASS, PROGRAM WILL TYPE PASS COMPLETE MESSAGE
;AND THEN RESUME TESTING
```

A.4.1 Test Selection

When the "SELECT TEST NUMBER ..." typeout occurs, the operator selects the desired test by typing the test number followed by a carriage return.

NOTE

Switches are in the normal position (clear) when down. The switch options in Table A-1 are available to the operator.

Table A-1
Switch Options

```
;SWITCH REGISTER OPTIONS
;-----------------

SW15=100000              ;=1, HALT ON ERROR
SW14=40000               ;=1, LOOP ON CURRENT TEST GROUP
SW13=20000               ;=1, INHIBIT ERROR TYPEOUT
SW12=10000               ;=1, DELETE TYPEOUT/BELL ON ERROR.
SW11=4000                ;=1, INHIBIT ITERATIONS
SW10=2000                ;=1, ESCAPE TO NEXT TEST ON ERROR
SW09=1000                ;=1, LOOP WITH CURRENT DATA
SW08=400                 ;=1, LOOP ON ERROR
SW07=200
SW06=100  - INHIBIT AUTO SIZE
SW05=40
SW04=20
SW03=10
SW02=4                   ;=1, LOCK ON TEST SELECT
SW01=2                   ;=1, RESTART PROGRAM AT SELECTED TEST
SW00=1                   ;=1, SELECT DEVICE ADDRESS, VECTOR, ETC.
```

A.5 OPERATING PROCEDURE

Upon loading, the teleprinter prints information concerning the operation of the program and the tests available. After the heading is printed, the operating parameters are displayed and checked by the operator. If it is desired to change a parameter, type the desired value followed by a Carriage Return. If no change is needed, a Carriage Return will retain the present value as the operating parameter.

A.6 TEST ABSTRACT

A.6.1 PRETST: Pretest

This test checks the reset function. It is performed each time a test is selected.

A.6.2 Test 1

Test 1 is a logic test which checks the interface logic.

A.6.3 Test 2

Test 2 is a logic test which tests the transport response to all types of commands.

A.6.4 Test 3
Test 3 is a reliability test which checks the ability of the transport and the interface to operate without error over an extended period of time.

A.6.5 Test 4
Test 4 is the read part of a compatibility test. This test reads tapes written by Test 3.

A.6.6 Test 5
Test 5 is a maintenance aid. This routine allows the operator to loop on any subtest by entering the starting address at the teleprinter. The loop control maintains the selected test running. If loop is not selected, the test will execute once and another starting address must be entered. Test 5 also validates that the TR79-FA can be placed off-line by the program. Operator intervention is required and the operator is instructed by TTY commands. An EOT reflective strip should be installed about 50 ft from End of Tape. This is for diagnostic purposes only.

NOTE

If errors detected in both Tests 3 and 4 have identical pass numbers, a defective tape should be the first consideration.

A.7 ERRORS
Two basic error typeouts occur. The first contains the following information:

1. PASS XXX

SUBTEST	PC	STATUS	CORRECT	ACTUAL	LOCATION
XXXXXX	XXXXXX	XXXXXX	XXXXXX	XXXXXX	XXXXXX

2. PASS = (THIS IS THE CURRENT PASS NUMBER)
   SUBTEST = (THIS IS THE STARTING ADDRESS OF THE CURRENT SUBTEST BEING EXECUTED)
   PC = (THIS IS THE PC FROM WHICH ERROR WAS CALLED)
   STATUS = (THIS IS THE CONTENTS OF THE PROCESSOR STATUS REGISTER AT THE TIME OF THE ERROR)
   CORRECT = (THIS IS WHAT SHOULD HAVE BEEN IN THE REGISTER OR LOCATION BEING TESTED)
   ACTUAL = (THIS IS WHAT WAS IN THE REGISTER OR LOCATION AT THE TIME IT WAS EXAMINED)
   LOCATION = (THIS IS THE LOCATION THAT WAS IN ERROR)
   COMMENT = (OPTIONAL)

The remaining typeout provides the pass, PC, and SR. When this short error printout is typed, the message which follows provides ample information concerning the error.