1.0 System Description

1.1 General Information

The TU16/TM02 tape system will consist of between one and eight tape drives and a single electronics package which will serve as an interface between any one of those drives and a Massbus controller.

1.2 Definition

For the purposes of this specification, the following definitions apply:

1.2.1 Controller - any Massbus controller.

1.2.2 Slave - a tape transport.

1.2.2.1 Selected Slave - that slave whose select code appears in bits 0-2 of the Tape Control (TC) Register.

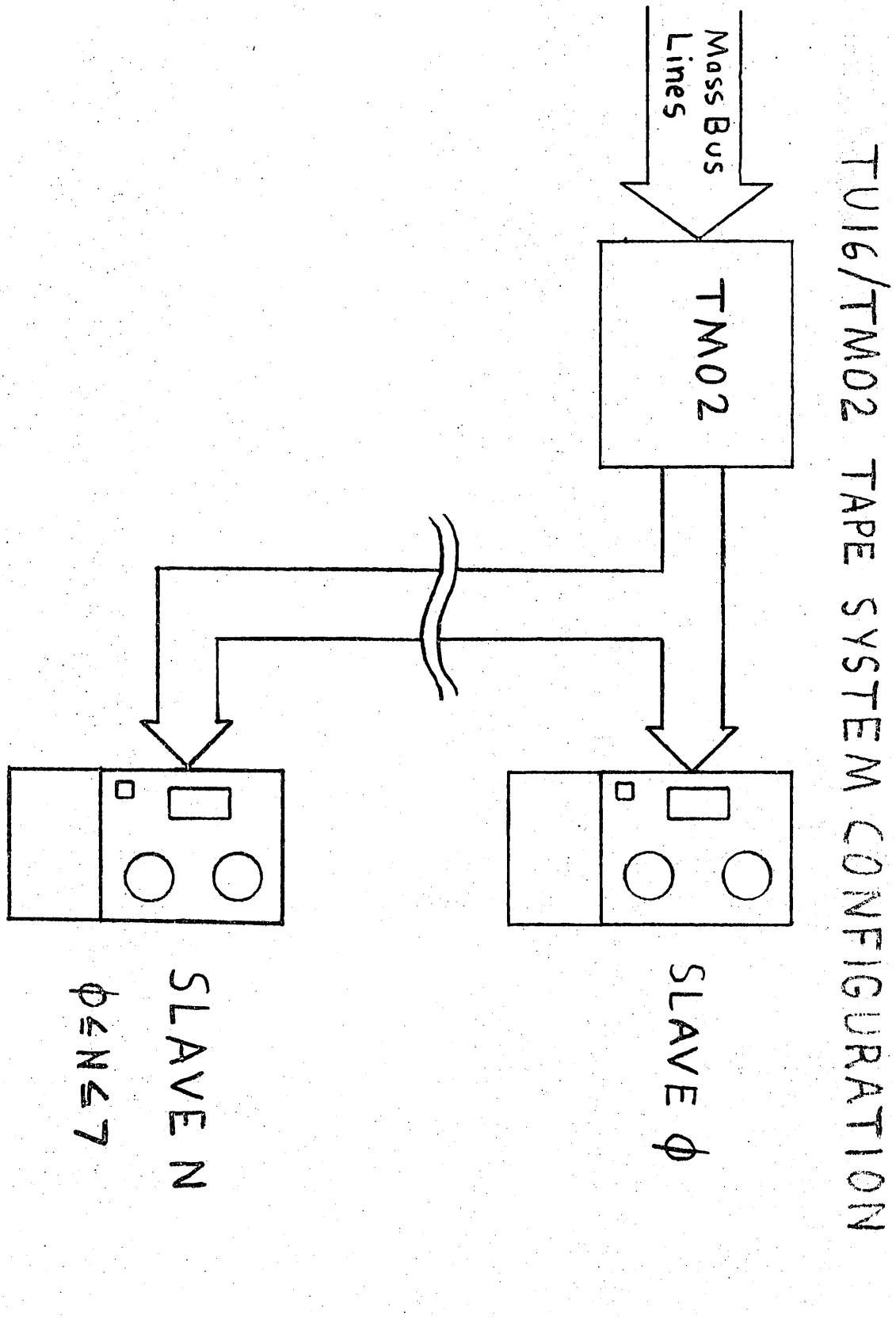
1.2.3 TM02 - defined operationally. The TM02 electronics package interfaces to the controller. It accepts commands which a selected slave must execute while providing the controller with information about the status of the slave. During data transfers the TM02 controls fetching, formatting, and sending of data. The TM02 also oversees the handling of error conditions and slave servicing requirements.

1.2.4 Drive - When bits 0-2 of the Tape Control Register in the TM02 contain the select code of an existing slave, then the Master and the selected slave together become equivalent to what is defined as a "drive" in the Massbus Specification. No more than one slave may be legally selected at any time, and commands can not be issued to unselected slaves. However, unselected slaves are able to make important status changes known to the Controller. (See SSC bit of Status Register.)

1.3 System Configuration

The following block diagram illustrates the configuration of a TU16/TM02 tape system:

TITLE



TU16/TM02 TAPE SYSTEM CONFIGURATION

	SIZE	CODE	NUMBER	REV
	A			

1.4 Applicable Documents

Before reading this document, the reader should familiarize himself with the Massbus Specification. In addition, attempts to program the TU16/TM02 system should be prefaced by a thorough study of the programming manual for the particular Massbus controller with which the program will interface.

2.0 Commands Implemented

2.1 Commands will be executed only if they are directed to ONLINE slaves. The following commands will be implemented on the TU16 tape system. Functions codes not listed here will be treated as illegal functions.

F5	F4	F3	F2	F1	Operation Name
0	0	0	0	0	No-op
0	0	0	0	1	Rewind, Offline
0	0	0	1	1	Rewind
0	0	1	0	0	Drive Clear
0	1	0	0	0	Write Filemark
0	1	0	1	0	Erase
0	1	1	0	0	Space Forward
0	1	1	0	1	Space Reverse
1	0	1	0	0	Write Check Forward
1	0	1	1	1	Write Check Reverse
1	1	0	0	0	Write Forward
1	1	1	0	0	Read Forward
1	1	1	1	1	Read Reverse

2.1.1 The requirement for a "read-in" mode on the TU16/TM02 system will engender either one or two additional commands. Details of the "read-in" commands and sequencing will be published at a later date.

2.2 Description of Commands

2.2.1 NO-OP: Causes immediate reset of GO and assertion of DRY. No tape motion or status change occurs in the selected slave. No attention generated.

2.2.2 REWIND, OFFLINE: The selected slave begins rewinding and goes OFFLINE. GO is reset and DRY, SLA, SSC, and ATA become asserted (SLA and SSC are asserted because the slave has gone OFFLINE). Operator intervention is required to bring the slave back ONLINE.

NOTE: This command generates only one Attention, whereas a REWIND command may generate either one or two Attentions.

2.2.3 REWIND: The selected slave executes a rewind back to the reflective strip marking beginning of tape (BOT). Sequencing of a REWIND command proceeds as follows

2.2.3.1 When a REWIND command is loaded with GO = 1, the drive first checks the Settledown (SDWN) bit in the Status Register.

a) If SDWN = Ø, the selected slave immediately begins rewinding.

b) If SDWN = 1 (indicating that the selected slave is slowing to a halt after completion of a prior command) and the last command loaded called for tape motion in the REVERSE direction, the selected slave immediately begins rewinding.

c) If SDWN = 1 and the last command loaded called for tape motion in the FORWARD direction, the TM02 delays execution of the REWIND until SDWN = Ø, indicating that the drive has stopped. The maximum length of the Settledown interval on TU16 is 15 milliseconds.

2.2.3.2 As soon as the slave has recognized the REWIND command, the drive returns to the ready state and DRY and ATA become asserted. In cases 2.2.3.1 a) and b), the time from initiation of the Control Bus write sequence which loads the REWIND command until re-assertion of DRY is less than 2 microseconds. In case c), re-assertion of DRY may not occur for up to 15 milliseconds after initiation of the REWIND sequence.

2.2.3.3 Once the selected slave reaches BOT, it will cause SLAVE ATTENTION (SLA) to become asserted, in turn causing SLAVE STATUS CHANGE (SSC) and ATA to become asserted. If the selected slave was already at BOT when the REWIND command was loaded, the ATA condition generated in section 2.2.3.2 and the ATA condition generated in section 2.2.3.3 will occur so close together in time that they will be indistinguishable to the programmer.

2.2.3.4 The following examples will indicate the states of important status bits during a rewind sequence. For simplicity, the possibility of SLA and SSC becoming asserted due to status changes in slaves other than the rewinding slave will not be treated.

a) During the time between reception of the REWIND command and initiation of a rewind by the selected slave: DRY = Ø, ATA = Ø, SSC = Ø, SLA = Ø, SDWN = Ø or 1, PIP = Ø.

b) After initiation of the rewind, if the selected slave was already at BOT: DRY = 1, ATA = 1, SSC = 1, SLA = 1, SDWN = Ø, PIP = Ø.

c) After initiation of the rewind, if the selected slave was not at BOT: DRY = 1, ATA = 1, SSC = Ø, SLA = Ø, SDWN = Ø, PIP = 1.

d) After completion of the rewind, if the selected slave was not already at BOT: DRY = 1, ATA = 1, SLA = 1, SSC = 1, SDWN = Ø, PIP = Ø. (Identical to case 2.2.3.4 b)

e) Note that SSC is an indication of status changes in at least one slave. Thus, it should not be cleared until all slaves have been polled to confirm their status.

2.2.3.5 In a multi-slave system the presence of rewinding slaves on the TM02-TU16 bus does not interfere with the execution of commands by selected slaves which are not rewinding. Any command recognized as a legal function by the TU16 may be issued to a rewinding slave if DRY = 1. If this is done, the following sequence of events will occur:

a) When command is loaded, GO becomes asserted;

b) Execution of command is deferred until rewind is complete (until PIP becomes negated); GO remains asserted;

c) When rewind reaches completion, PIP becomes negated and SLA becomes asserted; command execution is initiated.

d) When command reaches completion, ATA becomes asserted because of prior assertion of SLA.

NOTE THAT, WORST CASE, THIS SEQUENCE COULD CAUSE THE ENTIRE TU16 SYSTEM TO GO BUSY FOR UP TO 5 MINUTES. IF A DATA TRANSFER COMMAND IS ISSUED TO A REWINDING SLAVE, DATA BUS TIMING RESTRICTIONS MAY BE VIOLATED.

2.2.4 DRIVE CLEAR: Performs reset on TM02 and selected slave, does not affect unselected slaves. Like any other command, DRIVE CLEAR can be loaded into the TU16/TM02 system only if DRY = 1.

DRIVE CLEAR command resets: SLA in selected slave, SSC (if no other slaves have current attention-demanding conditions), IDB, ERR, ATA in STATUS Register; resets all but bit 6 of MAINTENANCE Register; resets FCL in TAPE CONTROL Register; resets all bits in ERROR Register except bit 14 (UNS), and resets UNS if the TM02 is not experiencing a power-fail.

The time from reception of a DRIVE CLEAR command to re-assertion of DRY = 1 is 2 microseconds (maximum). If DRIVE CLEAR is issued to a TM02 which is experiencing a power-fail, ATA and ERR will become asserted when DRY becomes asserted. DRIVE CLEAR cannot affect a rewinding slave.

2.2.5 WRITE FILEMARK: The selected slave writes an extended (3") inter-record gap, a filemark, and stops. ATA becomes asserted when DRY becomes asserted; EOF will be asserted if a detectable filemark was written (this is the normal case).

2.2.6 ERASE: The selected slave writes an extended inter-record gap and stops. ATA becomes asserted when DRY becomes asserted.

2.2.7 SPACE FORWARD: The selected slave spaces forward (towards EOT) over the number of records specified by the contents of the Frame Count Register. Detection of a filemark (EOF) causes a SPACE command to be aborted.

All data errors are inhibited during this operation. DRY becomes asserted when operation is complete and a valid inter-record gap found. ATA becomes asserted when DRY asserted.

2.2.8 SPACE REVERSE: Like SPACE FORWARD, except that detection of BOT or EOF will abort the operation, and that the direction of tape motion is in the reverse direction (towards BOT).

2.2.9 READ FORWARD/WRITE CHECK FORWARD:

The tape system makes no distinction between these commands.

The tape system reads one record. Data transmission will normally be terminated by detection of FRAME COUNT overflow. See Chapter 4 for a discussion of other causes of transmission terminations.

2.2.10 READ REVERSE/WRITE CHECK REVERSE:

This operation is identical to READ (WRITE CHECK) FORWARD with the following exceptions: Massbus data transfers occur in the order shown in Chapter 6, and tape motion is on the reverse direction.

2.2.11 WRITE:

Transport writes one record while moving forward. Record length is controlled by the FRAME COUNT Register. See Chapter 4 for a discussion of other types of terminations.

2.3 INIT: INIT differs from DRIVE CLEAR with the following aspects:

a) INIT may be issued at any time,

b) INIT affects all slaves, not just the selected slave;

c) INIT clears EOF in the STATUS Register.

INIT resets:

GO, SLA (all slaves), SSC, EOF, IDB, ERR, and ATA in the STATUS Register; resets all but bit 6 of MAINTENANCE Register, resets FCL in TAPE CONTROL Register; resets all bits in ERROR Register except bit 14 (UNS), and resets UNS if the TM02 is not experiencing a power-fail. INIT sets DRY.

INIT, like DRIVE CLEAR, requires 2 microseconds (maximum) for completion. If the TM02 is experiencing a power-fail when INIT is issued, ATA and ERR will be asserted at the completion of the system reset.

INIT has no effect on a rewinding slave, but will halt a slave which is executing any other command.

NOTE: Issuing an INIT during a write operation ruins the record being written. The only safe recovery from INIT is a rewind.

3.0 Registers Implemented

3.1 The following registers will be implemented in the TU16 Tape System:

Type	Register	Name
R/W	00	CONTROL I (CSI)
Read	01	STATUS (DS)
Read	02	ERROR (ER)
R/W	03	MAINTENANCE (MT)
R/W	04	ATTENTION SUMMARY (AS)
R/W	05	FRAME COUNTER (FC)
Read	06	DRIVE TYPE (DT)
R/W	07	TAPE CONTROL (TC)
Read	10	CHECK CHARACTER (CC)
Read	11	SERIAL NUMBER (SN)

3.2 Description of Control I Register

The CSI Register will be used as defined in the Massbus Specification. Loading this register with a GO Bit and a valid function code will initiate a cycle to check for the various possible error conditions and, if no errors are detected, initiate command execution.

3.2.1 Bits in the Control Register

3.2.1.1 BIT 0 - GO BIT:

Loading a "1" in this bit initiates a command execution cycle. When this bit is set, the selected slave becomes busy, and no other slaves may be used. This bit is reset by the drive when the drive returns to the DRY condition. (Logical address of the current selected slave is described in TC Register discussion.) The GO bit is cleared by an INIT.

3.2.1.2 BITS 1 to 5 - F1 to F5

Function Code bits (See Section 2). INIT and DRIVE CLEAR have no effect on bits 1-5.

3.2.1.3 BIT 11 - DRIVE AVAILABLE (DVA)

Always set in TU16.

3.2.1.4 For a description of the other CSI bits, consult the Massbus specification, and the various controller specifications.

3.3 Description of the STATUS Register:

The status register indicates the status of various sections of the drive. Individual bits which are generated in the selected slave will be followed by (SS). Bits which can be generated by any slaves will be followed by (S). Bits which are generated in the TM02 will be followed by (M).

3.3.1 Bits in the Status Register:

3.3.1.1 Bit 0 - SLAVE ATTENTION (SLA) - (SS):

Asserted by a selected slave which requires attention for one of the following reasons: REWIND completed, detection of power fail, coming ONLINE, going OFFLINE. SLA is cleared by DRIVE CLEAR or INIT (sections 2.2.4, 2.3.1).

3.3.1.2 BIT 1 - BEGINNING OF TAPE (BOT) (SS):

Asserted whenever the selected slave detects the BOT marker. INIT and DRIVE CLEAR cannot affect this bit.

3.3.1.3 BIT 2 - END OF FILE (EOF) (M):

Asserted when a filemark is detected: remains asserted until the next tape motion operation is initiated. The Phase Encoded filemark written by TU16 consists of 40 characters with zero's in tracks 1, 2, 4, 5, 7, and 8 and with tracks 3, 6, and 9 DC erased. The NRZI filemark written by the TU16 consists of a single character record followed by the LRC for that record.

The single record contains octal 023 on 9-Track slaves and octal 017 on 7-Track slaves. EOF should be high after the completion of a WRITE FILEMARK command.

INIT clears EOF, DRIVE CLEAR does not affect it.

3.3.1.4 BIT 3 - IDENTIFICATION BURST (IDB) (M):

Set on recognition of the PE identification burst. In the forward direction the bit remains set thru the READING, WRITING, OR SPACING operation. On a PE tape, IDB should be asserted after any tape motion operation which began from BOT. IDB becomes reset when another command is issued. Cleared by INIT or DRIVE CLEAR.

3.3.1.5 BIT 4 - SLOWING-SETTLING DOWN (SDWN) (SS):

This bit is set during the period when tape motion is stopping. DRY is asserted on the leading edge of SDWN. DRIVE CLEAR and INIT cannot affect this bit.

3.3.1.6 BIT 5 - PHASE ENCODED STATUS (PES) (SS):

This bit reflects the format mode in which the formatter is operating. PES originates in the selected slave and in TU16 should be identical to BIT 10 in TC register. It is asserted when selected slave in PE mode, negated when selected slave in NRZI mode. DRIVE CLEAR and INIT cannot affect this bit. (See also bits 8-10 of TAPE CONTROL Register).

3.3.1.7 BIT 6 - SLAVE STATUS CHANGE (SSC) (M):

This bit is asserted and latched by the TM02 whenever any slave has an attention condition as defined in Section 3.3.1.1

Setting SSC results in ATA becoming asserted as soon as DRY becomes asserted, (ATA becomes asserted immediately if DRY is already asserted.)

INIT always clears SSC. DRIVE CLEAR clears SSC if only the selected slave has a current attention condition. Note that power-fail in a slave is a transient attention condition, and that SSC should not be cleared before polling all slaves to confim their status.

3.3.1.8 BIT 7 - DRIVE READY (DRY) - (M):

Asserted at completion of any command. INIT sets DRY.

3.3.1.9 BIT 8 - DRIVE PRESENT (DPR) - (M):

Always asserted in the TU16 system.

3.3.1.10 BIT 9 - NEUTRAL (NTL) - (M):

Always negated in the TU16 system.

3.3.1.11 BIT 10 - END OF TAPE (EOT) - (SS):

When the EOT marker is recognized during forward tape motion, this bit is set. It is reset when the EOT Marker is passed over during reverse tape motion. DRIVE CLEAR and INIT do not affect EOT.

3.3.1.12 BIT 11 - WRITE LOCK (WRL) - (SS):

Asserted whenever a reel of tape without a write enable ring is loaded on the selected slave. DRIVE CLEAR and INIT cannot affect this bit.

3.3.1.13 BIT 12 - MEDIUM ON LINE (MOL) - (SS):

The selected slave is loaded and the online switch activated. This condition is necessary for response to any commands, i.e., if GO = 1 and MOL = Ø, command is aborted, and UNS and ATA become asserted. DRIVE CLEAR and INIT cannot affect this bit.

3.3.1.14 BIT 13 - POSITIONING IN PROCESS (PIP) -

Asserted during SPACE (M) and REWIND (SS) operations. Cleared by INIT during SPACE operations. Unaffected by DRIVE CLEAR or INIT during REWIND operations, DRIVE CLEAR cannot be issued during SPACE operations.

3.3.1.15 BIT 14 - COMPOSITE ERROR (ERR) - (M):

Asserted whenever any error bit in the Error (ER) register is asserted. Reset by Drive Clear or INIT. (See Sections 2.2.3.4 and 2.3.)

3.3.1.16 BIT 15 - ATTENTION ACTIVE (ATA) - (M):

See Section 5.

3.4 Description of the ERROR Register. See Section 4 for descriptions of error-handling algorithms.

3.4.1 Bits in the ERROR Register

3.4.1.1 BIT 0 - ILLEGAL FUNCTION (ILF):

Asserted when GO bit is loaded with a "1", and BITS F1 to F5 of CSI do not denote a function implemented by the TU16. Cleared by INIT or DRIVE CLEAR.

3.4.1.2 BIT 1 - ILLEGAL REGISTER (ILR):

Asserted if the Controller addresses a register which is not implemented on the TU16. No register modification should occur. On a Control Bus read, all zeros are gated onto CONTROL lines. Cleared by INIT or DRIVE CLEAR.

3.4.1.3 BIT 2 - REGISTER MODIFICATION REFUSED (RMR):

Asserted whenever the controller attempts to write into any implemented TU16 Register except Register 3 (Maintenance) or Register 4 (Attention Summary) while the GO bit is asserted. If RMR occurs, the addressed register is not modified; ATA becomes asserted as soon as DRY is asserted. Cleared by INIT or DRIVE CLEAR.

3.4.1.4 BIT 3 - MASSBUS PARITY ERROR (PAR):

Asserted whenever a parity error is detected on the Massbus DATA Lines or CONTROL Lines when data is being transmitted from the Controller to the TM02. ATA becomes asserted as soon as DRY is asserted. No register modification should occur on CONTROL bus writes. Cleared by INIT or DRIVE CLEAR.

3.4.1.5 BIT 4 - FORMAT ERROR (FMT):

Asserted whenever a data transfer command is loaded with GO = 1 and the tape format code loaded in the TC Register is not implemented on that TM02. Tape motion is inhibited; EXC and EBL are raised. DRY and ATA become asserted when EBL becomes negated. Cleared by INIT or DRIVE CLEAR.

3.4.1.6 BIT 5 - FORMATTER PARITY ERROR (FPAR):

Asserted whenever a parity error is detected during the process of transforming tape word images into Massbus word images. (Will not be implemented on all tape formats.) ATA becomes asserted when DRY becomes asserted. Cleared by INIT or DRIVE CLEAR.

3.4.1.7 BIT 6 - INCORRECTABLE DATA ERROR/VPE (INC/VPE):

Asserted when performing a data transfer on a PE slave and multiple dead tracks, dead tracks without parity errors, parity errors without dead tracks, or skew overflow are detected.

Asserted when performing a data transfer on an NRZ slave and a vertical parity error is detected. Cleared by DRIVE CLEAR or INIT.

3.4.1.8 BIT 7 - FORMAT ERROR/LRC (PEF/LRC):

In PE mode this bit is asserted whenever an invalid preamble or postamble is discovered. In NRZ mode, the bit is asserted when the LRC character generated from readback data does not match the LRC character read from tape. ATA becomes asserted when DRY becomes asserted. Cleared by INIT or DRIVE CLEAR.

3.4.1.9 BIT 8 - BAD TAPE ERROR (BTE):

Asserted whenever any tape characters are read while the read head is scanning the first half of the inter-record gap. ATA becomes asserted when DRY becomes asserted. Cleared by INIT or DRIVE CLEAR.

3.4.1.10 BIT 9 - FRAME COUNT ERROR (FCE):

Asserted whenever a SPACE, READ, or WRITE terminates and the FRAME COUNTER contains any number but octal 0000. ATA becomes asserted when DRY becomes asserted. Detection of this error is affected by state of INHIBIT RECORD LENGTH ERROR and IGNORE FRAME COUNT bits in TAPE CONTROL Register. FCE cleared by INIT or DRIVE CLEAR. (See IFC bit, Section 3.9.8)

3.4.1.11 BIT 10 - CORRECTABLE SKEW/ILLEGAL FILE MARK (CS/IFM):

In PE mode, this bit is asserted when excessive but correctable skew is detected in data read back from tape. It is a warning only, and does not indicate that bad data was read from tape.

In NRZ mode, this bit is asserted when a bit pattern is detected on tape which has the general characteristics of an NRZ filemark (specifically, a one-character record followed by another one-character record spaced an appropriate distance away from the first) but which does not contain the exact data expected in an NRZ filemark. When such a bit pattern is detected in NRZ mode, both EOF in the DS Register and CS/IFM in the ER Register will become asserted.

CS/IFM is cleared by DRIVE CLEAR or INIT. (See Figure 4.1.3.1.)

3.4.1.12 BIT 11 - NON-EXECUTABLE FUNCTION (NEF):

Asserted whenever one of the following occurs:

3.4.1.12.1 Write operation requested with WRL status bit asserted.

3.4.1.12.2 SPACE REVERSE or READ REVERSE or WRITE CHECK REVERSE requested with BOT status bit asserted.

3.4.1.12.3 PE/NRZI bit loaded into TC Register does not agree with PES status bit asserted by selected slave.

3.4.1.12.4 SPACE, READ, or WRITE command is loaded with GO = 1 and FCL in TAPE CONTROL Register = Ø and IFC in TC Register = Ø.

3.4.1.12.5 READ or WRITE command is loaded with DEN2 in TAPE CONTROL Register = 0 and FRAME COUNT Register set to two's complement of 1 or 2 and IFC = Ø. (Minimum NRZ record length is 3 data characters.)

Cleared by INIT or DRIVE CLEAR.

3.4.1.13 BIT 12 - DRIVE TIMING ERROR (DTE):

Asserted whenever one of the following occurs:

a) During a WRITE operation, a SCLK signal was generated, and a WCLK signal was not received in time to provide valid data for the next tape character written.

b) A data transfer command was loaded into the TU16/TM02 system while OCC = 1.

Case a) can be distinguished from case b) by looking at the FRAME COUNT Register. In case a), the FC Register will have been incremented at least once since its loading. In case b), the FC Register will contain the same number with which it was loaded prior to the loading of the data transfer command. Also, DTE during a READ operation can occur only due to case b). DTE is cleared by INIT or DRIVE CLEAR.

3.4.1.14 BIT 13-- OPERATION INCOMPLETE (OPI):

Asserted if no record is detected within 7 seconds after initiation of a READ or SPACE command. Asserted if no record is detected within 0.7 seconds after initiation of a WRITE command. (Initiation of a command = setting GO to 1 with bits F1 to F5 of CSI Register set to the Function Code for that command.) OPI is cleared by INIT or DRIVE CLEAR.

3.4.1.15 BIT 14 - DRIVE UNS (UNS):

Asserted if GO = 1 and MOL in ST Register = Ø. Also asserted if TM02 detects imminent power-fail condition. (AC LO signal is asserted, DC LO signal not asserted. See A-SP-5409728-0-8.)

If UNS is caused by GO = 1 while MOL = 0, it is cleared by INIT or DRIVE CLEAR. If UNS is caused by a transient voltage - low condition, it can be cleared by INIT or DRIVE CLEAR when voltage returns to an acceptable level. If UNS is caused by a permanent voltage - low condition, it cannot be cleared. (See Figure 4.1.3.2.)

3.4.1.16 BIT 15 - CORRECTABLE DATA ERROR/CRC ERROR (COR/CRC):

In PE mode, this bit becomes asserted whenever a tape parity error and a single dead track occur on the same tape character. In this case, the data bit in the dead track is inverted to correct the parity error.

In NRZ mode, this bit is asserted when the CRC character generated from readback data does not agree with the CRC read from tape.

COR/CRC is cleared by DRIVE CLEAR or INIT. (See Figure 4.1.3.1.)

3.4.2 Table 3.4.2 describes those errors which might reasonably be detected during normal operation of the TU16/TM02 system.

ENGINEERING SPECIFICATION — CONTINUATION SHEET

TITLE

OPERATIONS ↓ / ERRORS →	ILF	ILR	RMR	PAR	FMT	FPAR	INC/VPE	PEF/LRC	BTE	FCE	CS/IFM	NEF	DTE	OPI	UNS	COR/CRC
WRITE TO ANY REGISTER *		X	X	X												
READ FROM ANY REGISTER		X														
LOAD NO-OP WITH GO=1	X	X	X	X								X			X	
LOAD REWIND OFF LINE WITH GO=1	X	X	X	X								X			X	
" REWIND " GO=1	X	X	X	X								X			X	
" DRIVE CLEAR " GO=1	X	X	X	X											X	
" WRITE FMK " GO=1	X	X	X	X			X	X	X	X	X	X		X	X	
" ERASE " GO=1	X	X	X	X			X	X	X	X	X	X			X	
" SPACE FWD " GO=1	X	X	X	X						X	X	X		X	X	
" SPACE REV " GO=1	X	X	X	X						X	X	X		X	X	
" WRITE CHECK FWD " GO=1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
" WRITE CHECK REV " GO=1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
" WRITE FWD " GO=1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
" READ FWD " GO=1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
" READ REV " GO=1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MASS BUS INIT															X	
WRITE TO AS . OR MT REG		X		X												

* Except AS OR MT

TABLE 3.4.2 : TM02 OPERATIONS WITH ERRORS WHICH COULD BE DETECTED DURING THOSE OPERATIONS AND REMAIN ASSERTED AFTER THE OPERATION IS COMPLETE

SIZE	CODE	NUMBER	REV
A			

SHEET ____ OF ____

DEC FORM NO DEC 16-(381)-1022-N370
DRA 108

3.5 Description of MAINTENANCE (MT) Register

The MT Register will serve in the following capacity:

a) It will provide data wraparound paths for checking the various sections of the data formatting logic in the TM02.

b) It will provide a means for testing error detection circuitry within the TM02.

c) It will act as a storage buffer for the Longitudinal Parity Check (LRC) Character when operating in NRZ mode.

Bits in the MT Register are allocated in the following manner:

3.5.1 BIT Ø - Maintenance Mode (MM)

Must be written to '1' when any Maintenance Mode function is desired. Setting the MM bit to '1' does not initiate any action on the part of the drive, but rather alters the manner in which the drive executes various commands. The manner in which command execution is altered depends on the Maintenance operation code resident in bits 1-4 of the MT Register.

The MM bit is cleared by DRIVE CLEAR or INIT.

3.5.2 BITS 1 to 4 - Maintenance Op Code bits (MOP Ø-3):

These bits control the Maintenance function which will occur when the MM bit is set to '1' and the TM02 is loaded with the appropriate command.

MOP Ø-3 are cleared by DRIVE CLEAR or INIT.

3.5.3 BIT 5 - Maintenance Mode Clock (MC)

This bit controls the sequencing of data through the TM02 data paths when operating in Maintenance mode. Cleared by DRIVE CLEAR or INIT, or by writing the MM bit to 'Ø'.

3.5.4 BIT 6 - Selected Slave Clock (SCK):

This bit displays the signal WRT CLK, which is transmitted to the TM02 from the selected slave. The frequency of this clock is dependent both upon the Density Select bits located in bits 8-10 of the Tape Control Register and upon the operating speed of the selected slave. Its purpose is to enable a check on the proper decoding of the Density Select bits by the selected slave.

This bit cannot be cleared.

3.5.5 BITS 7 to 15 - Maintenance Data Field (MDF Ø-8):

These bits act as a buffer for data generated during checks of the TM02 data paths.

In addition, at the end of data transfer operations in NRZ mode, this field holds the LRC character for the last record read.

MDF Ø contains the parity bit for the maintenance data character. MDF 1 contains the least significant bit of the maintenance data character, and the remaining higher order bits are contained, in order, in MDF 2 through 8.

3.6 ATTENTION SUMMARY Register

This Register will be handled in accordance with the Massbus Specification. During a Control Bus write to Register 04, the Control line corresponding to the TM02's logical address on the Massbus will be gated to the ATA bit. During a ControlBus read of Register 04, the TM02's ATA bit will be gated onto the C line corresponding to the TM02's logical address on the Massbus. For further discussion of the ATA bit, see Section 4.

3.7 Description of the FRAME COUNT Register

The frame counter does exactly what its name implies: it counts tape frames.

During a data transfer operation, it is incremented each time a six-bit (for 7-track operation) or 8-bit (for 9-track operation) character is transferred to (write) or from (read) tape. During a SPACE operation, the frame counter is incremented once each time a record is detected on tape.

3.7.1 Frame Counter Operation During WRITE's:

Before a WRITE operation is initiated, the Frame Counter must be loaded with the 2's complement of the number of tape characters to be written. (The ratio of actual tape characters written on tape to processor core words involved in the transfer will depend on the tape format used.) Each time a tape character is written, the frame counter will be incremented. In normal circumstances a write operation will terminate when the frame counter overflows to zero.

3.7.2 Frame Counter Operation During READ:

Before a READ operation can be initiated, the Frame Counter must be loaded with the 2's complement of the number of tape characters to be read. The counter is incremented each time a tape character is read. In normal circumstances, the TM02 read timing section will detect the end of a record after the frame counter overflows to zero.

3.7.3 Frame Counter Operation During Spacing Function

Before a Spacing Operation is initiated, the Frame Counter must be loaded with the 2's complement of the number of records to be spaced over. In normal circumstances a spacing operation will terminate when the frame counter overflows to zero.

3.7.4 Errors Related to Frame Counter

See NEF and FCE bits described in Section 3.4. See also IFC bit desribed in Section 3.9.8.

3.7.5 Clearing the Frame Counter

The Frame Counter will be cleared by writing zeros into it. DRIVE CLEAR and INIT cannot affect the bits of the Frame Counter.

3.8 DRIVE TYPE Register

The DT Register will be used to provide the following information:

a) Number of slaves available in the TU16/TM02 system.

b) Number and type of slaves which are in the power-on state.

c) Standardized Massbus data field indicating the TU16/TM02's physical characteristics (bits 11-15).

Bit assignments in the DT Register are the following:

3.8.1 Bits 0 to 8: DRIVE TYPE NUMBER (DT 0-8):

Contains the drive type number for the selected slave. If no slave has been assigned the select code resident in bits 0-2 of the TAPE CONTROL Register, the drive type code readback will be 010_8. If a slave has been assigned the select code resident in bits 0-2 of the TC Register but is not in the power-on state, the drive type code will be 010_8. If a slave has been assigned the select code resident in bits 0-2 of the TC Register and has power-on, the drive type code will be $01X_8$, $0 < X \leq 7$.

. The drive type code assigned to TU16 slaves is 011_8. Neither INIT nor DRIVE CLEAR can affect DTO-8.

3.8.2 Bit 9 - spare

This bit is always negated.

3.8.3 Bit 10 - SLAVE PRESENT (SPR)

If a slave has been assigned the select code resident in bits 0-2 of the TC Register, this bit is asserted (even if that slave is not in a power-on state). Otherwise, this bit is negated. Neither INIT nor DRIVE CLEAR can affect this bit.

3.8.4 Bit 11 - DRIVE REQUEST REQUIRED (DRR):

Never asserted in TU16/TM02 system.

3.8.5 Bit 12 - SEVEN CHANNEL (7CH)

Asserted if the selected slave is a seven-channel unit. Negated if the selected slave is a nine-channel unit. Also negated if the selected slave either is not in a power-on state or else is not physically present on the TM02-slave bus. Neither INIT nor DRIVE CLEAR can affect this bit.

3.8.6 Bit 13 - MOVING HEAD (MOH):

Never asserted in TU16/TM02 system.

3.8.7 Bit 14 - TAPE (TAP):

Always asserted in TU16/TM02 system.

3.8.8 Bit 15 - NOT SECTOR ADDRESSED (NSA):

Always asserted in TU16/TM02 system.

3.9 TAPE CONTROL Register

Bit assignments in the TC Register are the following.

3.9.1 Bits 0 to 2 - SLAVE SELECT CODE:

Specifies select code of selected slave.

Unaffected by INIT or DRIVE CLEAR.

3.9.2 Bit 3 - EVEN PARITY

When this bit is written to '1', even parity will be written on tape, and even parity will be expected when data is read.

This bit is ignored in Phase Encoded (PE) mode.

Neither INIT nor DRIVE CLEAR affect this bit.

3.9.3 FORMAT SELECT CODE:

These bits determine the manner in which Massbus Data Characters will be mapped to tape characters during WRITE operations and in which tape characters will be mapped to Massbus Characters during READ operations.

Format codes are:

0000 - PDP-10	FORMAT:	'10-CORE DUMP'
0001 - PDP-10	FORMAT:	'10-7 TRACK'
0010 - PDP-10	FORMAT:	'10-ASCII'
0011 - PDP-10	FORMAT:	'10-COMPATIBLE'
0110 - PDP-8	FORMAT:	'8 9-TRACK'
0111 - PDP-8	FORMAT:	'8 7-TRACK'
1100 - PDP-11	FORMAT:	'11-NORMAL'
1101 - PDP-	FORMAT:	'11-CORE DUMP'
1110 - PDP-	FORMAT:	'15-NORMAL'
1111 - PDP-	FORMAT:	RESERVED

Formats 0000 to 0011 will be implemented in TM02's containing an M5907 data formatting module. (NOTE: FORMAT CODE 0001 may not be used with a slave which has been programmed to operate in phase-encoded mode.

For-
mats 1100 to 1111 will be implemented on TM02's containing an M5906 data formatting module. Codes not listed here are not implemented.

If the FORMAT SELECT bits specify a format not implemented on a given TU16/TM02 system, and a valid data transfer command is loaded into the CSI Register setting GO = 1, then FORMAT ERROR (FMT, bit 4 of ER Register) will become asserted, and the operation will be aborted.

Neither INIT nor DRIVE CLEAR affects the FORMAT SELECT bits.

3.9.4 Bits 8 to 10 - DENSITY SELECT CODE:

These bits determine the density of data which will be written on tape during WRITE operations and which will be expected of data read back from tape during READ operations.

BIT 10	BIT 9	BIT 8	
DEN 2	DEN 1	DEN Ø	DENSITY
0	0	0	200 BPI NRZ
0	0	1	556 BPI NRZ
0	1	0	800 BPI NRZ
0	1	1	800 BPI NRZ
1	0	0	1600 BPI NRZ
1	0	1	1600 BPI PE
1	1	0	1600 BPI PE
1	1	1	1600 BPI PE

Neither DRIVE CLEAR nor INIT affects the DENSITY SELECT bits.

3.9.5 Bit 11 - INHIBIT FCE ON SHORT RECORD

This bit, when written to '1', will inhibit the setting of the FRAME COUNT ERROR bit (FCE, bit 9 of ER Register) when end of record is detected before Frame Count overflow occurs.

NOTE: In some cases the controller will not respond to the TM02's assertion of END OF BLOCK (EBL: Consult Massbus Specification) by dropping the RUN line (again, consult Massbus Specification). Should this occur, the TM02 will assert FRAME COUNT ERROR, indicating to the controller that the TM02 has completed command execution. Consult the programming manual for the various Massbus Controllers for further details. Neither INIT nor DRIVE CLEAR affects this bit.

3.9.6 Bit 12 - ENABLE ABORT ON WRITE ERROR:

This bit, when written to '1', will cause a write operation to be aborted as soon as one of the following errors is detected:

a) Parity error on Massbus Data Bus;

b) COR/CRC, bit 15 of ER Register;

c) FMT/LRC, bit 7 of ER Register;

d) INC/VPE, bit 6 of ER Register;

e) FPAR, bit 5, ER Register;

Neither DRIVE CLEAR nor INIT affects this bit.

3.9.7 Bit 13 - FRAME COUNT LOADED (FCL)

This bit becomes set to '1' at the completion of a Massbus Control Bus write to the FC Register. It becomes reset when the FC Register is clocked from the all-1's state to the all-0's state. INIT and DRIVE CLEAR both cause this bit to become reset. Unless the IGNORE FRAME COUNT BIT is set, loading any SPACE, READ, or WRITE command with GO = 1 while FCL = 0 will cause NON-EXECUTABLE FUNCTION (NEF, bit 11 of ST Register) to become asserted and will cause command execution to be aborted. No tape motion will occur.

3.9.8 Bit 14 - IGNORE FRAME COUNT (IFC):

When asserted, this bit inhibits all checks on the FRAME COUNT Register and FCL bit, allowing execution of SPACE, READ, or WRITE operations to commence regardless of the status of the FC Register or the FCL bit.

When IFC is asserted, READ operations will not terminate until the TM02 detects the end of a record on tape. No check on record length will be made. READ operations which take place with IFC = 1 will not terminate with FCE = 1 unless the condition described in section 3.9.5 occurs. When IFC is asserted, READ or SPACE operations will still be terminated by FRAME COUNT overflow.

Neither DRIVE CLEAR nor INIT affects IFC.

3.9.9 Bit 15 - spare

3.10 CHECK CHARACTER REGISTER

3.10.1 CHECK CHARACTER DATA FIELD (CCDØ-8)

After the completion of a READ or WRITE operation, this field contains either:

a) In P.E. mode, the contents of the dead track register, or

b) In NRZ mode, the contents of the LRC character.

3.10.1.1 Dead Track Register Operation

Consider a tape on which data has been recorded on all nine tracks and which has itself been mounted on a tape transport. Assign track numbers to the various data tracks: let track 1 be the data track farthest from the tape transport chassis; let track 9 be the data track closest to the tape transport chassis. Tracks 2 through 8 are arranged in numerical order between tracks 1 and 9.

If, while reading a P.E. data record, the read circuitry examining track 1 detects either transient or total loss of signal, a '1' will be stored in bit Ø of the Dead Track Register. This '1' will be transferred (when the operation is complete) into CCDØ of the CC Register.

Similarly, a dropped bit or bits in Track 5 (the middle data track) will cause a '1' to be stored in CCD4 at the end of the operation.

The relationship between track numbers and the binary weight of a bit stored in that track is as follows:

TRACK NUMBER	BINARY WEIGHT
1	2^0
2	2^2
3	2^4
4	P
5	2^5
6	2^6
7	2^7
8	2^1
9	2^3

3.10.1.2 CRC Character Storage

At the end of an NRZ READ or WRITE operation, the CRC parity bit will be stored in CCD8. The least significant bit will be stored in CCDØ, most significant in CCD7.

3.10.1.3 CAUTION: The CHECK CHARACTER register will contain the check characters described above at the end of a READ or WRITE operation when DRY changes from Ø to 1. CCDØ-8 will be guaranteed true only as long as DRY remains equal to 1.

3.11 SERIAL NUMBER Register

3.11.1 BITS 0 to 3 - SNØ1, SNØ2, SNØ4, SNØ8:

Least significant digit of DEC Serial Number of selected slave (BCD).

3.11.2 BITS 4 to 15 - SN11 to SN18, SN21 to SN28, SN31 to SN38:

Next three digits of DEC Serial Number of selected slave (BCD).

TM02 REGISTERS*

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Φ0 CONTROL															
	-	-	DVA	-	-	-	-	-	F5	F4	F3	F2	F1	GO
Φ1 STATUS															
ATA	ERR	PIP	MSL	WRL	EOT	NTZ	DPR	LRY	SSC	PES	SDWN	IDB	FOF	BOT	SLA
Φ2 ERROR															
COR CRC	UNS	OPI	DTE	NEF	CS 1 FMT	FCE	BTE	PEF LRC	INC VPE	FDAT	FMT	PAR	RMR	ILR	ILF
Φ3 MAINT.															
MDF 8	MDF 7	MDF 6	MDF 5	MDF 4	MDF 3	MDF 2	MDF 1	MDF 0	SCK	MC	MDP 3	MDP 2	MDP 1	MDP 0	MM
Φ5 FR. CNT.															
FC 15	FC 14	FC 13	FC 12	FC 11	FC 10	FC 9	FC 8	FC 7	FC 6	FC 5	FC 4	FC 3	FC 2	FC 1	FC 0
Φ6 DRV TYP															
NSA	TAP	MSH	7CH	DRK	SPR	-	DT 8	DT 7	DT 6	DT 5	DT 4	DT 3	DT 2	DT 1	DT 0
Φ7 TAP CONT.															
-	IFC	FCL	EAO WE	INH FCF	DEN 2	DEN 1	DEN Φ	FMT SEL 3	FMT SEL 2	FMT SEL 1	FMT SEL Φ	EVEN PAR	SLAV SEL 2	SLAV SEL 1	SLAV SEL Φ
10 CHK CHAR															
-	-	-	-	-	-	-	CCD 8	CCD 7	CCD 6	CCD 5	CCD 4	CCD 3	CCD 2	CCD 1	CCD Φ
11 SER. NO.															
SN 38	SN 34	SN 32	SN 31	SN 28	SN 24	SN 22	SN 21	SN 18	SN 14	SN 12	SN 11	SN Φ8	SN Φ4	SN Φ2	SN Φ1

*ATTENTION SUMMARY REGISTER NOT SHOWN. SEE SECTION 3.6.

4.0 ATTENTION ACTIVE (ATA) and ATTENTION (ATTN)

ATA is displayed in bit 15 of the ST Register. ATTN is logically equal to ATA. (Consult Massbus Specification.) In the discussion following, ATA will be the mnemonic used.

4.1 ATA indicates that the TU16/TM02 requires servicing due to an error condition, has become ready after completion of a non-data transfer operation, or has detected an important internal status change. ATA will become asserted only if the TU16/TM02 system has DRY = 1. However, the condition ATA = 1 does not in itself prevent execution of commands.

4.1.1 ATA will be set if, while DRY is asserted, one of the following signals changes from the negated to the asserted state:

4.1.1.1 ERR

4.1.1.2 SSC

4.1.2 ATA will be set if at the time when DRY changes from the negated to the asserted state one of the following conditions is met:

4.1.2.1 ERR is in the asserted state.

4.1.2.2 SSC is in the asserted state.

4.1.2.3 Bits F1 to F5 in the CSI Register denote a SPACE, ERASE, WRITE FILEMARK, or REWIND command.

4.1.2.4 EOT is in the asserted state.

4.2 Clearing the ATA Bit

The ATA bit may be cleared by writing a "1" into its position in the Attention Summary Register. Parity is checked during the Control Bus transfer which controls the writing of the ATA bit, and if a parity error is detected, the ATA bit will be set at the completion of this transfer. The ATA bit will also be cleared by issuing a valid Drive Clear command, by asserting the INIT line, or by loading a GO bit into the Control I Register while ERR is negated.

The discussion below applies only to clearing the ATA bit by writing a "1" into it.

4.2.1 Clearing the ATA bit while ERR is asserted will result in negation of ATA but will not affect the status of the Error Register. No commands except Drive Clear can be executed until the Error Register is cleared.

4.2.2 Clearing the ATA bit when the Attention condition is caused by normal completion of a SPACE, REWIND, or WRITE FILEMARK operation will result in negation of ATA and will result in no other drive status changes.

4.2.3 Clearing the ATA bit when the Attention condition is caused by assertion SSC will result in negation of ATA. SSC will remain set, and unless it is cleared by DRIVE CLEAR or INIT, completion of the next command will cause ATA to become set.

Note that SSC can be generated by up to eight slaves in the TU16 Tape System and that its assertion may indicate status changes in several slaves including the selected slave. Thus while a Drive Clear Command will clear SLA in selected slave, unselected slaves could continue to assert SSC. Moreover, it an unselected slave caused SSC to be asserted because of a power failure, issuance of Drive Clear may (and INIT will) succeed in clearing SSC while leaving a broken slave on the Master-Slave Bus waiting to abort the next command issued it. BECAUSE OF THIS, SSC SHOULD NEVER BE CLEARED BEFORE ALL AVAILABLE SLAVES ARE POLLED AND THE STATUS OF EACH IS VERIFIED.

4.2.4 Clearing the ATA bit when the Attention condition is caused by assertion of DRY while EOT is asserted will result in negation of ATA and ATTN and will leave the drive ready to accept another command. Note that detection of EOT during tape motion will not generate an ATA and will not cause an abort. The EOT flag is a warning only, and it is the programmer's responsibility to go no more than 10 feet beyond the EOT marker.

5.0 Data Formats

This section deals both with the specific algorithms by which the TU16/TM02 system will map Massbus transfers onto tape during WRITE operations and with the algorithms by which tape characters will be mapped onto the Massbus Data lines during READ operations. Section 5.2 outlines a nomenclature for bits in PDP-10, PDP-11, and PDP-15 processor words, and indicates the expected location of these bits during a Massbus transfer. Section 5.2 also presents the data formatting algorithms which will be used on the TU16/TM02 system for PDP-10, -11, and -15 processor words. See Section 3.9.3 for further discussion of format codes and their implementation.

5.1 Handling of Massbus Transfers

Consider a single record which is to be written on tape. Four Massbus transfers will occur during the writing of this record. Assume for the sake of simplicity that all bits in every transfer will be deposited on tape. Allow the contents of transfer number 1 to be 111111_8, the contents of transfer number 2 to be 222222_8, of transfer 3 to be 333333_8, of transfer 4 to be 444444_8.

5.1.1 WRITE:

During a WRITE operation, the Massbus transfers will be mapped into tape characters according to one of the algorithms specified in Section 5.2. The algorithm used will be specified by the FORMAT CODE located in bits 4 to 7 of the TC Register.

5.1.2 READ:

During a READ operation, the procedure of Section 5.1.2 will be reversed, with tape characters mapped into Massbus transfers.

5.1.2.1 READ FORWARD:

During a READ FORWARD, four Massbus data transfers will occur. The contents of those transfers will be:

111111_8 - first transfer
222222_8 - second transfer
333333_8 - third transfer
444444_8 - fourth transfer

5.1.2.2 READ REVERSE:

During a READ REVERSE, four transfers would take place, but the order of transfer would be reversed, as follows:

444444_8 - first transfer
333333_8 - second transfer
222222_8 - third transfer
111111_8 - fourth transfer

IMPORTANT: The TM02 cannot maintain the orderly processing of data shown in Section 5.1.2.2 unless an integral number of processor words are transferred to tape.

Explanation: Define a constant, R, which is the number of tape characters required in a given format to make up one processor word.

For PDP-10 'Compatability' mode, R = 4; for PDP-10 'ASCII' mode, R = 5; for PDP-11 '9-TRACK' mode, R = 2, and so on.

If a record is to be written on tape which must later be read with a READ REVERSE command, then unless when the record is written the FC Register contains the two's compliment of R times the number of processor words to be transferred, the data flow illustrated in 5.1.2.2 will not be maintained.

5.2 DATA FORMATTING ALGORITHMS

5.2.1 Nomenclature

5.2.1.1 PDP-10 Core Word

5.2.1.1.1 B0 B35; B0 is MSB

5.2.1.1.2 Core-to-Massbus mapping is:

D17	D0	
B0	B17	1st Massbus Transfer*
B18	B35	2nd Massbus Transfer*

*In Read Reverse, order of Massbus Transfers are reversed.

5.2.1.2 PDP-15 Core Word

5.2.1.2.1 N0 - N17; N0 is MSB

5.2.1.2.2 Core-to-Massbus mapping is:

D17	D0
N0	N17

5.2.1.3 PDP-11 Core Word

5.2.1.3.1 R15 - R0; R15 is MSB

5.2.1.3.2 Core-to-Massbus mapping is:

D17 D16 D15	D0
R15	R0

PACK/UNPACK
MODES IMPLEMENTED

PDP-10

Mode 1: "10 Compatibility"

Tape Word Positions

Tape Frames	MSB								LSB
	TP	T7	T6	T5	T4	T3	T2	T1	T0
1	P	B0							B7
2	P	B8							B15
3	P	B16							B23
4	P	B24							B31

Mode 2: "10 Core Dump"

1	P	B0							B7
2	P	B8							B15
3	P	B16							B23
4	P	B24							B31
5	P	Ø	Ø	Ø	Ø	B32			B35

Mode 3: "10 ASCII"

Tape Frames	TP	T7	T6	T5	T4	T3	T2	T1	T0
1	P	~~0~~	B0						B6
2	P	~~0~~	B7						B13
3	P	~~0~~	B14						B20
4	P	~~0~~	B21						B27
5	P	B35	B28						B34

Mode 4: "10 Seven-Track"

	TP	T7	T6	T5	T4	T3	T2	T1	T0 (LSB)
1	P	-	=	B0					B5
2	P	-	=	B6					B11
3	P	-	=	B12					B17
4	P	-	=	B18					B23
5	P	-	=	B24					B29
6	P	-	=	B30					B35

PACK/UNPACK
MODES IMPLEMENTED
(cont.)

PDP-11

Mode 1: "11 Nine-Track:

Tape Frames	TP	T7	T6	T5	T4	T3	T2	T1	T0
1	P	R7							R0
2	P	R15							R8

Mode 2: "11 Seven-Track (Normal)"*

1	P	-	=	R5					R0
2	P	-	=	R13					R8

Mode 3: "11 Seven-Track (Core-Dump)"*

	P	-	=	Ø	Ø	R3			R0
	P	-	=	Ø	Ø	R7			R4
	P	-	=	Ø	Ø	R11			R8
	P	-	=	Ø	Ø	R15			R12

*If PDP-11 7-Track formats are used on 9-Track drives, the contents of the 2 high-order bits of the 9-Track tape frames are undefined (i.e., not necessarily 0).

PACK/UNPACK
MODES IMPLEMENTED
(cont.)

PDP-15

Mode 1: "15 9-Track"

	Tape Word Positions								LSB
Tape Frames	TP	T7	T6	T5	T4	T3	T2	T1	T0
1	P	N2							N9
2	P	N10							N17

Mode 2: "15 Core Dump"

1	P	Ø	Ø	N0					N5
2	P	Ø	Ø	N6					N11
3	P	Ø	Ø	N12					N17

6.0 TM02 Specifications

Maximum Transfer Rate (TM02 to slave) (tentative)	120 Kbytes/sec in PDP-10 7 TRACK FORMAT 240 Kbytes/sec - all other formats (See NOTE 1)
Maximum Transfer Rate (18-Bit Massbus Data Words)	Dependent on TM02 - slave transfer rate and format used.
Error Detection	See Section 3
Maximum Record Length	2^{17} bytes, PE or NRZ
Minimum Record Length	1 byte, PE; 3 bytes, NRZ
Write Lock	Dependent upon write lock signal from slave
Operating Environment	60° F to 95° F 20% to 80% RH, no condensation
Vibration	
Shock	
Power Requirements	D.C. - None A.C. - 90-135/180-270 VAC, 47-63 Hz
Installation	inch panel height 19 inch rack mount
Shipping Weight	pounds (uncrated)
Reliability (TM02 + slave)	Recoverable error rate: less than one recoverable error in 1×10^{8} bits read. A recoverable error is defined as an incorrect transfer of data from tape that occurs only once in four successive retries. Non recoverable error rate: less than one error in 1×10^{9} bits transferred.

(NOTE 1) Ability to mix PE slaves of different data rates on TM02 - slave bus requires further evaluation of PE read circuitry. Maximum transfer rates specified are design goals and have not yet been evaluated.

7.0 Interface Specification

7.1 Data Bus Signals

7.1.1 D⟨0:17⟩: Massbus data transfers are carried out using the D(DATA) lines. DPA: Data Parity bit. Odd Parity used.

7.1.2 RUN: Asserted by controller to indicate that a data transfer function is to be performed. If RUN is not negated within 1.5 microseconds after the drive asserts EBL, FRAME COUNT ERROR (FCE, bit 9 of ER Register) will be asserted.

7.1.3 END OF BLOCK (EBL): Asserted by the TM02 to indicate that data transmission has halted.

7.1.4 EXCEPTION (EXC): Asserted by drive to indicate presence of an error condition during data transfer.

7.1.5 SYNC CLOCK (SCLK): Asserted by drive to request new data from controller (WRITE) or to indicate readiness of new data from drive (READ).

7.1.6 WRITE CLOCK (WCLK): Asserted by controller during WRITE's to indicate readiness of new write data. Asserted in response to SCLK.

7.1.7 Occupied (OCC): Asserted by the drive to indicate that the drive has control of the DATA (D) lines. Sampled by the drive before seizing control of the D lines to determine availability of D lines. (See DTE, bit 12 of ER Register.)

7.2 CONTROL Bus

7.2.1 REGISTER SELECT (RS⟨0:4⟩): Asserted by controller to select drive registers. Drive register codes given in Section 3.

7.2.2 CONTROLLER TO DRIVE (CTOD): Asserted by controller to indicate direction of CONTROL Bus transfer.

7.2.3 DEMAND (DEM): Asserted by controller to initiate CONTROL Bus transfer.

7.2.4 TRANSFER (TRA): Asserted by TM02 to indicate that it is responding to CONTROL Bus transfer.

7.2.5 ATTENTION (ATTN): Asserted by TM02 to indicate abnormal condition or status change. See Section 5.

7.2.6 DRIVE SELECT (DS 0:2): Asserted by controller to select one of up to 8 Massbus drives.

7.2.7 INITIALIZE (INIT): Asserted by controller to return all drives to a known state.