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INTEROFFICE MEMORANDUM

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SUBJ: PDP-11/74 Multiprocessor System Evaluation

The attached 11/74 plan has been updated to encompass testing a multiprocessor based on modified PDP-11/70's. This plan encompasses verifying that the changes to the 11/70 do not affect its performance or software compatibility. This plan encompasses only testing involving approved MP peripherals. It also includes testing of the RH70-C Massbus adapter. This plan considers the fact that drafting will be using our machine during the evaluation. This plan will be submitted to document retrieval. A preliminary copy of this plan has been reviewed by 11/74 engineering.

Additional copies of this plan (DOC RET # RWC-79-004-00-U) may be obtained from Maddy Anastas, ML3-5/B39, extension 223-2339.

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Preliminary

11/74 Multiprocessor System Evaluation Plan

Version 4.1

COMPANY CONFIDENTIAL

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ML3-3/E67
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1.0 INTRODUCTION

This plan describes what will be done by Systems Evaluation Engineering for the 11/74 Multiprocessor. The 11/74 will be evaluated to determine the effects of the MP additions to the 11/70 processor. The 11/74 will be treated as a complete hardware/software system with its associated processors, memory, and peripherals. Primary emphasis will be given to the Dual CPU configuration. Special emphasis will be given to the Fault Tolerant Multi-processor System concept during the 11/74 evaluation. Both the hardware and software will be considered in this light.

1.1 Product Description

1.1.1 11/74 Processor

The 11/74 Processor will be an upward compatible processor to the 11/70. It will contain the necessary modifications for the addition of multiprocessor capability. The modifications affect the memory system, cache, memory management, unibus mapping, and power up actions. The 11/74 will have a new multiport memory system (MKA11). The 11/74 will also incorporate a large buffer Massbus adapter the RH70-C.

1.1.2 11/74 Multi-Processor System

The 11/74 is a Multiprocessor System consisting of 2 to 4 11/74 processors, multiprocessor peripherals (DT07, IIST, M9312-MP, RH01, etc.), and a new Multi-processor Operating System RSX-11M-PLUS. The 11/74 System will only support a specified subset of peripherals supported by the 11/70 (Table 1). The system is intended for markets which require enhanced availability, i.e. Fault Tolerance and/or extended performance above and beyond the 11/70 single processor.

The Multiprocessing System will have 2, 3 or 4 CPU's. Each processor will be connected to every memory box and a portion of the I/O devices, i.e. at least one memory box for each CPU on the System. Each CPU has at least one memory box and each CPU can access each memory box. All of the processors will be operated under a single-operating system RSX-11M-PLUS which provides for interaction between processors and I/O devices, fault detection, on-line diagnosis, and reconfiguration. The topology will be symetrical.

1.2 Evaluation Goals (reference section)

1.2.1 Verify that the 11/74 processor is upward compatible with the 11/70, identify any differences, and identify their consequences.(5.1.7)

1.2.2 Verify electrical characteristics of new multiprocessor peripherals (IIST, DT07, M9312).(7.0)

1.2.3 Verify by benchmarks that the 11/74 CPU performance is equal to or greater than the 11/70 processor.(13.1)

1.2.4 Verify that the 11/74 multiprocessing system does not violate any Unibus configuration rules.(5.1.11)

1.2.5 Verify proper power fail and bootstrap operation of the 11/74 multiprocessing system.(5.1.4,5.1.5)

1.2.6 Verify Subsystem Isolation via port switches (DT07, RH01).(5.1.12,6.1.7)

1.2.7 Determine any AC Power Consumption problems using the cabinet power analyzer. (2)(6.1.5)

1.2.8 Identify any cabling or mounting problems encountered with the 11/74 multiprocessor system.(5.1.10)

1.2.9 Identify serviceability problems encountered with 11/74 if any.(5.1.6)

1.2.10 Verify proper operation under fault free conditions of all diagnostics for 11/74 multiprocessor, RH01, DT07, IIST, M9312.(5.1.11)

1.2.11 Determine the effect of the loss of system components in the multiprocessor system by fault simulation.(5.1.13)

1.2.12 Verify port isolation in MP system via port switches and induced power failures.(6.1.7)

1.2.13 Verify that there are no crosstalk or reflection problems on the UNIBUS in MP systems.(7.1.5)

1.2.14 The PAULI(Programmed Analysis of Unibus Lengths and Interconnects) data base will be updated to include the 11/74 with its specific set of options.(5.1.11)

1.2.15 Collect DMT data in conjunction with DMT test plan.

1.3 Evaluation Non-Goals

1.3.1 Environmental Tests will not be done during this evaluation.

1.3.2 EMI/RFI testing will not be part of this evaluation.

1.3.3 230 VAC or 50 HZ power tests will not be conducted during this evaluation.

1.3.4 Fault Insertion for diagnostics and DEC/X11 will not be done during this evaluation.

1.3.5 Static Discharge susceptibility will not be done by Systems Evaluation.

2.0 EVALUATION OVERVIEW

A dual CPU 11/74 will be delivered to Systems Evaluation and installed between June 15th and July 6th. The dual CPU will be upgraded to a quad when the dual CPU testing is completed. About 3 to 4 weeks will be needed for this upgrade.

Refer to Appendix A for detailed break out of time required to complete each section.

2.1 Modified Processor Evaluation (11/74)

The 11/74 processor with its associated new parts (i.e. backplane, MKA11, and new cache modules) will be tested as a single processor system. It will be evaluated separately from the multiprocessor (multiple CPU) system. The processor will be connected to various devices in the CSL as indicated in appendix D, table 1.

2.2 New Software Evaluation

The new Executive RSX-11M-PLUS cannot be thoroughly evaluated until it is running in the dual processor system. Features which will be checked include operator interface, human engineering, sysgen improvements, new device support, loadable diagnostics(XXDP on FILES-11), and user mode diagnostics. The effectiveness of secondary bootstrap diagnsotics will be evaluated. (see sect. 10.2.2.1)

2.3 Operator Interface Evaluation

All operator interfaces (MKA11,DIP-11,DT07,CS-11 switch panels) including operator's guide (if available), and the associated human engineering factors can be evaluated as soon as the multiprocessor, RSX11-M-PLUS, and software operator's guides are available.

2.4 Compatibility Testing (11/74 vs 11/70)

The compatibility testing will be done in the CSL lab. Side by side tests will be made using the 11/70 and 11/74 processors. All software specified in Section 10 will be tried on the 11/74 and all 11/70-74 diagnostics will be tried on the 11/70.

2.5 Multiprocessing System Testing

Multiprocessing System testing will be conducted in two (2) phases to facilitiate hardware availability. Dual processor testing using a dual 1174D-DA will be done in the CSL lab. Quad CPU testing will commence after dual CPU testing is complete and the dual CPU has been converted to a quad. The only tests on the quad processor will be software including 11/74 diagnostics, memory diagnostics, DEC/X11MP, RSX-11M-PLUS, and Hardware Throughput Measurements.

2.6 Hardware Test Configuration

2.6.1 11/74 Multiprocessor (Dual CPUs)

The 11/74 dual processor will be evaluated in the CSL using all existing MP supported peripherals (as indicated in appendix D Table 1) for checkout. Electrical and Mechanical tests will be done only on the dual processor. All tested configurations will be documented.

2.6.2 11/74 Multiprocessor (Quad CPUs)

The quad 11/74 will be located in the CSL and will use MP supported dual ported peripherals. This configuration will be at least the minimum packaged system required for the multiprocessor system. (See Appendix C)

2.7 Relationship to other Products

2.7.1 DT07 Development

The DT07 Bus Switch is being designed at CSS as a replacement for the DT03. The advantage of the DT07 is that it provides port independency as well as port isolation. The DT07 is powered from the connected ports allowing devices to be powered down for repair. This is needed for on-line debug/fault isolation, power-fail/recovery, reconfiguration, etc. Without the DT07 the multiprocessor system will be delayed.

2.7.2 IIST Development

The IIST (Interprocessor Interrupt and Sanity Timer) is another multiprocessor peripheral. It is needed for multiprocessor systems. It is being developed at CSS. Without the IIST the multiprocessor Diagnostic and System software cannot run.

2.7.3 M9312 Development

The M9312 is the bootstrap module for the 11/74 system. It is used by the MKA11 to reboot on battery backup depletion. It is also used by the IIST (DIP-11-C) so one processor can boot another processor if it should go down. Without the M9312 Diagnostic and Bootstrap ROM reconfiguration will be impossible. It is also needed for the multiprocessing software to start-up additional processors.

2.7.4 RSX-11M-PLUS Development

This is the operating system planned for all multiprocessing systems. Without the RSX-11M-PLUS software it will be impossible to evaluate the multiprocessor system as a total system. The development of RSX-11M-PLUS is also the base for RSX-11M 3.X. RSX-11M-PLUS development is taking place in Tewksbury. They have only one prototype multiprocessor.

2.7.5 XXDP Development

XXDP will contain new diagnostics for the 11/74 multiprocessor peripherals and modified peripheral diagnostics to take into account multiprocessor hooks and port isolation features.

Delays in the development of XXDP diagnostics will hamper the debugging of multiprocessor peripherals, the 11/74 CPU, and delay the evaluation process.

2.7.6 MKA11 Multi-Port Memory Development

The MKA11 is the multi-port version of the MK11 memory for the 11/70. The MKA11 features MOS memory with up to four (4) ports, one for each CPU. It will be impossible to evaluate a multi-processing system without a multiport memory. The MKA11 is the only memory which will be supported by the 11/74 multi-processing system.

2.7.7 11/74 Performance Measurements

The performance group will be studying the 11/74 multi-processor from a performance point of view. Their results will provide needed information for Marketing, Software Development, and Systems Evaluation. Since improved performance through enchanced availability is a major goal, their results will enable Systems Evaluation to determine which areas need improvement if any.

2.7.8 RH70-C Development

The RH70-C is the same as the RH70 except for a one sector silo. It is needed to reduce data-lates with peak loads on the multi-port memory. Without the RH70-C additional performance measurement and software recovery would be necessary.

3.0 DEVICE PERFORMANCE INTEGRITY

3.1 Multi-processor 11/74 (Dual CPU)

3.1.1 Device Diagnostics

All CPU and MP supported peripheral diagnostics will be evaluated on a dual processor 11/74MP system. Diagnostics will be run in chain mode, stand-alone, and under spt. Fault insertion will not be performed. The ability of the XXDP diagnostic package to avoid affecting operations taking place in another part of the multi-processor system will be tested. XXDP diagnostics will also be tested with FILES-11 loading and with operating system assistance.

3.1.2 DEC/X11

DEC/X11 will be evaluated on a dual processor, 11/74 system with each of the 11/74 supported peripherals. DEC/X11 will be evaluated to determine its effect on other operations occurring in another part of the MP system. Data-late conditions will be determined using this configuration. The effects of the MKA11 memory system and the RH70-C Massbus adapter will be noted.

3.1.3 Extender Board Operation

To insure that the 11/74 can be operated in a troubleshooting environment applicable diagnostics and DEC/X11 will be run with each processor module placed on a multilayer extender board. Any problems will be noted or resolved.

3.1.4 Power Fail Recovery

The 11/74 will be powerfailed one unit (peripheral, CPU, memory) at a time while running .DEC/X11 and operating system software to verify proper powerfail recovery sequences of the 11/74, MKA11, and M9312. The length of time until failure (high temperature cutout, battery depletion, or smoke) will be determined. The AC/DC LO Monitor will be used to measure the AC/DC LO timing relationships.

3.1.5 Hardware Bootstrap

The 11/74 multi-processor will be tested with the M9312 diagnostic and bootstrap ROM. ROM's for all MP supported peripherals will be checked for proper operation. Proper operation under all conditions including MKA11 status will be verified; these include power fail, operator panel control and IIST.

3.1.6 Serviceability

The 11/74 will be evaluated from a serviceability point-of-view. Inputs will be obtained from Field Service. A Remote Diagnosis Console for the 11/74 will also be tested.

3.1.7 Compatibility Testing 11/70 vs 11/74

All 11/70 CPU and RH70 diagnostics and related DEC/X11 processor modules will be run on the 11/74 multiprocessor system. All diagnostics and DEC/X11 for the 11/74 CPU, supported peripherals and options will be run on the 11/70.

3.1.8 CPU Timing Margins

The 11/74 TIG will be margined using DEC/X11 while running a MASSBUS disk, a UNIBUS disk, the FPP module and the CPU module. Several relocations will be allowed to occur at each margin. The total range of the RC maintenance clock will be attempted. The range 140ns to 250ns is considered acceptable.

3.1.9 RH70-C Massbus Adapter

The RH70-C Massbus Adapter will be tested using RH70 diagnostics and DEC/X11 for the supported RH70 interfaced peripherals.

3.1.10 Multiprocessor Cabling and Mounting

A dual processor system and its H9500 series cabinet will be analyzed for cabling and mounting problems which may occur in assembly, installation, use, servicing, and shipping. Any obvious hot spots, cable problems, or restrictions will be noted or resolved.

3.1.11 Configuration Rules

Since the multi-processing system will be sold as packaged systems only, a limited number of dual and quad processor basic configurations will exist. These configurations will be analyzed to determine if any configuration rules have been violated; the PAULI program will be used to verify Unibus electrical configuration rules (AC loads, DC loads, cable lengths).

3.1.12 Multiport Support/Protection

XXDP and DEC/X11 will be evaluated to make sure that they do not effect operations occurring in other parts of the multi-processing system. For example, if RSX is running on one processor and a disk, and the 11/74 system exerciser (XXDP) is run on another processor it should not use the disk or memory associated with the other processor. All 11/70-74 diagnostics and DEC/X11 modes for devices approved for the 11/74 will be tested.

3.1.13 System Fault Insertion/Detection

Each system component of the dual CPU multi-processor system will be disconnected or powered down while other parts of the system are running. Any effect on the running system will be noted.

While the multi-processing operating system is running each system component will be powered down or disconnected to verify that they are correctly detected by the operating system. Bus and comm line switches will be thrown to verify that these actions are handled correctly by the operating system.

3.1.14 Operator Panel Considerations

The multi-processor control panels will be evaluated for complexity, ease of use, and human engineering. Any physical constraints or confusion will be noted. These include the CPU console, console terminal, MKA11 control panel, IIST (DIP 11-C boot) control panel, and power control panel.

3.2 Multi-processor 11/74 (Quad processors)

3.2.1 Device Diagnostics (11/74 only)

Processor and memory diagnostics will be run on the quad processor configuration to verify their operation.

3.2.2 DEC/X11 (for MP supported peripherals)

DEC/X11 will be run in the quad configuration to verify its operation on this configuration.

4.0 DEVICE ELECTRICAL INTEGRITY

4.1 Multi-processor 11/74 (Dual CPU only - includes RH70-C, IIST, DT07, M9312, UBE, RH01)

4.1.1 DC Power Supply Margining

The processor power supplies will be individually margined to the limits specified in the 11/74 engineering specification and beyond while running DEC/X11. Any failures will be noted.

4.1.2 AC Voltage Margining (see appendix A note 2)

The AC input voltage will be margined while running DEC/X11 with all processor options installed. Any failures will be noted.

4.1.3 DC Power Consumption

The 11/74 processor with all options installed will be measured to determine if any power supply limits are exceeded. Measurements will be made with and without DEC/X11 running.

4.1.4 Ground Isolation

Tests will be conducted to determine if logic reference can be isolated from chassis reference ground.

The potential difference between logic reference and chassis reference will be measured if possible to insure that no hazardous voltages are present.

4.1.5 AC Power Consumption (see appendix A note 2)

The system AC Power Consumption will be measured on a dual processor system package with all processor options installed. This will be done while running DEC/X11 or other suitable system exerciser. The total power consumption will be used to determine building power requirements, air conditioning requirements and uninterruptable power supply requirements. We will only collect the data during this test.

4.1.6 Subsystem Isolation

Each port or subsystem will be powered down and disconnected while the rest of the multiprocessing system is running. The purpose is to verify subsystem isolation required for maintenance. Diagnostics and DEC/X11 will be run to verify that there will be no interference to the remaining parts of the multiprocessor.

4.1.7 Port Isolation

Every multiport device will be powered down to verify that the port isolation switches work and do not affect processors attached to the isolated port.

4.1.8 Bus Switch Immunity

Equipment on the isolated side of Unibus switches will be powered down and disconnected. Any effect on the operation of the rest of the multiprocessor system will be noted.

5.0 UNIBUS/MEMORY BUS ELECTRICAL INTEGRITY

5.1 Modified Processor 11/74 (Dual Processor Configuration includes RH70-C, IIST, DT07, MKA11, RH01, M9312)

5.1.1 Time Domain Reflectometer (TDR)

TDR Measurements will be made on the 11/74 backplane with and without modules to determine if there are any excessive loading factors on the Unibus.

5.1.2 DC Loading

A schematic analysis will be made on all processor modules connected to the Unibus or Massbus to determine the gate loading factor and type for each signal line. This information will be used to determine the DC loading factor.

5.1.3 Timing Margins

Tests will be conducted to determine how much the 11/74 Unibus control degrades Unibus timing. Unibus timing relationships will be varied to determine the tolerance to the Unibus specification and operational limits. Small machine language test programs will be written for these tests.

5.1.4 Voltage Marginings

The 11/74 processor with all MP supported Unibus peripherals will be margined to verify that the Unibus is not degraded or system performance impaired by the 11/74 processor.

5.1.5 Crosstalk Measurements

Crosstalk measurements will be made on the Unibus using the single ended voltage margining technique. Measurements will be made while running DEC/X11.

5.1.6 Memory Bus Measurements

The 11/74 memory bus will be measured using the TDR system and a modified version of the "cable" program to determine its characteristic impedence and identify any reflective nodes. The memory bus will be voltage margined while running a predetermined memory pattern test using a special margin head and terminator supplied by 11/74 engineering. Crosstalk measurements will also be made using this special equipment.

6.0 HARDWARE THROUGHPUT MEASUREMENTS

6.1 Modified Processor 11/74 (RH70-C)

DEC/X11 will be used in a single CPU configuration with all multiprocessor supported peripherals to determine what configurations if any will produce data late conditions.

6.2 Multi-processor 11/74 (quad CPU)

DEC/X11MP will be used on the quad processor 11/74 system using only multi-processor supported peripherals. Any configurations which produce data lates will be noted. The exact configurations tested including DEC/X11MP parameters will be detailed in the final report.

6.3 Memory Sharing/Lockout Effects(see appendix A note 3)

The effects of memory contention and cache flushing on data lates will be determined. The cache flush feature has been optimized for RSX-11M-PLUS. For the exact details of this testing please see the Systems Performance Analysis Plan for the 11/74.

7.0 HARDWARE CONFIGURATIONS

7.1 11/74 Dual Processor

One dual processor 11/74 will be evaluated in the CSL using existing MP supported peripherals for comparison to the 11/70.

7.2 11/74 Quad Processor

One quad processor 11/74 with its associated multi-processor peripherals will be evaluated in the CSL using only MP supported peripherals.

8.0 SYSTEM SOFTWARE EVALUATION

8.1 Modified Processor 11/74 Software Compatibility

8.1.1 Software Utilities

8.1.1.1 XXDP package, ROLLIN (DOS), PRESERV (RSX-11S), DSC (RSX-11S), DEC/X11, SAVE/RESTORE (RSTS/E)

These utilities will be run on the 11/74 to verify that they operate the same as on an 11/70.

8.1.1.2 Operating System Software

Existing operating system software will be run to verify that the 11/74 operates in an 11/70 compatible form.

8.1.2.1 RSX-11M V3.2 (CSL IOX)
8.1.2.2 RSTS/E V7.0 (DEVTST)
8.1.2.3 RT11 V4 (I/O Test)
8.1.2.4 RSX-11M-PLUS (BL5)(CSL IOX)

8.2 Multi-processor 11/74 (includes IIST, M9312, RH70-C, and DT07)

8.2.1 Software Utilities

8.2.1.1 XXDP, DEC/X11, DSC, On-Line Diagnostics

8.2.2 Operating System Software

8.2.2.1 RSX-11M-PLUS

This is currently the only operating system designed for multi-processors. It will be tested in all phases on both dual and quad CPU hardware configurations. Features to be tested include the following:

Improved System Generation
Error Logging
Power Fail Recovery
UETP
Bad Block Handling
System Reconfiguration
New Device Support
System I/O Exerciser
User Mode Diagnostics
Software Bootstrap
(including secondary bootstrap diag.)
Applications Test Package
FORTRAN I/O Exerciser
User Interface - Terminal Service
System Reconfiguration

The exact system generated will be documented in the final report.

9.0 VERIFICATION OF PACKAGED SYSTEMS

All packaged systems in Appendix C for the 2, 3 and 4 CPU systems will be configured and verified to be operational. Feasibility will be determined by running the PAULI program if possible. The PAULI data base will be updated to include new 11/74 data. DEC/X11 and the RSX-11M I/O Exerciser will be run with all devices being exercised.

For the multi-processor system DEC/X11 and RSX-11M I/O Exerciser will be run on each possible single processor configuration and DEC/X11 will be run on at least the minimum system configuration. The package system in Appendix C represents minimum hardware configuration; additional hardware may be necessary to run operation system software.

10.0 INTRA BOX/CABINET CONFIGURATION

10.1 Dual CPU 11/74

The multi-processor will be evaluated to determine if the physical arrangement of options causes electrical or physical problems in the box or cabinet.

10.2 Multi-Processor 11/74 (Quad)

The quad CPU multi-processor system will be evaluated to determine if devices are affected by physical proximity. Tests will be made while running DEC/X11.

11.0 BENCHMARKS

Benchmarks will be conducted with the assistance of the Systems Performance Analysis group.

11.1 Processor 11/70 vs 11/74

11.1.1 RSX-11M V2.1 unmapped (KT11, Cache, Parity)

Benchmarks will be run on the 11/70 and 11/74 to compare instruction speed and performance. They will be FORTRAN IV PLUS benchmarks and they will be run using the FP11-C. These benchmarks will be run with and without the memory mux card.

11.1.2 RT11 (KT11, Cache, Parity)

Benchmarks will be run on the 11/70 and 11/74 to compare speed and performance. They will be in FORTRAN IV and will test: basic instruction, EIS, and FPP.

11.2 11/74 vs 11/70 (Conflicts and Arbitration)

Benchmarks will be run on all processors simultaneously to determine the effects of memory lockout, whether data lates occur, and if there are cache flush conflicts in the 11/74. This testing will be done with the assistance of the Systems Performance Analysis group. They will determine the benchmarks to be run and how they should be run.

12.0 ACOUSTICAL NOISE MEASUREMENTS

If the noise level produced by the 11/74 is noticeably greater than the 11/70, detailed noise level measurements will be instigated.

13.0 MULTI-PROCESSOR FAULT TOLERANCE

13.1 On-Line Diagnostics - User Mode

The On-Line User Mode diagnostics will be run and evaluated as to their effectiveness in a fault tolerant system.

13.2 Off-Line vs On-Line loadable XXDP

The On-Line RSX-11M-PLUS system will be used to load XXDP diagnostics into a non-running segment. An evaluation of this method vs off-line loaded diagnostics will be made.

13.3 Independent Processor/Peripheral Operation

The multi-processor system will be evaluated in a diagnostic or repair mode and in a multi-purpose user mode. In the diagnostic mode XXDP and DEC/X11 will be used while the remainder of the system uses RSX-11M-PLUS. In the multi-purpose user mode two different operating systems will be run on the same system simultaneously and any interactions noted.

13.4 Operator and Operator's Panel
The amount of operator ability and dexterity required will be determined on the multiprocessor system. The operator's panel will be evaluated for purpose, ease of use and functionality.

13.5 Error Logging

Error logging capabilities and resulting actions required by the operator will be evaluated for correctness, completeness and human engineering.

13.6 Trouble Shooting

The ability to perform troubleshooting on a subsystem while the remainder of the system is running will be evaluated.

4.0 MULTIPROCESSOR RECONFIGURATION (see appendix A note 4)

14.1 Manual

All manual controls such as bus switches will be evaluated for availability, operability, human engineering and operator documentation.

14.2 Software

Software Reconfiguration will be attempted on a Quad Processor Configuration. Any problems with ease of use, functionality, human engineering, documentation, or performance will be noted.

14.3 Reconfiguration Time

The amount of time required to reconfigure the multiprocessor after a failure, possible failure, or operator error will be determined using a highly trained operator. The purpose of this testing is to determine what kind of down-time the customer will experience after a fault and the amount of operator skill required. An attempt will be made to determine if this can be done within 15 minutes 90% of the time. Fault creation will not be done by the operator. A list of the faults created, the effects on the system, and the time to reconfigure will be included in the final report.

15.0 HUMAN ENGINEERING EVALUATION

15.1 Operator Skills/Requirements

The required operator skills will be evaluated to determine what degree of training is necessary.

15.2 Operator's Guide

This guide should allow the operator to quickly and easily isolate and identify faults, recover and reconfigure under software control, or perform a desired user request.

15.3 Reconfiguration Human Engineering

15.3.1 Hardware

Hardware reconfiguration controls and procedures will be evaluated for human engineering factors.

15.3.2 Software

Automatic Recovery under Software Control will be evaluated for human engineering, completeness, and minimization of operator intervention.

15.4 Field Service Operability/Feasibility

The major goal of the 11/74 is increased availability through multi-processing. This environment is new to Field Service. It should not effect their ability to perform their functions. The on-line loading of off-line processors and the operability of user-mode diagnostics will be evaluated from a Field Service point-of-view. Field Service flow charts will be used to determine their usefulness in resolving faults.

16.0 FINAL REPORT

A final report will be generated within one month after completion of the multiprocessor evaluation. A monthly status report will be written, and status reports will be given at bi-weekly status meetings.

Appendix A

PDP-11/74 Multiprocessor Time Schedule and Cost

Section	Description	Time (man-days)
3.0	DEVICE PERFORMANCE INTEGRITY ----------	55
3.1.1	Device Diagnostics	12
3.1.2	DEC/X11	5
3.1.3	Extender Board Operation	1
3.1.4	Power Fail Recovery	3
3.1.5	Hardware Bootstrap	3
3.1.6	Serviceability(1)	5
3.1.7	Compatability 11/70-11/74	5
3.1.8	CPU Timing Margins	1
3.1.9	RH70-C Massbus Adapter	2
3.1.10	Cabling and Mounting	1
3.1.11	Configuration Rules	2
3.1.12	Multiport Support/Protection	5
3.1.13	System Fault Insertion	5
3.1.14	Operator Panel Considerations	1
3.2.1	Device Diagnostics(quad cpu)	2
3.2.2	DEC/X11 (quad cpu)	2
4.0	DEVICE ELECTRICAL INTEGRITY ----------	12
4.1.1	D.C. Power Supply Marginins	1
4.1.2	A.C. Voltage Marginins (2)	1
4.1.3	D.C. Power Consumption	2
4.1.4	Ground Isolation	2
4.1.5	A.C. Power Consumption (2)	1
4.1.6	Subsystem Isolation	1
4.1.7	Port Isolation	1
4.1.8	Bus Switch Immunities	2
5.0	UNIBUS/MEMORY BUS ELECTRICAL INTEGRITY ------	32
5.1.1	Time Domain Reflectometer	15
5.1.2	D.C. Loading	2
5.1.3	Timing Margins	2
5.1.4	Voltage Margins	2
5.1.5	Crosstalk Measurements	1
5.1.6	Memory Bus Measurements	10
6.0	HARDWARE THROUGHPUT MEASUREMENTS (3) --------	25
6.1	Modified Processor 11/74	5
6.2	Multiprocessor 11/74(quad)	10
6.3	Memory Sharing/Lockout	10
8.0	SYSTEM SOFTWARE EVALUATION ----------	35
8.1.1	Software Utilities	1
8.1.2	Operating System Software	5
8.2.1	Software Utilities(MP)	4
8.2.2	Operating System Software(M+)	25

PDP-11/74MP Multiprocessor Time Schedule and Cost

Section	Description	Time (man-days)
9.0	VERIFICATION OF PACKAGED SYSTEMS ----------	5
10.0	INTER BOX/CABINET CONFIGURATION ----------	1
11.0	BENCHMARKS (3) ----------	5
12.0	NOISE MEASUREMENTS ----------	1
13.0	MULTIPROCESSOR FAULT TOLERANCE ----------	4
14.0	MULTIPROCESSOR RECONFIGURATION(4)----------	15
15.0	HUMAN FACTORS EVALUATION (no trainins) -------	5
16.0	FINAL REPORT (includes bi-weekly reports, -- dual cpu report,and quad conv.)	53

TOTAL COST $60K

TOTAL MAN-DAYS 248

(1) RD Console may be funded by field service
(2) May be done by DMT
(3) To be done in association with Performance Measurements
(4) The Field Service study will comprise the bulk of the fault insertion/system reconfiguration effort.

Appendix B:

PDP-11/74 Time Schedule (Milestones)

Dual CPU 11/74 arrives in CSL	15 June 1979
Dual CPU 11/74 tests complete	late August 1979
Dual CPU 11/74 conversion to Quad CPU starts	September 1979
Dual CPU 11/74 Report written	late Sept. 1979
Quad CPU 11/74 multiprocessor tests begin	October 1979
QUAD CPU 11/74 multiprocessor tests complete	late November 1979
Final Report issued	December 1979

NOTE: This time schedule is based on two(2) people from Systems Evaluation Engineering working full time on this project.

Appendix C: Packaged Systems

11/74 Multiprocessor(Dual CPU) Basic Test Configuration

1 X 1174D-DA	2 KB11-CM CPU 4 MKA11 dual-port memory 1MB each 2 DIP11-A (IIST), 2 H9602 (w/BA11-F and DD11-DF), 8 RH70-C
1 X LA36-HE	Console terminal (CSL)
1 X LA120	Console terminal (CSL)
1 X RP06-BA	Dual-port disk (CSL)
2 X RP05-BA	Dual-port disk (CSL)
2 X TM03/TWE16-AA	Mastape (1 CSL, 1 11/74 Eng. avail in Aus.)

Note

All of these packaged systems are absolute minimum configurations; most software requires more than these minimums.

All configurations tested will be documented, indicating position of devices on the Unibus, arbitration order(for RH70's), and cable lengths.

APPENDIX D

Table 1

Devices Approved for 11/74 Multi-processor Systems

RWP05/06	*BMS11
TWE16/TM03	CR11
DB11-A	CS11
DIP11-A	DT07
DH11-AA,AD,AE	*PC11
DL11 (all)	PCL11
LP11 (all)	LA36
RH01	VT52
DUP11	FP11-C
DMC11	RH70-C
DZ11 (EIA)	VT100
MKA11-BA	LA120

*Will not be tested during this evalution.

APPENDIX D

Table 2

Devices available in the CSL for test purposes

11/70 CPU	LP01	PC11/PC05
MJ11-A,B	RX11/RX01	M9312(boot)
FP11-C	RX211/RX02	TC11/TU56
TM03/TWE16	TU77	MK11
RWS04	LA36	TA11
RWP04/06	LA30	LT33
LP02	LA120	LP05
RK05J/F(2)	VT05	G5084 (apt interface)
KY11-R	VT52	DUP-11
KW11-P	RL11/RL01/RL02(2)	VT100
DH11	RK611/RK06/RK07(2)	DMC-11(2)
DJ11	KMC11	DL11(2)
DZ11	UBE (M7855)(4)	LP11

Note:

Unless specified only one of each device can be made available at any one time.

APPENDIX D

Table 3

Equipment needed for 11/74 Evaluation

11/74 dual and quad cpu's, FP11-C, DIP-11A, M9312, LA36, MKA11, and 4 RH70-Cs per CPU (74 Engineering).

RH01 Massbus Switch (74 Engineering)

CS11-MA Comm. Line Switch (74 Engineering)

DT07 Programmable Unibus Switch (CSS Supplied)

BMS11-L,-C Manual Bus Switch for line printer and card reader (CSS)

PCL11 Parallel Commnication Link (CSS)

TM03/TWE16 (74 Engineering)

H308 null modem (74 Engineering) (4)

H315 EIA turnaround (74 Engineering) (12)