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DATE: 15 August 1978
FROM: Hank Watkins HW
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EXT: 2577
LOC/MAIL STOP: TW/C18

SUBJ: PRELIMINARY 11/74 KB11-E DIFFERENCE SPECIFICATION

Attached please find a copy of the above specification for your information.

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DATE: 7 AUG 78
FROM: Ray Boucher
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SUBJ: PRELIMINARY KB11-B/E DIFFERENCE SPECIFICATION

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9.1 GENERAL

3.2 THE FOLLOWING IS A LIST OF KB11-E/CISP INTERFACE SIGNALS

CCRA	CISP PRESENT L
CCSA	ROM ADR<12:00> H
CCS	PERR 66 H
CCS	DIS TTRAP L
CCS	TRACK H
CCS	SET SUSP L
CCS	CLR SUSP L
CDI	CIS N BIT H
CDI	CIS Z BIT H
CDI	CIS V BIT H
CDI	CIS C BIT H
CDI	PAR ERR H
CDI	LOAD CC L
CDI	DALUB<07:00> H
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CDI	HGHNBL ZRO H
CDI	LOWNBL ZRO H
CDI	DALU<7:4> COUTB H
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DSCC	ADR<15:00> H
DSCA+B	ZERO DET H
DSCB	SIGN H
DSCB	OVERFLOW H
DSCB	CSAVE IN H
DSC	CIS ABORT L
DSCK	KBGRADD<02:00> H

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DSCL      PAR ERR H

DAPH      SHFR<15:00> H
GRAC      GRA<03:00> L
GRAC      GRWE LOB B L
GRAC      GRWE HIB B L

IRCH      Z (1) H

RACD      UADR<08:00> L
RACA      UIRK H
RACF      ENB CISMAF L
RACF      CIST H
RACF      TRACK L
RACK      ENB ADR (1) L

PDRA      BRMX<15:00> H
PDRH      DISP S2 H
PDRD      PS11 (1) H

TMCC      ABORT H
TMCB      BRQ TRUE L
TMCF      PS08 (1) H
TMCF      CLK PB H

UBCE      INIT L

TIGB      PB SYNCH H
TIGC      T1B H
TIGC      T1B L
TIGC      T2 H
TIGC      T2 L
TIGD      T3B H
TIGD      T3B L
TIGD      T4B H
TIGD      T5B L
TIGD      T5.5 H
TIGE      TS2 L
TIGE      TS3 L
TIGE      ENB DSCGRS H

MAPA      DATA<15:13>

BUS INTD<15:00> L
MAINTBUS<15:00> H
SRBUS<15:00> H
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3.3 The CISP/KE11-E(CIK) interface consists of 6 general categories: address, data, maintenance, suspendability, condition codes, and errors. All signals fall into one of these categories during the execution of CIS instructions.

The CIK interface has 2 major modes. One where KB11-E is master and CISP is slave, and two where CISP is master and KB11-E is slave. When KB11-E is master the CIS will track all KB11-E general register writes updating its own when necessary. When CISP is master, the KB11-E turns control of its ROM address over to CISP and waits for its next command from CISP.

The CISP/KB11-E interface has 3 main data paths: BRMX for data into CISP, BUS INTD for data out of CISP, and ADR for virtual address input to BAMX.

The CISP/KB11-E interface has 2 secondary data paths: SHFR primarily for tracking writes to KB11-E general registers, but can be used to get data from KB11-E to CISP, and SRBUS primarily for updating KB11-E GRs with 2901A GRs, but can be used to send bidirectional data between CISP and KB11-E. Since the SRBUS is input to BAMX, it can be used to supply virtual address to memory management from KB11-E or CISP.

The KB11-E generates GRA<03:00>, GRWE, and PS11 to write 2901A general registers at the same time as it writes its own general registers. This copy mode is referred to as IDLE, TRACK, or SHADOW. Likewise, if CISP is in control, it would use KBGRADD<02:00>, and the fact that it has complete control of KB11-E to update KB11-E GRs from CISP GRs.

In order for CISP to control the KB11-E, it must be able to address KB11-E ROM. It uses RACD UADR to address KB11-E ROM in much the same way it uses CCSA ROM ADR to address its own CISP ROM. CCSA ROM also goes to KB11-E for display and microbreak.

Gating signals like ENB CISMAF, CIST, TRACK, and ENB ADR allow CISP or KB11-E to obtain control of BUS INTD, ADR, or RACD UADR.

A part of the interface is used for maintenance and display. Part of the main data display of KB11-E is MAINTBUS which is also used as the microbreak data path. PDRA DISP S2 switches MAINTBUS from 2901A output to ROM ADR, FPP microaddress, KB11-E microaddress, or decimal ALU display (DALUB). Certain control signals such as 2901A N,Z,V,C bits and DALUB Z low nibble, Z high nibble,

carry out high, and carry out low are displayed in KB11-E to help maintain CISP. MAPA data and CLK PB are used to set CISP maintenance mode to executed 11/74 CISP maintenance instructions.

Since most CISP instructions can be interrupted before completion BRQ TRUE, PS08, SET SUSP, and CLR SUSP are used to keep suspended instruction status in the KB11-E PSW.

The CISP N,Z,V,C which are output from the M8167 FPLA along with LOADCC will update KB11-E condition codes to indicate CISP instruction completion status.

TMCC abort, CIS abort, PERR 66, PAR ERR, and INIT serve to reset display or flag error conditions in the CISP.

3.4 The following is a list and explaination of CISP to KB11-E interface signals per module.

M8165

CCRA CISP PRESENT L - indicates that a CISP option is present and enables execution of instructions with 076 opcodes.

M8166

CCSA ROM ADR<12:00> H - used to address 8K of CISP microcode. It is sent to the KB11-E for maintenance and display.

PDRA BRMX<15:00> H - used as the main data path from KB11-E to CISP such as during CISP DATI/DATIP cycles. It can also be used to cycle data within CISP such as DOR to DIR.

RACD UADR<03:00> L - part of the tristate address lines to address 1K of KB11-E control store. Used with CDI UADR 09 L, and RACD UADR<08:04>L on M8167 to allow the CISP to address the IK of KB11-E control store.

TMCC ABORT H - gated with TIGE TS2 L and used to initialize CISP to its IDLE, TRACK, or SHADOW mode.

UBCE INIT L - used to initialize CISP to its IDLE, TRACK, or SHADOW mode.

RACF ENB CISMAF L - used to enable the CISP side of the tristated address lines to address IK of KB11-E control store. It can only be generated if CISP is present and after an 076 opcode decode.

TMCB BRQ TRUE L - used to inform the CISP that an external and/or internal break request exists and requires service.

RACA UIRK H - used to inform the CISP on when to load DIR for instruction decode. The CISP ignores all except 076 opcodes.

TIGB PB SYNCH H - used to enable "CCS DIS TTRAP L."

CCS DISTTRAP L - used to prevent the KB11-E PSW trace trap bit from interrupting CISP instructions each time a break strobe is generated. The trace bit will be re-enabled when CISP returns to its IDLE, TRACK, or SHADOW mode.

TMCF PS08 (1) H - KB11-E PSW BIT 8. When set indicates a suspended (interrupted) CISP instruction. When clear indicates that there is no suspended instruction.

CCS SET SUSP L - used to direct set "TMCF PS08 (1) H" before exiting an interrupted CISP instruction.

CCS CLR SUSP L - used to direct clear (reset) "TMCF PS08 (1) H" after re-entering a suspended CISP instruction.

MAPA DATA<15:13> H - UNIBUS data bits <15:13> used to shadow the micro-break register (PB=17777770) into CISP to set maintenance mode and enable 11/74 maintenance instruction execution.

TMCF CLK PB H - used to clock "MAPA DATA <15:13>H" into a shadow register in CISP.

IRCH Z (1) H - the KB11-E Z condition code used to negate "CSS enable PCK L" (generated by a CISP PCK ORD) when the CISP micro-address goes to 0 during a maintenance microcode parity check. "CCS enable PCK L" returns the KB11-E to FET00 to fetch another instruction.

CSS PERR 66 H - indicates that a parity error occurred on the CISP microword contained on the M8166 module. It is sent to the KB11-E for display. Also used to generate "DSC CIS ABORT L."

CCS TRACK H - indicates that CISP is in the IDLE, TRACK, or SHADOW mode copying KB11-E general register writes into the respective 2901A general register.

TIGC T1B H, TIGC T2 H,
TIGD T3B H, TIGD T4B H,

TIGD T5BL, TIGD T5.5 H,
TIGE TS2L, TIGE TS3L - various timing pules and states used on the M8166.

M8167

BUS INTD<15:00> L - used as the main data path form CISP to KB11-E such as during CISP DATO/DATOB cycles. It can also be used to cycle data within CISP such as DOR to DIR.

CDI CIS N BIT H - the CISP N bit condition code sent to KB11-E to be loaded at the end of a CISP instruction.

CDI CIS Z BIT H - the CISP Z bit condition code sent to KB11-E to be loaded at the end of a CISP instruction.

CDI CIS V BIT H - the CISP V bit condition code sent to KB11-E to be loaded at the end of a CISP instruction.

CDI CIS C BIT H - The CISP C bit condition code sent to KB11-E to be loaded at the end of a CISP instruction.

CDI LOADCC L - used to load "CDI CIS N,Z,V,C bit H" into the KB11-E condition code latches at the end of a CISP instruction.

CDI DALUB<07:00> H - the output of the decimal ALU portion of CISP buffered and sent to KB11-E for display.

RACD UADR<08:04> L - part of the tristate address lines to address IK of KB11-E control store. Used with CDI UADR 09 L, and RACD UADR<03:00> L on M8166 to allow the CISP to address the IK of KB11-E control store.

CDI UADR 09 L - gated with "RACF ENB KBMAF L" and used with RACD UADR<08:00>L on M8166 and M8167 to address the 1K of KB11-E control store.

RACF ENB CISMAF L - used to enable the CISP side of the tristated address lines to address 1K of KB11-E control store. Also controls enabling the DOR onto the KB11-E "BUS INTD<15:00>L." It can only be generated if CISP is present and after an 076 opcode decode.

RACF TRACK L - it is "CSS TRACK H" inverted by KB11-E and sent to CISP to control enabling the DOR onto the KB11-E "BUS INTD<15:00>L." Used by KB11-E as a gating factor to assert "RACF ENB CISMAFL."

RACF CIST H - used to generate "GET OFF" in KB11-E for "BUS INTD <15:00>L", and to generate DATOB write

capability under CISP control in KB11-E. Also, used in CISP to control enabling the DOR onto the KB11-E "BUS INTD<15:00>L."

CDI PAR ERR H - indicates that a parity error occurred on the CISP microword bits contained on the M8167 module. Also, used to generate "DSC CIS ABORT L." It is sent to the KB11-E for display.

UBCE INIT L - used to reset various control flops and registers on M8167.

CDI HGNNBL ZRO H - indicates that the high nibble portion of the decimal ALU in CISP equals zero. It is sent to KB11-E for display.

CDI LOWNBL ZRO H - indicates that the low nibble portion of the decimal ALU in CISP equals zero. It is sent to KB11-E for display.

CDI DALU<7:4> COUTB H - indicates that there is a carry out of the high nibble portion of the decimal ALU in CISP. It is sent to KB11-E for display.

CDI DALU<3:0> COUTB H - indicates that there is a carry out of the low nibble portion of the decimal ALU in CISP. It is sent to KB11-E for display.

TIGC T2 H, TIGD T4B H,
TIGD T5B L, TIGD T5.5 H,
TIGE TS2 L - various timing pulses and states used on the M8167.

M8168

DAPH SHFR<15:00> H - used for copying KB11-E general register writes into CISP during IDLE, TRACK, or SHADOW MODE. IT is the main KB11-E data path sent to CISP specifically to track KB11-E GR writes. It can also be used as another KB11-E to CISP data path during CISP instruction execution.

DSCC ADR<15:00> H - is input to KB11-E "BAMX" as the CISP virtual address to memory management. This direct path to BAMX leaves the KB11-E free to compute using SR and DR during CISP data transfers.

SRBUS<15:00> H - a tristate bus connecting the KB11-E "SR" with CISP "ADR" to update KB11-E general registers at the end or during CISP instruction execution. It can also be used as another KB11-E to CISP or CISP to KB11-E general data path.

MAINTBUS<15:00> H - a tristate bus connecting the buffered CISP 2901A output with the KB11-E data display path. Used to display 2901A general registers in maintenance mode or general 2901A data.

DSCK KBGRADD<02:00> H - used to select KB11-E general registers under CISP control when KB11-E "PAD" field equals 3. It is generally used to update KB11-E GRs during or at end of CISP instruction or if CISP instruction has been interrupted.

GRAC GRA<03:00> L - used with "PDRD PS11 (1) H" to select 2901A general register during IDLE, TRACK, or SHADOW mode to copy KB11-E general register writes.

PDRD PS11 (1) H - KB11-E PSW bit 11 when set is used to select 2901A general registers 8 to 15. When clear is used to select 2901A general registers 0 to 7.

DSCL PAR ERR H - indicates that a parity error occurred on the CISP microword bits contained on the M8168 module. Also used to generate "DSC CIS ABORT L." It is sent to the KB11-E for display.

TIGE ENB DSCGRS H - sent to the M8168 as the maintenance time window for viewing 2901A general registers at the "DESCR" data display on the front console panel.

DSCA+B ZERO DET H - the "Z" bit directly out of the 2901A which is used for microword branching and sent to KB11-E for display.

DSCB SIGN H - the "N" bit directly out of the 2901A which is used for microword branching and is sentto KB11-E for display.

DSCB OVERFLOW H - the "V" bit directly out of the 2901A which is used for microword branching and is sent to KB11-E for display.

DSCB CSAVE IN H - the "C" bit directly out of the 2901A which is used for microword branching and is sent to KB11-E for display.

DSC CIS ABORT L - control signal sent to KB11-E which immediately cancels the CISP instruction and flags the fatal error in KB11-E CPU REG (17777766).

UBCE INIT L - used to reset various control flops and registers on M8168.

PDRH DISP S2 H - used to enable the 2901A output "DSBUS<15:00>H" onto the "MAINTBUS<15:00>H" for display at KB11-E.

RACF ENB ADR (1) L - used to enable the CISP "ADR" onto the "SRBUS" for updating KB11-E GRs or passing data from CISP to KB11-E.

GRAC GRWE LOB B L - a low byte write enable signal sent to CISP to control writing to 2901A general registers in IDLE, TRACK, or SHADOW mode.

GRAC GRWE HIB B L - a high byte write enable signal sent to CISP to control writing to 2901A general registers in IDLE, TRACK, or SHADOW mode.

TIGC T1B H, TIGC T1B L,
TIGC T2 L, TIGD T3B L,
TIGD T5B L, TIGD T5.5 H - various timing pulses used on the M8168 module.

3.5 The following is list of general hardware changes. To explain the changes more easily, they are grouped into 12 different categories: ROM and ROM Control, GR and GR Control, BUS INTD, BRMX, SR and SR Control, Condition Codes, Suspendability, Timing, Errors, Maintenance, Miscellaneous, and Enhancements.

The KB11-E ROM is 1K by 84 bits (a change from 256 by 84 bits). The KB11-E was modified to address 512 by 84 bits, and the CIS can address all 1K by 84 bits. The UFEN field was redesigned to obtain the extra bit for KB11 ROM address. The UAD field was tristated with KBPTR field in CIS to allow either KB11-E or CIS to address KB11-E ROM. Control logic was added to decide whether KB11-E or CISP is master of tristated UAD field.

An additional MUX was added to allow CIS to address KB11-E general registers (KGR) with a redesigned UPAD field of 3. The KB11-E GR address was buffered and used to address CIS general registers (CGR). The KB11-E write enable lines were buffered and sent to CIS to be used in track mode.

The GET OFF logic was redesigned to guarantee no overlap of the CIS decimal ALU tristate driver on the INTD BUS, and any other open collector driver on the INTD BUS. The UBSC field decode of 4 was changed from selecting FP11 "C" lines to FP11 "C" lines or CIS DATOB when CIS is in control doing a DATOB transfer over INTD BUS to memory.

The BRMX steering logic was redesigned to select BUS INTD for CIS writes to memory and to CACHE/UNIBUS for CIS

reads from memory. Obviously, it cannot select both read and write so, WRITE BUST/WRITE PAUSE followed by READ BUST/READ PAUSE must and can load BR/BRA at T1 of PAUSE.

The KB11 SR was tristated with CIS to create the SRBUS selecting the CIS as master with a USRX field decode of 3. All other USRX decodes will select SR.

The logic which controls loading condition codes was modified to gate another input to KB11 N,Z,V, and C bits. The continuous clocking of KB11 CCs is disabled while CIS is in control of KB11-E. A separate load CC code will gate CIS condition codes into KB11-E at the end of a CIS instruction.

A suspendability bit was added to the KB11 PSW. Bit 8 of PSW will indicate a suspended CIS instruction which is gated onto the UNIBUS and INTD Bus in the same manner that the rest of the PSW is gated to those buses.

A new time pulse T5.5H was added by deleting the unused T4L. The MEMSYNC/CLK BR logic was redesigned to add flop T5.5 (1) H to the timing ring counter. As a result of timing module changes, the TPB H and TPB L pulses had to be rerouted and terminated.

The abort logic was redesigned to include CIS abort signal, and an additional input to the ZAP logic was needed to abort KB11-E on CIS microword parity error. The odd address check logic was modified to enable odd address check (if desired) during CIS instruction execution. The CPU error register was increased by 2 bits to flag CIS abort error conditions.

The KB11 data display was increased from 4 data paths to 8 data paths. An additional cable conductor from the console was needed to display 3 CIS data paths, an increased KB11 ROM address, and 4 other KB11 existing data paths. The PB register was extended from 8 to 16 bits (a 13 bit portion to compare a ROM address and stop, and a 3 bit CIS maintenance portion). The data display MUX was increased to gate the additional 8 bits to the UNIBUS for display. The PB CMP logic was redesigned to provide the same detection speed for the increased register length. To control the additional display MUX, the PB, SL, PS and PIR encodes were redesigned. Some new logic was added to delay T2 pause restart and to generate a display time window for looking at CGRs in maintenance mode. The logic to display the KB11 state during pause was moified to simplify timing and bus condition interpretation.

Because of the structure of CIS instructions added to the PDP-11 basis architecture, some modifications were

necessary to handle CIS instructions. The condition BUST logic was inhibited during CIS instruction decode. The ability to disable T bit trapping during CIS was added. Logic was added to disable halt switch enable detection until CIS instruction execution has ended. Logic was added to enable ODD address detection during a CIS instruction (otherwise it is always disabled).

Several changes were made to increase reliability, availability of parts, maintainability, or to enhance KB11-E features. Several parts changes were made such as "H" series to "LS" or "S" as applicable. Some multiprocessor hooks were added. The timing module time states were redesigned to eliminate possible reflection interference. Additional console to KB11-E cable grounds were added. All +5V runs from KB11-E to console have fuses. Some UNIBUS drivers and receivers were placed near module fingers to reduce AC loading.

A new QUAD module M8169 was added to the CPU. The M8169 is a maintenance and data display module (MDC). Since aditional fingers were not available on the M8174 to display CIS data paths, it was necessary to remove one 16 bit data path from M8174, MUX CIS data paths with the one removed and send the result back to the M8174. The M8169 also serves to latch the CIS ROM address for display, terminate CIS timing pulses not used when CIS is not installed, and generate a CIS parity error.

3.6 The following is a list of hardware changes on a mosule basis. For further details see the KB11-E customer print set. The TIG signals were rerouted on all modules changed to minimize SKEW.

CONSOLE - The 5413474 console now contains 5 separate grounds and 4 separate +5V sources. It is important that they remain separate to minimize ground loops, remote logic interference and crosstalk induced by switch rotation. See D-CS-5413474 for +5V and ground distribution. The address and data display switch led indicators were deleted and replaced by marks on the logo panel to indicate displayed data path. Another 9318 chip was added to change the data display from 4 paths to 8 paths. The lamp test signal was brought out to M8180 over console J2 to do a lamp test on the maintenance W131 module.

M8169 - The "RACD RAR" and "FRMB RARB" input to M8174 was deleted and replaced with a tristated MUX output from M8169 and SM8168. The M8169 MUX is a 16 bit wide MUX made up of 74S253 chips. The 4 inputs to the 74S253 are "RACD RAR", "FRMB RARB", CIS ROM address, CIS decimal ALU data display, and various control bits scattered around unused bit locations. The MDC module also contains logic

and IC lamp drivers for the W131 module used to display time pulses as they appear on the backplane. The M8169 also contains various registor and diodes to preheat W131 lamps and test W131 lamps by illuminating all at one time.

M8170 - Name change only.

M8171 - Added 2 74S157 muxes to enable CIS to address KB11-E general registers. Also added combinational logic to decode UPAD field of 3 to control that MUX. The write enable signals were buffered and brought to module fingers for CIS to use in tracking KB11-E GR writes. The 3 74S174 SR chips were deleted and replaced by 4 2918 tristate chips to create a tristate bus between CIS and KB11-E called SRBUS.

M8172 - Added the decode of ASRB for multi-processor hooks. Replaced 8251-1 decoders to 74S138 for higher parts availability. Deleted 2 74H50 chips to direct set KB11 condition codes and added 4 74S64 chips in order to gate CIS CCs as another input. Redesigned the 74S64 direct clear inputs to KB11 COND codes in order to gate CIS as another input. Added some combinational logic to use the CIS load CC signal to gate CIS COND cones into KB11-E and to use CIST to inhibit unwanted KB11 COND code clock pulses during CIS instruction execution.

M8173 - Changed 17 256 by 4 ROMS to 17 1K by 4 ROMS which increased KB11 control store by a factor of 4. Redesigned UFEN field decode to obtain extra UAD field bit needed for KB11 to address 512 locations of its 1K control store. Tristated UAD field (9 bits) using 74LS240 with CIS KBPTR field to transfer master control of KB11-E control store between CIS and KB11-E. Added a 74S74 and combinational logic to control whether KB11-E or CIS is master of KB11-E control store. Added a 74S64 to insure "RACH BUST" is not asserted in KB11-E during a conditional bust decode of CIS instructions. Added combinational logic to decode USRX field of 3 to enable CIS ADR and disable KB11-E SR from SRBUS. Added 74S64 and comb logic to allow KB11 to address 512 instead of only 256 control store locations using the extra ROM bit obtained by redesigning UFEN field. Added comb logic to allow CIS to address 1K of KB11-E control store. Redesigned ZAP logic to allow CIS abort to JAM KB11-E ROM address to 200. Added logic to use UAD ROM bit 08 to enable odd addressing check in KB11-E during CIS instruction execution.

M8174 - Added 2 74S157 MUXES and COMB logic to display upper byte of PB register (all 8 bits added) or SL register. Deleted 2 7485 chips and added 3 74S85 chips plus COMB logic to do a PBR compare on 13 bits instead of

8 bits. The 74S85 chips are needed to meet PB comapre requirements on the CIS ROM address. Added COMB logic to gate new PSW bit 08 to the UNIBUS and INTD BUS. Added one 74S02 to control the display of 8 data paths instead of 4 data paths. The 74S02 is needed to drive 10 SCHOTTKY loads. The RACD RAR/FRMB RARB input to the display MUX is changed to MAINTBUS (a documentation change on the M8174). Added additional grounds to console cable connector. Added a fuse on +5V conductor to console. Added one additional data display switch conductor to console cable for 8 data path COMB control logic. Changed 74H01 INTD BUS drivers to 74S03 (parts list change only). Moved UNIBUS drivers and receivers closer to module fingers to reduce AC loading.

M8175 - Redesigned ODD address detection logic to disable ODD address error during CIS instruction unless KBRADR08 is true. Minor change to kernal R6 logic to do a stack limit check during a JSR if GR set 1 is selected (a KB11-C fix). Used other input to 74S11 to disable T bit trading during CIS instruction execution. Added 2 bits to CPU ERR REG 17777766 (bit 01 = CIS ABORT, BIT00 UNUSED). Changed CLK LR gating from TS5 to TS4 for reliability. Redesigned PB, SL, PS, and PIR address encoding to accomodate extended PB REG clocking and display. Used other 74S11 input to CLK CONF signal to disable halt switch enable detection during CIS instruction execution (used track H to module finger with 1K pull up). Added some COMB logic to UBSC field decode of 4 to generate a DATOB under CIS control or FP11-C control lines under KB11-E control. Redesigned BRMX steering with COMB logic to select BUS INTD during CIS write and UNIBUS/CACHE during CIS read. Added COMB logic to guarantee all drivers are off BUS INTD (GET OFF signal) before CIS takes control. Added flop to store PSW bit08 and COMB logic to direct set, direct clear, and clock BR08 data. Removed ability to clock PB REG low byte and high byte (M8174 finger limitation, always clocks word). Changed "H" series parts to "LS" or "S" series (parts list change only).

M8176 - MP changes only. See section 9.

M8177 - MP changes only. See section 9.

M8178 - Increased ROM from 256 by 16 bits to 1K by 16 bits. Added 2 ROM address lines to address the 1K of memory management ROM locations. Deleted ROM output resistors (parts list change only). Redesigned GET OFF logic using COMB logic to increase speed of disable to drivers.

M8179 - Added new time pulse T5.5 H (goes high between T5 and T1) by deleting unused T4 L. Redesigned MEMSYNC

RECEIVE/CLK BR logic to add T5.5 (1) H flop to timing ring counter (deleted 4 chips added 2.5 different chips). Redesigned time states to prevent reflections from interfering with the time states latched condition. Added 74S74 to delay T2 pause restart for 60NS to provide 2901A GR display window. Rerouted and terminated TPB L and TPB H because of added logic changes (TPB H has 2 terms PULL UP/PULL DOWN, and TPB L has 3 terms PULL UP/PULL DOWN). Added COMB logic (1.5 chips) to generate a display window to look at 2901A GRs in maintenance mode. Redesigned PB CMP logic to speed up decode for PB REG expansion (delete 1 chip and add 1 different chip). Changed TX MAT signal to the A version flop (move 1K from one flop output to another), and buffered stop T1 and stop T3 with 1K to module finger to simplify CPU state condition on W131 maintenance module. Removed 6.8 microfarad caps from S1 and S2 debounce circuit to minimize spurious step pulses from moving ground on W131 maintenance module (parts list change only).

M8180 - Redesigned 8234/74S05 BUS INTD drivers to speed up GET OFF logic (8234 has 16MA limitation changed to 74S157 and 74S05 to 74S03). Added 2 bits to 74S157 spare inputs for 2 new CPU error REG bits. Brought console lamp test from J1 connector to backplane to do a W131 lamp test (750 MA return MAX). Added fuse to J1 +5V source and J2 +5V source. Added additional ground returns to both J1 and J2 console connectors.

M8181 - MP change only. See section 9.

M8182 - MP change only. See section 9.

M8183 - MP change only. See section 9.

M8184 - Name change only.

M8185 - Name change only.