PDP-K Technical Memorandum # __9__

Title: PDP-K Initial Cost Considerations

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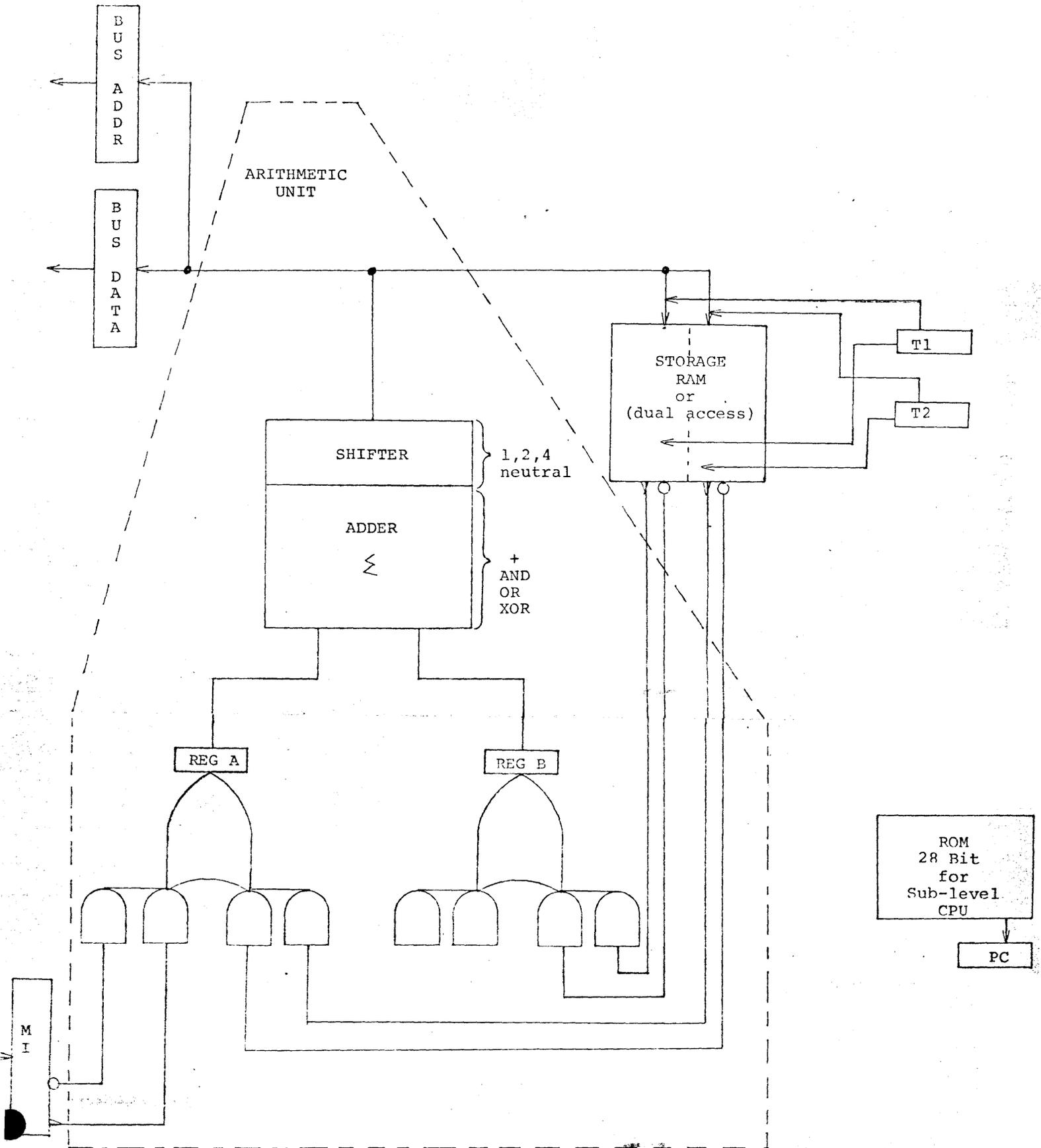Revision: None

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1.0 Introduction

This memo outlines the initial considerations made in
determining the manufacturing cost of the PDP-K com-
puter. The main interests at this time were directed
toward what hardware would be used, in generating a
general flow of processor elements. In the PDP-K
meeting to come, the actual cost figures for manufacture
will be estimated.

BUS ADDR

BUS DATA

ARITHMETIC UNIT

STORAGE RAM or (dual access)

T1

T2

SHIFTER

1,2,4 neutral

ADDER

$\lessgtr$

+ AND OR XOR

REG A

REG B

ROM 28 Bit for Sub-level CPU

PC

M I

FLOW DIAGRAM
Figure 1

2.0 Initial Considerations

Since determination of cost was the initial objective at this meeting, a number of questions were raised as to how the processor elements should be implemented. The prime concern was the economics involved in integrating these elements.

It was noted that in the low level component area that high-speed TTL technology should be used wherever possible since a cost reduction of 43% for IC's was realized in the 69/70 calendar. This would mean that today DEC is paying about 48¢ per guard gate, and by 1972, DEC would be paying approximately 30¢ for the same elements. With this condition present, then this alone would steer us away from any extensive use of the ECL technologies for this computer.

The assumption was made that the PDP-K could be a microprogrammable machine. Using this as a basis, a basic processor flow was generated, and attention given to the use of a ROM and RAM memory as an integral part of the processor. Being a microprogrammable machine, the need for a small sub-level processor with the main processor was obvious. This sub-level processor would contain its own ROM and PC and would operate on the main processor. As seen in Figure 1, the CP elements were laid out with the arithmetic unit in the center. In considering the arithmetic unit, in order to up the efficiency of the entire CPU, it was found that information should be presented to Reg A and Reg B simultaneously. To achieve this function, it was necessary to add a "Dual Access Register" or RAM type memory in the processor loop. This redundant storage would consist of up to 64 words.

Microprogram Format

A general format was considered to get a feel for the usefulness of using a ROM. As a basis for this format, the Source-Destination technique of the PDP-11 was used.

In the PDP-K case, the ROM word was partitioned in the following manner:
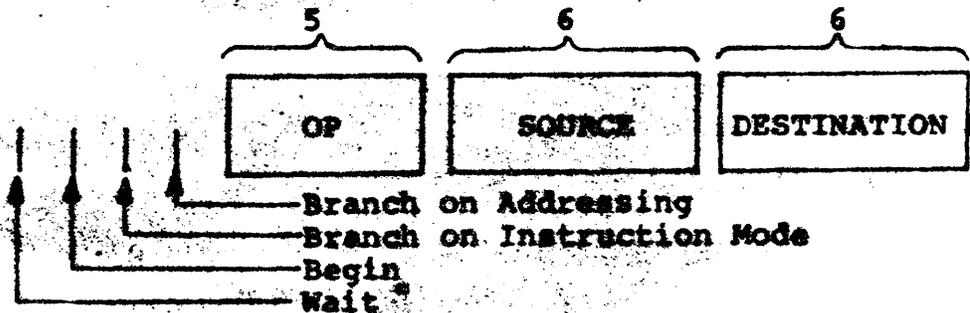
The capacity of the ROM was estimated to have approximately 640 locations. This was derived from a Source-Destination Address Computation in which the average turned out to have a value of 10. This is actually best guess. The ROM word would modify the opcode which consists of ADD, AND, OR, XOR; the subtract function could be achieved by an inversion at the input to either Reg A or Reg B.

Register to Register Transfer Execution

The next item that was considered was the amount of time it took to do a register to register transfer. The first assumption was that core memory would take 500 nsec maximum to be accessed, and that a full processor cycle could take 100 nsec using today's technology.

The subroutine calculation for a register to register transfer is as follows:

```
A+B→B

(PC)→(MA)
READ→MEMORY
(PC)+1 (MA)
WAIT FOR READ
BRANCH ON SOURCE AND DESTINATION INSTRUCTION (64 ways
BR=      MOV     SF to T1
         MOV     DF to T2
         BR      INSTR
ADD I (T1), I(T2)        where I means indirect
```
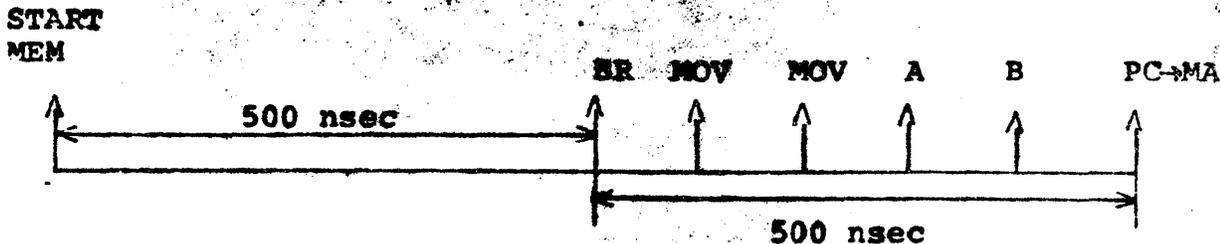
Timing realized from the above subroutine is as follows:

START
MEM
                                    BR MOV   MOV   A   B   PC→MA

         |←——— 500 nsec ———→| ↑   ↑   ↑   ↑   ↑   ↑

                                    |←————— 500 nsec —————→|

For this subroutine it took four Source-Destination instructions and required approximately 1.0 usec to perform the A+B→B transfer. A more time-consuming computation would be a Memory Register to Destination Register transfer. The subroutine computation to accomplish this is as follows:

```
              (PC)→(MA)
              READ→MEMORY
              (PC)+1→PC
              WAIT FOR READ
              BR ON SOURCE AND DESTINATION INSTRUCTION


MR→           (PC)→(MA)  ⎫
              READ       ⎬     SOURCE SECTOR
              (PC)+1→PC  ⎭


              DR→T2   ———————     DESTINATION SECTOR
              K→T1
              WAIT
              (MR)→(MA)→MA
              READ
              WAIT FOR READ
              BR ON INSTRUCTION
              ADD T1
              BEGIN
```

Assuming again 800 nsec for a full R/W core memory cycle, and Read Access being at 500 nsec, then 900 nsec of this subroutine is CPU execution time while 1.6 usec belongs to the core memory itself. Thus, total of 2.5 usec for a 6 instruction transfer.

A curve of processor execution time versus core memory speed could now be generated for a Memory Register to Destination Register transfer.
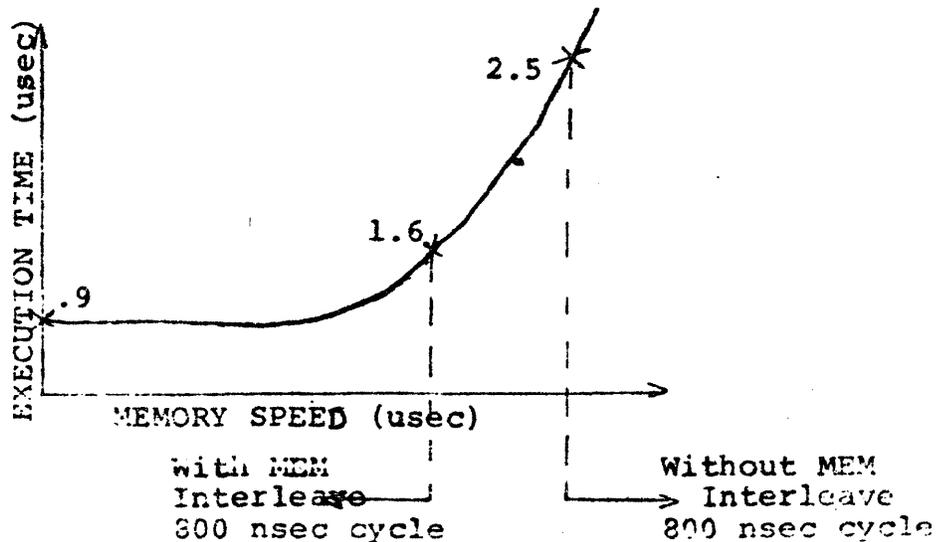
From these initial considerations, it can be seen that
a ROM memory does form an integral part of this system,
and that a RAM also could be utilized.

Actual manufacturing costs will be established at the
next meeting held on PDP-K. Under consideration at
this next meeting will be the estimated cost of the
following:

ROM
RAM
Arithmetic Unit
ROM Control
RAM Control
Bus Control
Console
I/O Control
Power Supply
Cabinet