

**digital**

**KL8-J**

**Engineering Drawings**

**Digital Equipment Corporation**

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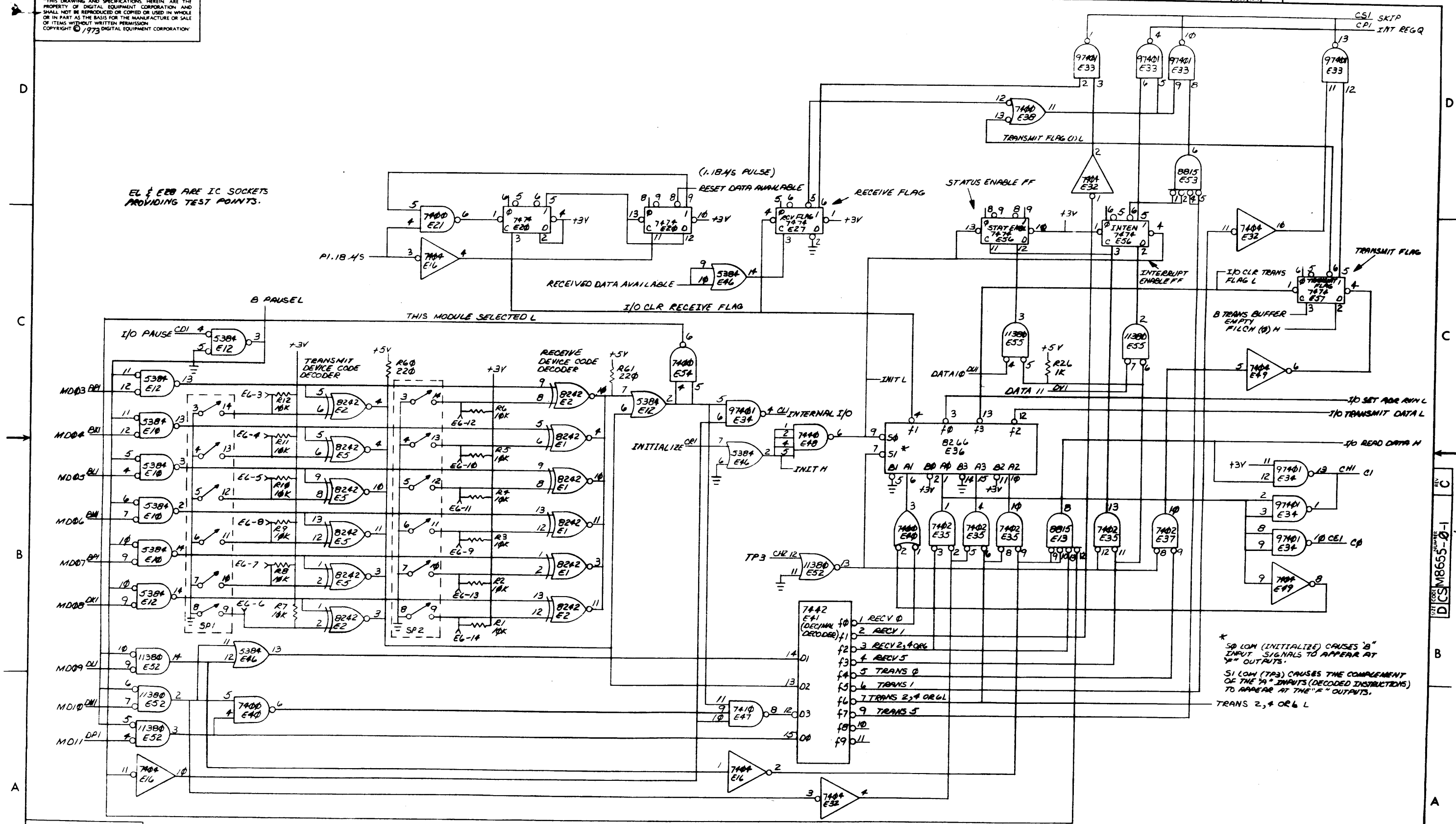
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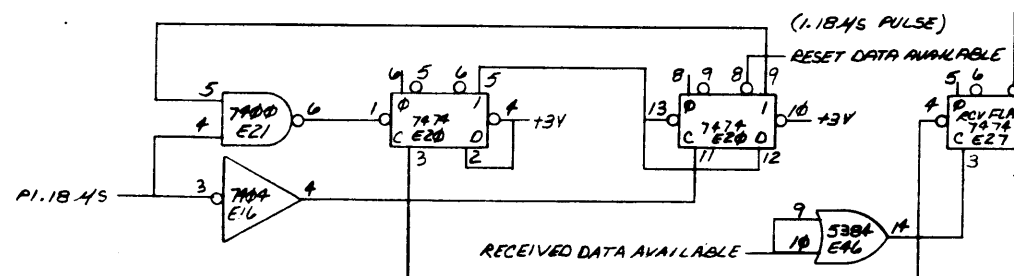




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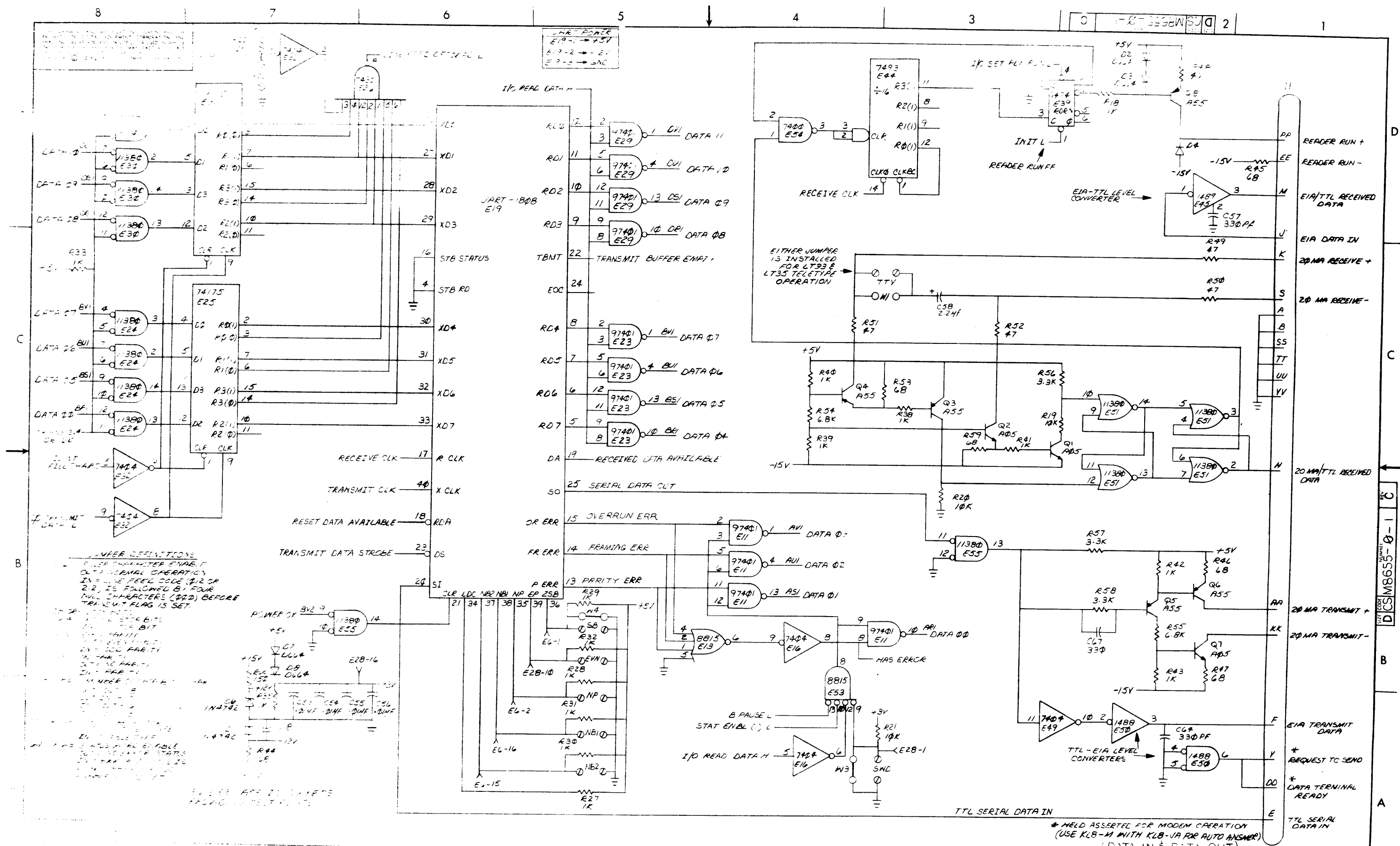


\* S0 LOW (INITIALIZE) CAUSES "B" INPUT SIGNALS TO APPEAR AT "A" OUTPUTS.  
S1 LOW (TP3) CAUSES THE COMPLEMENT OF THE "A" INPUTS (DECODED INSTRUCTIONS) TO APPEAR AT THE "F" OUTPUTS.

REVISIONS		
CHK	CHANGE NO	REV

(INSTRUCTION DECODING & FLAGS)			
TITLE	SIZE CODE	NUMBER	REV.
TERMINAL CONTROL	D	CSM8655-0-1	C
SCALE	SHEET 2	OF 5	DIST.





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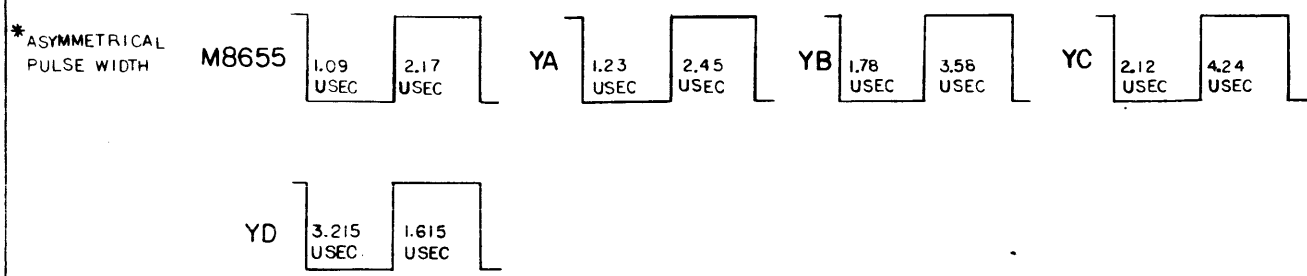
M8655 VARIATION TRANSLATION TABLE

PULSE NAME TRANSLATION TABLE

	M8655 OSCL 5.0688MHz. DEC #18-11660-02 CLK PULSE WD/BAUD RATE	M8655-YA OSCL 4.435 MHz. DEC #18-11660-11 CLK PULSE WD/BAUD RATE	M8655-YB OSCL 3.0737 MHz. DEC #18-11660-09 CLK PULSE WD/BAUD RATE	M8655-YC OSCL 2.619 MHz. DEC #18-11660-08 CLK PULSE WD/BAUD RATE
B1 B2 B3				
OFF OFF OFF	284 USEC/110	326 USEC/N/A	466 USEC/66.7	535 USEC/56.8
OFF OFF ON	208 USEC/150	238 USEC/N/A	343 USEC/N/A	402 USEC/N/A
OFF ON OFF	104 USEC/300	119 USEC/N/A	171 USEC/N/A	201 USEC/N/A
OFF ON ON	52 USEC/600	59.6 USEC/N/A	86 USEC/N/A	100 USEC/N/A
ON OFF OFF	26 USEC/1200	29.8 USEC/N/A	43 USEC/N/A	50.5 USEC/N/A
ON OFF ON	13 USEC/2400	14.9 USEC/N/A	21.4 USEC/N/A	25.1 USEC/N/A
ON ON OFF	6.5 USEC/4800	7.45 USEC/N/A	10.7 USEC/N/A	12.6 USEC/N/A
ON ON ON	3.26 USEC/9600	3.62 USEC/N/A	5.37 USEC/N/A	6.35 USEC/N/A
ON ON CN	1.63 USEC/19.2 KBD*	1.87 USEC/N/A*	2.69 USEC/N/A*	3.17 USEC/N/A*
	M8655-YD OSCL 3.419 MHz DEC #18-11660-10 CLK PULSE WD/BAUD RATE			
OFF OFF OFF	421 USEC/74.2			
OFF OFF ON	408 USEC/NA			
OFF ON OFF	154 USEC/NA			
OFF ON ON	77 USEC/NA			
ON OFF OFF	38 USEC/NA			
ON OFF ON	19 USEC/NA			
ON ON OFF	9.6 USEC/NA			
ON ON ON	4.8 USEC/NA			

SIGNAL NAME (ORIGINATING PIN)	PULSE WIDTH FOR M8655	PULSE WIDTH FOR M8655 YA	PULSE WIDTH FOR M8655 YB	PULSE WIDTH FOR M8655 YC
P99 NSEC (E03-03)	99 NSEC	113 NSEC	163 MSEC	192 MSEC
P296 NSEC (E08-09)	296 NSEC	339 NSEC	489 NSEC	573 NSEC
P592 NSEC (E06-08)	592 NSEC	677 NSEC	976 NSEC	114 MICROSEC
P3.26 MICROSEC (E15-09)	3.26 MICROSEC	3.74 MICROSEC	5.39 MICROSEC	6.31 MICROSEC
P1.09 MICROSEC (E15-12)	*1.09 MICROSEC	*1.23 MICROSEC	*1.78 MICROSEC	*2.12 MICROSEC
P17.8 MICROSEC (E14-11)	17.8 MICROSEC	20.2 MICROSEC	29.3 MICROSEC	33.4 MICROSEC
SIGNAL NAME (ORIGINATING PIN)	PULSE WIDTH FOR M8655-YD			
P99 NSEC (E03-03)	146 NSEC			
P296 NSEC (E08-09)	438 NSEC			
P592 NSEC (E06-08)	877 NSEC			
P3.26 MICROSEC (E15-09)	4.83 USEC			
P1.09 MICROSEC (E15-12)	1.615 USEC			
P17.8 MICROSEC (E14-11)	26.3 USEC			

NOTE: DIFFERENTIATION BETWEEN M8655, YA, YB, YC AND YD MODULES IS THE XTAL SELECTION.  
\*W2 OUT, W5 IN FOR THESE CLOCK PULSES—W2 IN W5 OUT FOR ALL OTHER CASES.



NOTE: THIS TABLE IN REFERENCE TO SHEET 3 OF M8655 LOGIC DIAGRAM.

REVISIONS		
CHK	CHANGE NO	REV.





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TITLE KL8-JA TERMINAL CONTROL/ASYNCHRONOUS DATA INTERFACE

until the next character began to be assembled. The KL8-JA being double buffered, has an additional register between the receiver shift register and the AC. In this case, a character is assembled in the shift register and transferred to the "receive holding register" at which time the receive flag is set indicating that a character is available. The character remains available to the CPU in the holding register until the next character is completely assembled allowing the program roughly an order of magnitude more time to react to a receive flag and read a character.

In the transmission of data with earlier interfaces, time was lost between the transmission of characters since the shift register had to be completely empty before the transmit flag was set and the next character transmission wouldn't start until the CPU (program) got around to issuing another character. Double buffering in this case ("transmit holding register" between the AC and transmit shift register) eliminates this lost time since the transmit flag is set (indication to the CPU that another character may be issued to the interface) when the holding register to shift register transfer has been made. To maintain full speed transmission of characters, the CPU must only react to the transmit flag within one character time to refill the holding register.

3.2 M8655/External Device Operation & Serial Data Format

3.2.1 Data Leads

Section 2.0 referred to electrically compatible data leads. The KL8-JA provides two types of data leads for different applications: 20 mA and EIA leads (choice is made by cable selection).

The 20 mA circuits represent the binary information as a switch connected to a power source, i.e., switch open = "1", switch closed = "0". The 20 mA data circuits on the M8655 are active. The power source for both the transmit and receive circuits is on the M8655. For an external device to be electrically compatible, its transmit and receive

SIZE	CODE	NUMBER	REV
A	SP	KL8-JA-1	

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circuits must be passive (no power added to the 20mA lines). (More technical information in section 4.5 on cabling.)

The EIA data leads represent binary data as one of two voltage levels. When using these lines, EIA (Electronics Industry Association) specification RS232-C must be adhered to.

3.2.2 Serial Data Format

KL8-JA/external device operation is asynchronous (a character or string of characters may begin at any point in time) and full duplex (transfers may occur in both directions simultaneously).

Where data is transferred serially, all definitions concerning that data are made with respect to time. Baud rate is the rate at which these decisions may be made. (Baud rate is the total possible bits/second.)

A data line may be in one of two states - mark or space. In the idle state (no data being transferred), the line is in the mark state. To signify to the receiving unit that a character is coming, the line changes to the space state for 1/baud rate seconds (start bit). This is followed by the data (5 to 8 data bits, LSB first). If parity is used, it appears after the most significant bit. This is followed by a return to the idle state which lasts for 1, 1.5 or 2 bit times (stop bit(s)). The next character may occur at any time after that. Following are the character definitions applicable to the KL8-JA.

Transmit Baud Rate - 110, 150, 300, 600, 1200, 2400, 4800, 9600 (Switch Selectable).

Receive Baud Rate - May be set equal to the transmit baud rate or 150 baud (Switch Selectable).

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A	SP	KL8-JA-1	

TITLE KL8-JA TERMINAL CONTROL/ASYNCHRONOUS DATA INTERFACE

- Start Bit - Always 1 per character
- Data Bits - 5, 6, 7 or 8 (Jumper Selectable)
- Parity - Even, odd or none (Jumper Selectable)  
(Parity is inserted after most significant data bit.)
- Stop Bits - Choice of 1 or 2 for 6, 7 and 8 data bits.  
Choice of 1 or 1.5 for 5 data bits.  
(Jumper Selectable)

3.3 Additional Options

3.3.1 Error Status Word

The error status word may be enabled by the insertion of jumper "SWD". Detected are parity, framing and overrun errors (see Programming section).

3.3.2 Filler Characters - VT05

To operate at speeds above 300 baud, the VT05 requires that filler characters be transmitted to it following any line feed character. Insertion of the "FIL" jumper on the M8655 causes four all zero characters to be automatically transmitted to the VT05 following every line feed. The transmit flag is not set until the KL8-JA is ready to accept other data.

3.3.3 Reader Run

Reader control is provided for operating LT33 teletypes. See Programming section.

3.3.4 Teletype Filter

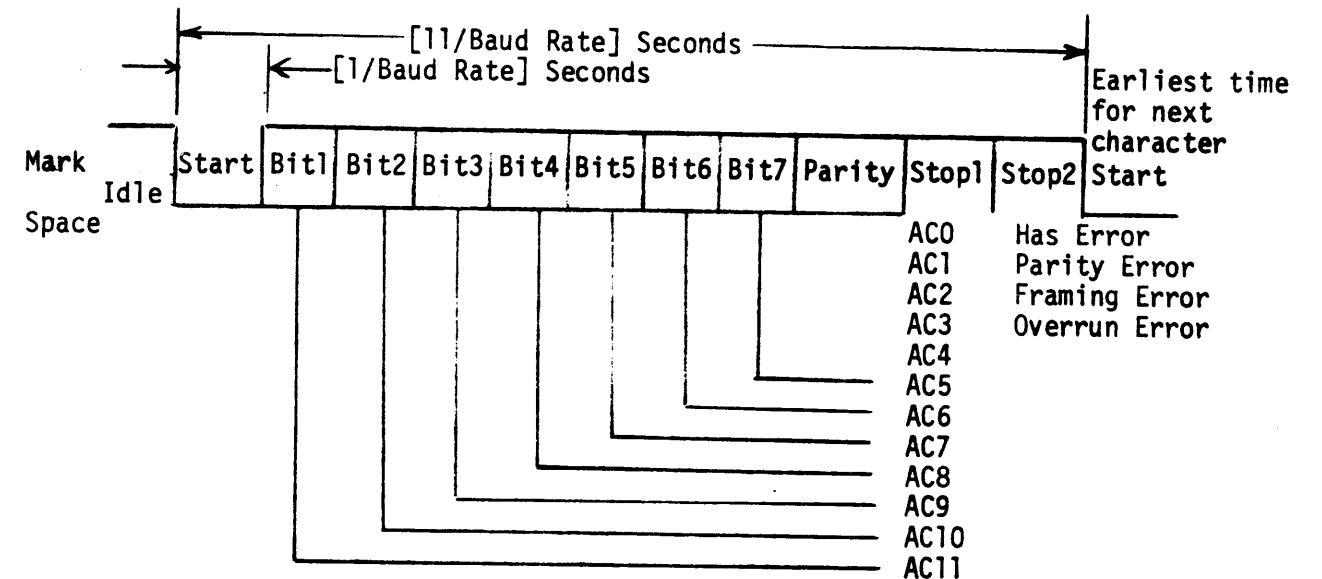
LT33 teletypes require a relatively large filter capacitor across the receiver lines. Installing the "TTY" jumper connects this capacitor.

SIZE	CODE	NUMBER	REV
A	P		

TITLE KL8-JA TERMINAL CONTROL/ASYNCHRONOUS DATA INTERFACE

SERIAL CHARACTER DEFINITION

Figure 1



The above example shows a character of one start bit, seven data bits, parity bit and two stop bits. Also shown is the relationship of the error status word to the AC bits.

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A	SP	KL8-JA-1	

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TITLE KL8-JA TERMINAL CONTROL/ASYNCHRONOUS DATA INTERFACE

4.0 Specifications

4.1 Physical

The M8655 meets the dimensional requirements for Omnibus type quad modules. Ref. D-MD-7605994 of the PDP8/E/F/M print set.

4.2 Power Requirements

From Omnibus - +5V at 1.1 Amps, -15V at 100 mA, +15V at 50 mA.  
From external device - None

4.3 Environmental Requirements

Ambient temperature of M8655 - Operate between 0 and 55°C  
Store between -15 and 65°C  
Humidity - 10% to 90% non-condensing

4.4 System Configuration Restrictions

Maximum number of M8655's in one PDP8/E system - 17 or the power supply limit.

4.5 External Signals and Cabling Requirements

4.5.1 EIA signals

The EIA signals and their assigned pins on the 40 pin connector (Circuit Schematic Ref. J1) are as follows:

Signal Name	Pin at J1
Protective Ground	UU
Send Data	F
Receive Data	J
Request to Send	V (Held Asserted)
Signal Ground	VV
Data Terminal Ready	DD (Held Asserted)

(Received data after EIA to TTL level conversion is jumpered at cable, pins E and M). Since the "Request to Send" lead is held true, M8655's are suitable for

SIZE	CODE	NUMBER	REV
A	SP	KL8-JA-1	

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FULL DUPLEX operation only.

Modem Control may be accomplished when an M8655 is combined with a KL8-M (M8653).

Total cable length from KL8-JA to associated terminal or modem must not exceed 50 feet.

4.5.2 20mA Signals

The 20mA signals provided and their assigned pins at the 40-pin connector (Circuit Schmetic Ref. J1) and at the Mate-N-Lock end of a BC05-M cable are as follows:

Signal Name	Pin at J1	Pin at BC05-M
Transmit +	AA	5
Transmit -	KK	2
Receive +	K	7
Receive -	S	3
Reader Run +	PP	6
Reader Run -	EE	4

} For LT33 Operation Only

(Received data after 20mA to TTL level conversion is jumpered at J1 pins E & H.)

The factors limiting the length of cable which may be attached to the 20mA circuits are: a) the total resistance which may be driven or, b) the total capacitance seen by the transmitter and receiver and the selected baud rate.

The following information will allow the user to calculate maximum cable distances:

Transmit + to Transmit -	700Ω
Receive + to Receive -	600Ω
Reader Run + to Reader Run -	1220Ω

(LT33 reader circuit has 1KΩ resistance which leaves 220 for total cable resistance.)

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A	SP	KL8-JA-1	

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Some Wire Resistances:

Wire Size	Ohms/1000 feet
26 AWG	40.81
24 AWG	25.67
22 AWG	16.14
18 AWG	8.05

Formula for calculating maximum distance due to cable capacitance and baud rate.

$$D_{max} = \frac{.3 \times 10^{-3}}{C_c \cdot Bd} - \left( \frac{C_T + C_R}{C_c} \right)$$

Where:  $D_{max}$  = maximum distance external device may be placed from KL8-JA.  
 $C_c$  = capacitance of cable per foot.  
 $Bd$  = baud rate.  
 $C_R$  = Capacitance across the receiver circuit in question.  
 $C_T$  = Capacitance across the transmitter circuit in question.

$C_R$  for M8655 is 2.2 uf if TTY jumper is installed;  $\emptyset$  if not.

$C_T$  for M8655 is  $\emptyset$ .

$C_R$  and  $C_T$  must be determined for external device.

Examples:

- LT33 with reader.  
 The limiting factor in this case is the Reader Run circuit. Using 26 AWG cable, the maximum wire length is  $\frac{220}{40.81/1000 \text{ feet}}$  or 5390 feet from Reader Run to Reader-. Therefore the maximum cable length is 2695 feet.

SIZE	CODE	NUMBER	REV
A			

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- High speed terminal (9600 baud) with  $\emptyset$  capacitance in either its transmitter or receiver. The limiting factor is cable capacitance. For this example cable capacitance is 30 pf/ft.

$$D_{max} = \frac{.3 \times 10^{-3}}{30 \times 10^{-12} \cdot 9600} - \frac{\emptyset}{30 \times 10^{-12}} = \frac{.3 \times 10^{-3}}{.288 \times 10^{-6}} = 1040 \text{ ft.}$$

## 4.6 Module Setup - Jumpers and Switches

Refer to Dwg. D-CS-M8655- $\emptyset$ -1, Sheet 1.

## 5.0 Programming

### 5.1 Instruction Set

- 6XX $\emptyset$  Clear keyboard flag (KCF)  
  
Receiver flag is cleared without clearing the AC or enabling the reader.
- 6XX1 Skip if keyboard flag is set (KSF)  
Increments the program counter to one location beyond the next sequential instruction if the receiver flag is set.
- 6XX2 Clear keyboard flag and set reader run (KCC)  
Clear the receiver flag, and AC, and enable the reader.
- 6XX4 Read keyboard static (KRS)  
Performs inclusive or of the receiver register and the AC leaving the result in the AC.
- 6XX5-AC11 Set/Clear Interrupt enable (KIE)  
Loads AC bit 11 into the interrupt enable flip flop on the M8655. (1) = enable, ( $\emptyset$ ) = disable.
- 6XX5-AC10 Set/Clear status enable (KSE).  
Loads AC bit 10 into status enable flip flop on M8655. (1) = enable, ( $\emptyset$ ) = disable. With SWD jumper installed, the status enable flop set causes the status word to be loaded into AC bits  $\emptyset$ -3 when a character is read (KRS or KRB inst.).

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A	SP	KL8-JA-1	

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- 6XX6 Read keyboard buffer dynamic (KRB)  
Performs the combined operations of KCC and KRS.
- 6YY0 Set teleprinter flag (TFL)  
Set the transmit flag.
- 6YY1 Skip on teleprinter flag (TSF)  
Increments the contents of the program counter to one location beyond the next sequential instruction if the transmit flag is set.
- 6YY2 Clear teleprinter flag (TCF)  
Clear the transmit flag.
- 6YY4 Load Teleprinter & Print (TPC)  
The least significant bits of the AC are transferred to a data holding register on the M8655 and then transmitted. The transmit flag is not cleared by this instruction.
- 6YY5 Skip if teletype interrupt (SPI)  
The next sequential instruction is skipped if the transmit or receive flag is set and the interrupt enable flip flop is set.
- 6YY6 Print character (TLS)  
Combination of TCF and TPC performed.

5.2 Operation

5.2.1 Initialize

Initialize (key clear or CAF 6007 instruction) clears the receive flag, transmit flag and status word enable flip-flop, if applicable. It also sets the interrupt enable flip-flop.

Initialize does not reset the transmit or receive circuitry; i.e., if the M8655 were in the process of transmitting or receiving a character, the respective flag is set at the appropriate time despite the issuance of initialize. This circuitry is cleared only when power is first applied to the PDP8.

SIZE <b>A</b>	CODE SP	NUMBER KL8-JA-1	REV
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TITLE KL8-JA TERMINAL CONTROL/ASYNCHRONOUS DATA INTERFACE

5.2.2 Status Word

This section applies only when the "SWD" jumper is installed on the M8655. (When this jumper is out, the read status logic is disabled.) Error status is read with the data bits when a read IOT is issued (KRS or KRB) if the status enable flip-flop was previously set.

- AC0 Inclusive or of the three error conditions.  
1 = error.
- AC1 Parity error (If NP jumper is not installed, this bit will always receive a zero.)
- AC2 Framing Error = 1 if a legal stop bit was not detected (a space was detected half way through Stop Bit 1).
- AC3 Overrun Error = 1 if the receive flag was not cleared prior to the character now being read (one character transmitted after another by the teletype without the first being read by the computer).

AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7	AC8	AC9	AC10	AC11
Error	Parity Error	Framing Error	Overrun Error	MSB	← Data Bits →				LSB		

AC After KRS or KRB Instruction With Status Enabled

SIZE <b>A</b>	CODE SP	NUMBER KL8-JA-1	REV
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TITLE KL8-JA TERMINAL CONTROL/ASYNCHRONOUS DATA INTERFACE

## 5.2.3 Receive Flag

The receiver flag is cleared by key clear, or the CAF, KCF, KCC, and KRB instructions.

The receiver flag is set half way through the first stop bit of the characters being transmitted by the external device. This differs from the operation of earlier serial interfaces in that they did not look for framing errors and therefore could set the receiver flag half way through the most significant bit.

## 5.2.4 Reader Run

Reader Run is typically set when the previously read character is read into the AC. It is cleared when the start bit of the character to be read is detected. (Cleared half way through the start bit.)

## 5.2.5 Transmit Flag

The Transmit flag is cleared by initialize, or the TCF and TLS instructions.

The Transmit flag is set by the TFL instruction or anytime the Transmitter buffer is empty. (The transmission may or may not have occurred at this time.)

When a character is to be transmitted to the external device, the character is received by the M8655, loaded into the transmit buffer, then loaded into the shift register from which the actual transmission occurs.

The first character being transmitted goes almost immediately from the transmit buffer to the shift register and the transmit flag is set. If another character is transferred from the computer at this time, the transmit flag is next set at the completion of the first transmission. (The transmit buffer is again empty.)

SIZE	CODE	NUMBER	REV
A	SP	KL8-JA-1	





TITLE

- E. Set switches "RECEIVE" & "TRANSMIT" to the customer specified device codes as illustrated on sheet 1 of the circuit schematic.
- F. Set baud rate as specified by customer as shown on sheet 1 of circuit schematic.
- G. Install jumpers that are required by the customer. Parity, even parity, bits/character, fill characters TTY jumper and error status word. Ref. sheet 1 of circuit schematic.
- H. Be sure power is off in PDP8 E/M/F and insert the M8655 into the omnibus according to PDP 8E maintenance manual Vol. 1 table 2-3.

## III. Acceptance procedure

- A. Load Maindec 08-DIKLA-A-PB (Loop Back Test) using normal binary loading procedures.
  - 1. Run diagnostic according to the Maindec write-up Maindec 08-DIKLA-A-D.
  - 2. Run at customers specified baud rate for 1 pass in 20 MA mode, and 1 pass in EIA mode. (See note 1) No errors are acceptable.
- B. If the KL8-JA is shipped with a teletype, load Maindec 08-DIKLB-A-PB using normal loading procedures.
  - 1. Run program 4 according to the maindec's write up, Maindec-08-DIKLB-A-D.
  - 2. No errors are acceptable.
- C. If the KL8-JA is shipped with a VT05 load, Maindec 08-DGV5A-B-PB using normal binary loading procedures.
  - 1. Run diagnostic for 1 complete pass according to the Maindec's writeup, Maindec 08-DGV5-B-D.
  - 2. No errors are acceptable.
- D. If the KL8-JA is shipped with a serial LA30, load Maindec-08-DHLAA-A-PB using normal binary loading procedures.

SIZE	CODE	NUMBER	REV
A	SP	KL8-JA-2	

TITLE

- 1. Run diagnostic for 1 complete pass according to the Maindec's writeup, Maindec-08-DHLAA-A-D.
- 2. No errors are acceptable.

Note: 1

- J1 connections for 20MA loop back test mode
  - E-H
  - K-KK
  - S-AA
- J1 connections for EIA loop back test mode
  - E-M
  - F-I

SIZE	CODE	NUMBER	REV
A	SP	KL8-JA-2	

