DEC-11-HR4C-D

KL11
teletype control
manual

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

1st Printing September 1970
2nd Printing (Rev) March 1971
3rd Printing (Rev) December 1971

The material in this manual is for informational purposes and is subject to change without notice.

CONTENTS

ILLUSTRATIONS

TABLES

CHAPTER 1
INTRODUCTION

This manual provides the user with the theory of operation and logic diagrams necessary to understand and maintain the KL11 Teletype® Control. The level of discussion assumes that the reader is familiar with basic digital computer theory. This manual contains both general and detailed descriptions of the Teletype Control.

Although control signals and data are transferred between the Teletype Control and the Unibus™, this manual does not cover operation of the bus itself. A detailed description of the Unibus is presented in the *PDP-11 Unibus Interface Manual* (DEC-11-HIAB-D). Because the Teletype Control is basically an interface between the bus and the Teletype, it is also beyond the scope of this manual to discuss operation of the Teletype unit itself. Detailed operation and maintenance of the 33 ASR Teletype is covered in *Teletype Corporation Bulletin 273B* (two volumes).

A complete set of engineering logic drawings is provided with each Teletype Control. These drawings are bound in a separate volume entitled *KL11 Teletype Control, Engineering Drawings.* The reduced drawings in the above manual reflect the latest print revisions and correspond to the specific component shipped to the customer.

This manual is divided into six major chapters: Introduction, General Description, Detailed Description, Programming Information, Adjustments, and Maintenance.

® Teletype is a registered trademark of the Teletype Corporation.

™ Unibus is a trademark of Digital Equipment Corporation.

CHAPTER 2
GENERAL DESCRIPTION

2.1 INTRODUCTION

A Teletype unit is provided as standard equipment with the PDP-11/20 System. This unit serves as an input (keyboard and perforated paper-tape reader) and an output (page-printer and tape punch) device for the system.

The KL11 Teletype Control assembles or disassembles Teletype serial information for parallel transfer to, or from, the PDP-11 Unibus. The control consists of three integrated circuit modules mounted on one-fourth of a system unit (slots 13 or 14 in the KA11 or KC11 Processor or slots 1, 2, 3, or 4 in the DD11-A Peripheral Mounting Panel). Thus, four Teletype Control interfaces can be mounted in the space of a single system unit.

There are six different models of the KL11 Teletype Control. This manual describes the KL11-A. Models KL11-B through KL11-F operate in an almost identical manner but differ in baud rates, bit times, etc. In addition, models B through F have only one, rather than two, HALT bits. The differences in the six different models are given in Appendix A.

2.2 TELETYPE

The 33 ASR Teletype (Model LT33-D) is the unit normally supplied with the PDP-11 System. However, there are seven other models that may also be used with the system. Each of these models is covered in the *Power Supply and Mounting Box Manual.* The KL11 Teletype Control is compatible with all eight Teletype models. For purposes of clarity in this manual, all Teletype references pertain to the 33 ASR.

The 33 ASR Teletype is used to type in or print out information at a rate of up to 10 characters per second. In addition, it has a paper-tape capability and can read in or punch out perforated oiled tapes at the rate of up to 10 characters per second.

Signals transferred between the Teletype and the Teletype Control are standard, serial, 11-bit code, Teletype signals. These signals consist of marks and spaces that correspond to bias and idle current in the Teletype, and to 1's and 0's in the computer. The 11-bit code consists of a start bit, 8 data bits, and 2 halt bits.

The 8-bit data code used by the Teletype is a modified ASCII code. To convert ASCII to Teletype code, 200 octal is added. This code is read in the normal octal form used in the system. Bits are numbered from right to left, from 0 through 7, with bits 0 through 2 containing the least significant octal number.

2.3 TELETYPE CONTROL

Serial information read or written by the Teletype Unit is assembled or disassembled by the Teletype Control interface for parallel transfer to or from the Unibus. When the processor addresses the bus, the Teletype Control decodes the address to determine if the Teletype is the selected external device and, if selected, whether it is to perform an input or output operation. For the following discussion, refer to the Teletype Control simplified block diagram shown in Figure 2-1.

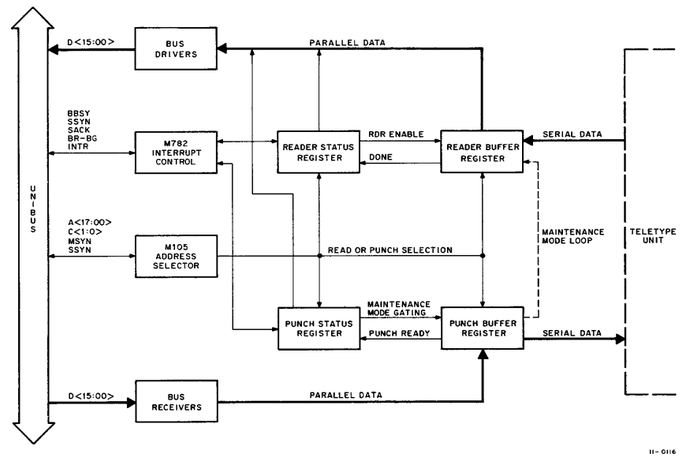


Figure 2-1 Teletype Control Interface Simplified Block Diagram

The Address Selector module decodes the incoming address and responds to one of four possible sequential addresses. The register that is selected and the type of bus data transfer operation being performed determine whether a read or punch operation is to be used. If, for example, the Teletype has been selected to accept information for printout, parallel data from the Unibus is loaded into the internal punch buffer. At this point the punch ready flag drops because the punch logic has been activated. The interface then generates a start bit, shifts the data from the buffer into the Teletype, one bit at a time, again sets the punch ready flag, and then times out two halt bits. Thus, the 8-bit parallel bus data is converted to the 11-bit serial input required by the Teletype. Whenever a series of characters is to be loaded into the Teletype, the punch ready flag is set prior to generation of the halt bits, thus allowing another character to be loaded from the bus as soon as the buffer is empty.

The punch ready flag is used to activate the interrupt control module, provided the module is enabled. The purpose of this module is to cause a program interrupt by means of a specific vector address.

When receiving data from the Teletype, the operation is essentially the reverse. The start bit of the 11-bit Teletype serial data activates the interface, and data is loaded a bit at a time into the reader buffer register. When loading of the buffer is complete, the interface sets a done flag, indicating to the program that a character has been assembled. The reader done flag activates the interrupt control module (if enabled), thereby causing a vectored interrupt.

The Teletype Control can also be operated in a maintenance mode, which is selected by the program by setting the appropriate bit in the punch status register. When in this mode, special logic is used to perform a closed loop test of the Teletype Control interface circuits. A character from the bus is loaded in parallel into the punch buffer register. The serial output of the register, rather than entering the Teletype, enters the reader buffer register where it is converted back into parallel data and applied to the bus. If the interface is functioning properly, the character received by the bus is identical to the character transmitted by the bus.

CHAPTER 3
DETAILED DESCRIPTION

3.1 INTRODUCTION

This chapter provides a detailed description of the KL11 Teletype Control. The Teletype Control may be divided into five major functional areas: selection logic, interrupt logic, transmitter logic, receiver logic, and maintenance mode logic. Each of these areas is covered separately in subsequent paragraphs. The purpose of each of these functional units is as follows:

selection logic	– determines if the Teletype unit has been selected for use and what type of operation (transmit or receive) has been selected. Consists of M105 Address Selector module and part of the M780 KL11 Teletype Control module.
interrupt logic	– permits the Teletype Control to gain bus control and perform a program interrupt. Priority level of bus request (BR) line may be changed by user. Consists of an M782* Interrupt Control module and interrupt enable bits within other functional areas.
transmitter logic	– converts parallel data from bus to serial data so the Teletype can punch the data into paper tape or print it out. Consists of part of the M780 KL11 Teletype Control module.
receiver logic	– converts serial data from either the Teletype keyboard or paper-tape reader into parallel data for transmission to the bus. Consists of part of the M780 KL11 Teletype Control module.
maintenance mode logic	– performs a closed loop test of the KL11 Teletype Control logic. Consists of part of the M780 KL11 Teletype Control module.

It should be noted that the Teletype Unit performs one of two basic operations: transmitting or receiving data. When transmitting, it prints data in hard copy on the printer and punches holes in paper tape (provided the punch is on). Thus, "transmitter", "printer", and "punch", all refer to the same basic operation. Conversely, when receiving data, the Teletype either reads data from the keyboard or from a punched paper-tape reader. Thus, "receiver", "keyboard", and "reader" all refer to the same basic operation.

The discussions in this chapter are supported by a complete set of engineering drawings located at the end of this manual. Programming, adjustment, and maintenance information are covered in subsequent chapters of this manual.

3.2 SELECTION LOGIC

The KL11 Teletype Control selection logic is used to decode the address on the bus lines to determine if the Teletype Unit has been selected for use. Unique addresses are assigned to registers in both the receiver and the transmitter logic; thus the manipulation of these registers (reading or writing) determines whether a character is to be read from the keyboard (or paper-tape reader) or printed out by the printer (or paper-tape punch).

The Teletype Control interface consists of four registers (or bus addresses). The selection logic is used to control the information flow between the Unibus and the interface registers. The logic produces SELECT line and gating IN or OUT signals, which determine the register to be used and whether it is to perform an input or output function.

The selection logic consists of an M105 Address Selector module, gating logic, and bus drivers and receivers.

3.2.1 Address Selector Module

The M105 Address Selector module (drawing CS-M105-0-1) decodes the address information from the bus and provides two gating signals and four select line signals that are used to activate appropriate Teletype Control circuits for the selected register. The M105 module jumpers are arranged so that the module responds only to standard device register addresses 777560 through 777566. Although these addresses have been selected by DEC as the standard assignment for the Teletype Control, the customer may change the jumpers to any address desired. However, any MainDEC program that references the Teletype standard address assignment must be modified if other than the standard assignments are used.

It is beyond the scope of this discussion to cover operation of the M105 Address Selector; detailed descriptions of this module are covered in the *1970 DEC Logic Handbook* and in the *Unibus Interface Manual* (DEC-11-HIAB-D).

3.2.2 Gating Logic

The gating signals and select line signals from the M105 Address Selector are applied to gating logic (drawing CS-M780-0-1), which provides the pulses that activate either the transmitter or receiver circuits. These pulses enable the bus drivers and bus receivers that are connected to the punch buffer (TPB) and punch status (TPS) registers in the transmitter logic, and to the reader buffer (TKB) and reader status (TKS) registers in the receiver logic.

The four register select signals (SELECT 0, SELECT 2, SELECT 4, and SELECT 6) indicate which register is being referenced. The two gating signals (IN, OUT LOW) indicate the direction of data flow.* The gating signals

* There are three modules that can be used to perform the Interrupt Control function, the M782, M7820, and M7821. The M782 and M7820 are identical except that the M7820 has a vector address range of 000–777, whereas the M782 has a range of 000–377. The M7821 has additional circuits to improve the NPR latency in large systems, but is otherwise pin compatible with the M782 and M7820. However, the M7821 uses a jumper for a 1 in the vector address bits, and the M782 and M7820 use a jumper for a 0.

* Direction on the Unibus is defined in relation to the master device, which in this case is the processor. Thus, IN means that the processor is reading information from the selected address; OUT LOW means that the processor is loading data into the selected address.

either gate data from the Teletype Control to the bus (IN) or gate data from the bus into the Teletype Control (OUT LOW).

The gating signals, select lines, and related functions are listed in Table 3-1.

Table 3-1
Gating and Select Line Signals

Sel. 0	Sel. 2	Sel. 4	Sel. 6	Gating Signal	Function Selected	Reg.	Bus Cycle
0	1	0	0	IN	Reader buffer to bus	TKB	DATI or DATIP
1	0	0	0	IN	Reader CSR to bus	TKS	DATI or DATIP
0	0	1	0	IN	Punch CSR to bus	TPS	DATI or DATIP
0	0	0	1	OUT LOW	Bus to punch buffer	TPB	DATO or DATOB
1	0	0	0	OUT LOW	Bus to reader CSR	TKS	DATO or DATOB
0	0	1	0	OUT LOW	Bus to punch CSR	TPS	DATO or DATOB

3.2.3 Bus Drivers and Receivers

The bus drivers and receivers (drawing CS-M780-0-1, sheet 2) are logic gates that are used to pass signals to and from the Unibus while maintaining the transmission-line characteristics of the bus. These gates have a high input impedance and proper logic thresholds required by the bus signals. It is beyond the scope of this manual to provide detailed information on bus drivers and receivers; detailed information is contained in the *1970 DEC Logic Handbook* and in the *Unibus Interface Manual* (DEC-11-HIAB-D).

3.3 INTERRUPT CONTROL

The M782 Interrupt Control module permits the Teletype Unit to gain control of the bus (become bus master) and perform an interrupt operation. When the reader done (RDR DONE) flag is set, it activates the interrupt control so that it can notify the processor that a character has been assembled. When the punch ready (PUN READY) flag is set, it activates the interrupt control so that it can notify the processor that another character can be loaded into the punch buffer. The jumper arrangement is for standard device vector addresses 60 and 64. Although this is the recommended address, the user may change the jumpers to correspond to any vector address desired, but MainDEC programs reference the standard vector addresses.

The reader initiates an interrupt whenever DONE = 1 and ID = 1 both become true. The vector address is 60. The punch initiates an interrupt whenever READY = 1 and ID = 1 both become true. This vector address is 64. The standard priority interrupt level is set at the BR4 level for both the reader and the punch. The reader has a slightly higher priority because it is electrically closer to the processor on the BG4 level. Although standard, the priority level may be changed by the user, if desired. MainDEC programs, however, reference priority level 4.

It is beyond the scope of this manual to cover detailed operation of the M782 Interrupt Control module; detailed descriptions of this module are covered in the *1970 DEC Logic Handbook* and in the *Unibus Interface Manual* (DEC-11-HIAB-D).

3.4 TRANSMITTER LOGIC

Upon program command, a character from a memory location (or a general register within the processor) is sent in parallel to the Teleprinter/Punch Buffer (TPB) register for transmission to the Teleprinter/Punch Unit in the Teletype. The TPB buffer register, part of the Teletype Control transmitter logic, consists of two 4-bit shift registers. The transmitter logic generates a start (space), shifts eight data bits serially into the Teletype Unit, and then generates halt marks. In effect, the eight bits from the Unibus (byte data) are converted to an 11-bit serial output consisting of a start bit, eight data bits, and two halt bits.

The transfer of information from the buffer into the Teletype Unit is accomplished at the normal Teletype rate and requires 100 ms for completion. A PUN READY flag indicates when the buffer is ready to receive another character.

The transmitter control logic operates by: initializing the logic, generating a clock, loading data from the bus into the buffer, shifting the data from the buffer serially into the Teletype, and halting when the transfer is complete. These functions are described in the subsequent paragraphs. The transmitter logic circuits are shown on drawing D-CS-M780-0-1, sheet 3; the transmitter timing diagram is shown on drawing D-TD-KL11-0-4.

3.4.1 Functional Description

This paragraph presents a functional description of the punch buffer register to aid the user in understanding the more detailed loading and shifting operations discussed in subsequent paragraphs. From a functional standpoint, the register should be considered as an 11-bit register consisting of the POINTER flip-flop, the 8-bit punch buffer, the LINE START flip-flop, and the LINE flip-flop.

When the TPB is loaded (e.g., MOV R0, TKB), information from the Unibus data lines is parallel-loaded into the buffer register and the POINTER flip-flop is set. At this point, bus data is stored in the punch buffer register along with a pointer bit that is used to indicate when the data has all been transferred to the punch/printer. Loading the buffer initiates transmitter action by clearing the PUN READY signal and turning on the clock. At this point, LINE is set and LINE START is clear.

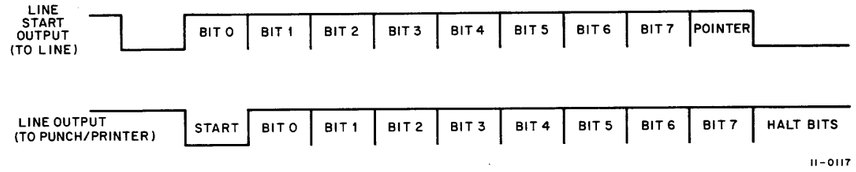
As the clock runs, it shifts out a start bit to indicate to the Teletype that it is now transmitting data. The register bits (pointer, buffer, line start, line) are then shifted out one at a time, starting with the least significant bit (LSB). The last bit shifted out is the previously stored pointer bit that indicates to the control logic that all data has been transmitted to the Teletype. The pointer is not sent to the Teletype but is used to generate a last bit signal that, in turn, produces two halt bits. The halt bits allow the Teletype to complete its printing cycle before the start of the next character.

The scheme used by the logic to keep track of the data transfer operation can be more easily understood by referring to Figure 3-1. This figure shows the status of data within the buffer and the states of the POINTER, LINE START, and LINE flip-flops. The state of the LINE flip-flop indicates the serial output of the interface. Note that the information in this 11-bit register keeps shifting across until the buffer finally contains all zeros and the pointer bit is shifted into the LINE flip-flop. These conditions qualify logic circuits that signal the end of the transfer operation.

3.4.2 Initialize

The first signal to enter the transmitter control logic is the BUS INIT L signal, which is normally generated when power is applied to the system. It can also be generated either by depressing the START switch on the programmer's console or by issuing a programmed RESET instruction. This signal sets all transmitter logic to the appropriate initial states to make certain that the transmitter is ready to begin a new operation.

The BUS INIT L signal clears the PUN RUN, POINTER, HALT 1, HALT 2, and PUN INT ENB flip-flops and the punch buffer register. The LINE flip-flop is normally held in the set state and the LINE START flip-flop is normally held clear. Thus, the initial states are LINE set, all other flip-flops cleared.



Pointer Bit	Buffer Contents									Line Start	Line	Remarks
0	0	0	0	0	0	0	0	0		0	1	After initialize, READY is set
1	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0		0	1	After loading, READY is cleared
0	1	X_7	X_6	X_5	X_4	X_3	X_2	X_1		X_0	0	Start bit (after first shift)
0	0	1	X_7	X_6	X_5	X_4	X_3	X_2		X_1	X_0	Data bit 0 (after second shift)
0	0	0	1	X_7	X_6	X_5	X_4	X_3		X_2	X_1	Data bit 1 (after third shift)
					.							Data bit 2
					.							Data bit 3
					.							Data bit 4
					.							Data bit 5
0	0	0	0	0	0	0	0	1		X_7	X_6	Data bit 6
0	0	0	0	0	0	0	0	0		1	X_7	Data bit 7 (after ninth shift) (Pointer Bit)
0	0	0	0	0	0	0	0	0		0	1	1st halt bit (after tenth shift) READY is set
					NOTE							
					Buffer can be reloaded after this shift, and 0's become X's again.							
0	0	0	0	0	0	0	0	0		0	1	2nd halt bit (after eleventh shift)

Figure 3-1 11-Bit Shift Register Operation

The fact that the buffer register is clear and both the POINTER and LINE START flip-flops are clear qualifies a gate that produces a PUN READY H signal to indicate that the transmitter logic is ready to receive data.

3.4.3 Loading

When the Teletype Printer/Punch has been selected for use, the transmitter selection circuits produce a BUS TO PUN BUF H pulse that sets the POINTER flip-flop and also qualifies a series of gates to produce the PUN BUF CLOCK L pulse. This initial PUN BUF CLOCK L pulse sets the POINTER flip-flop because the D input is high; however, subsequent PUN BUF CLOCK L pulses keep the POINTER flip-flop continually in the cleared state.

At the same time it sets the POINTER, the PUN BUF CLOCK L pulse parallel loads the buffer register with the information on Unibus data lines D ⟨07:00⟩. Loading is accomplished because the SHIFT control on the buffer is low, the LOAD control on the buffer is high, and the CLOCK input is making a negative transition. Since the POINTER flip-flop is set during loading, it disqualifies the gate producing the PUN READY H and the flag drops to indicate that the transmitter circuits are now being used.

3.4.4 Clock

When the BUS TO PUN BUF H pulse goes low after approximately 250 ns, the PUN BUF CLOCK L pulse is no longer produced. Since the 1 output of the HALT 2 flip-flop is low, the trailing edge of the BUS TO PUN BUF pulse produces a positive transition at the clock input of the PUN RUN flip-flop. The data input to this flip-flop is high because the POINTER is set. The high level at the data input and the positive-edge clock input set the PUN RUN flip-flop.

The 1 output of the PUN RUN flip-flop qualifies a series of gates that triggers the PUN CLOCK one-shot to produce a low on the 0 side. The transition of the 0 side from high to low produces a pulse that is ORed into the PUN BUF CLOCK L. This is the same signal that was produced during loading but is now produced by the PUN CLOCK flip-flop. When the PUN CLOCK one-shot times out (i.e., after 9.09 ms, the 0 side returns to a high level), the clock output is fed back through a series of gates which causes a delay of approximately two μs, to retrigger the PUN CLOCK one-shot. The PUN RUN flip-flop enables the PUN CLOCK to retrigger, again producing a low on the 0 side. This self-retriggering process continues as long as the PUN RUN flip-flop remains set, which is for the duration of the transfer process.

The clock interval is 9.09 ms in duration and is adjusted by potentiometer R4 in the PUN CLOCK flip-flop circuit. The procedure for making this adjustment is presented in Chapter 5 of this manual.

3.4.5 Shifting

Prior to the shift operation, the POINTER bit is set; the buffer register is loaded with the data from the bus lines; the LINE START flip-flop is cleared; and the LINE flip-flop is set.

The buffer is enabled by a PUN SHIFT ENB H level that is the result of PUN RUN being set and HALT 2 cleared. The first PUN BUF CLOCK L pulse shifts the least significant bit out of the buffer register and into the LINE START flip-flop. The 0 in LINE START is shifted to the LINE flip-flop. This 0 that is in LINE is transmitted to the printer/punch and is used as the start bit. At this point, the conditions are as shown in the third line of the table in Figure 3-1. This shift operation is repeated with each clock pulse until the pointer bit is in the LINE START flip-flop. As can be seen on the figure, at this time the buffer register contains all zeros, LINE START contains the pointer bit, and LINE contains the last bit of data.

Under these conditions, a LAST BIT L level is produced by a gate that is qualified when all buffer register outputs are 0, the POINTER flip-flop is cleared, and LINE START is set (indicating that the pointer bit is present).

The next clock pulse sets the HALT 1 flip-flop, because the LAST BIT L level is present. At the same time, the clock pulse shifts a 1 into LINE to produce the first halt bit. When HALT 1 is set, the 0 side goes low and qualifies a gate that produces the HALTING H signal. This signal disqualifies the gate that produced the PUN SHIFT ENB H pulse; thus, the buffer register is no longer shifted, although the pulses are still applied to the PUN CLOCK buffer.

When the pointer bit shifted out of the LINE START flip-flop, the 0 output went high and enabled a gate which produced the PUN READY H signal, indicating that the transmitter logic had completed transfer of the data bits. At the same time, the 1 side goes low and disqualifies the gate that produced the LAST BIT L level.

When the next clock pulse occurs, it sets the HALT 2 flip-flop (because the 1 side of HALT 1 is high) and clears the HALT 1 flip-flop because the LAST BIT L level is no longer present. The PUN RUN flip-flop does not clear

until HALT 2 is cleared, which occurs on the next clock pulse. The HALT 1 and HALT 2 flip-flops are used to time out two bit times while a 1 is present in the LINE flip-flop.

Note that if the buffer is reloaded at the 81st ms (when READY is set), the PUN READY signal is cleared and, when HALT 2 is cleared, the PUN RUN flip-flop remains set and a second start bit is transmitted to the printer/punch.

3.5 RECEIVER LOGIC

The receiver portion of the Teletype Control receives serial data from the Teletype Reader or Keyboard and converts it to parallel data for transmission to a memory location or a general register within the processor.

The receiver contains an 8-bit buffer register (TKB) that assembles and holds the code for the last character struck on the keyboard or read from the paper-tape reader. The code of the character is loaded into the buffer so that spaces correspond to binary 0's and marks (or holes) correspond to binary 1's. On program command, the contents of the buffer register may be transferred in parallel to the desired location.

Receiver logic is activated by receiving a start bit from the Teletype Unit. The start bit is produced by the Teletype when a key is struck or when the reader is activated. The reader is activated when there is paper in the reader, the reader is turned on, and the reader mechanism is released by setting the RDR ENB flip-flop in the Teletype Control.

Note that RDR ENB remains set until a start bit is received, at which point it is cleared. The bit must be set again to enable the reader to read the next character. This allows character-by-character control. Note also that it is not necessary for the receiver logic to know where the start bit comes from.

Detailed operation of the receiver logic is presented in the following paragraphs. The receiver logic circuits are shown on drawing D-CS-M780-0-1, sheet 4. The receiver timing diagram is shown on drawing D-TD-KL11-0-6.

The first signal to enter the receiver control logic is BUS INIT L, which is generated either by depressing the START switch on the programmer's console or by issuing a programmed RESET instruction. A derivative of the signal clears the RDR START, RDR ACTIVE, and DIV 2 flip-flops to make certain the receiver logic is ready to begin a new operation and to clear the RDR DONE and RDR INT ENB flip-flops.

The reader is enabled by setting bit 0 in the Teletype status register (e.g., MOV #1, TKS). When the Teletype Control selection circuits provide the BD00 H and BUS TO RDR CSR H levels, indicating that the Teletype Reader has been enabled for operation, the two levels set the RDR ENB flip-flop. The output of this flip-flop enables the Teletype Reader by releasing the reader mechanism; the receiver logic can then read in data from the paper-tape reader.

Each Teletype character is represented by an 11-bit serial code that consists of a start bit, eight data bits, and two halt bits. The receiver transforms this serial data into parallel data for use by the bus by loading the serial data one bit at a time into a buffer register (TKB); a RDR DONE signals when the entire character is in the buffer. The buffer actually consists of two 4-bit registers connected to function as an 8-bit (byte) buffer.

The first pulse arriving from the reader is the start bit that sets the RDR START flip-flop to begin receiver operation. The RDR START pulse triggers the RDR CLOCK and also disqualifies a gate, causing the RDR SHIFT ENB H to go low to disable the shift function and enable the load function of the buffer register.

The RDR CLOCK triggers the DIV 2 flip-flop which begins producing a square wave of 4.51 ms duration on the positive pulse and 4.51 ms on the negative pulse for a period of 9.09 ms. The RDR CLOCK is twice the incoming bit rate. The leading edge of the DIV 2 clock is designed to occur in the middle of each incoming character bit to ensure that the data is properly strobed from the reader. Duration of the basic clock, and hence the DIV 2 clock, is adjusted by potentiometer R12. The procedure for making this adjustment is presented in Chapter 5 of this manual.

The first DIV 2 clock leading edge that occurs sets the RDR ACTIVE flip-flop, provided the RDR START flip-flop is set and the start bit is still present. These two flip-flops function together to provide a spike detection circuit. If the first input from the Teletype is a spike rather than a valid start pulse, the RDR ACTIVE flip-flop is not set.

The RDR ACTIVE signal functions as a busy signal to let the processor know that the receiver is accepting data. The RDR ACTIVE flip-flop is also used to keep the clock running after the RDR START flip-flop is cleared.

The first DIV 2 clock produces a RDR BUF CLOCK L negative-going edge by means of a gate that is qualified when RDR ACTIVE and DIV 2 are both set. This negative edge parallel-loads a special character into the buffer register. At this time, the shift function of the buffer is still disabled because RDR SHIFT ENB H is still low. In effect, the shift operation is held off by RDR START, which enables the load operation.

The special character that is parallel-loaded into the buffer consists of a 1 in the eighth data bit (bit 7) and a 0 in each of the remaining bits. This is the equivalent of loading octal 200 into the buffer. The purpose of the 1 is to provide a pointer that indicates the end of the operation.

The next time the DIV 2 flip-flop changes state, the RDR START flip-flop is cleared. Since RDR START is clear, it qualifies a gate to produce RDR SHIFT ENABLE H, thereby enabling the shift function of the buffer register.

As each subsequent clock pulse shifts in another data bit from the reader, the pointer bit keeps shifting through the buffer. As the last data bit is shifted into the buffer, the pointer bit is shifted into the HALT flip-flop.

The HALT setting disqualifies a gate that causes RDR SHIFT ENABLE H to go low, thus disabling the shift function while the data is read out of the buffer. (The data remains intact although the clock continues to run.) The HALT setting also sets the RDR DONE flip-flop to signal the processor that the read operation has been completed and the data is available in TKB. The RDR DONE flag remains set until cleared by referencing (usually by reading) the buffer.

One bit time (9.09 ms) after the last bit is shifted into the buffer, the HALT flip-flop is cleared, producing a pulse which clears the RDR ACTIVE flip-flop, thereby turning off the clock and causing the buffer shift function to be enabled by producing RDR SHIFT ENABLE H. When RDR ACTIVE clears, the processor is informed that the operation is complete. At this point, all logic is back to its initial state and the receiver is ready to begin a new operation, i.e., accept a new start bit.

3.6 MAINTENANCE MODE

The maintenance mode is used to check the operation of the KL11 Teletype Control logic. Figure 3-2 is a simplified diagram of both the normal and maintenance modes. During normal operation, data from the bus is converted by the transmitter and sent to the Teletype, or data from the Teletype is converted by the receiver and sent to the bus.

During the maintenance mode, a character is loaded into the punch buffer from a memory location or from a processor register. This parallel character is then converted to serial output by the transmitter. However, as well as entering the Teletype, the serial data is also fed back into the receiver, which converts it back to parallel data and places it on the bus. If the character received by the bus is identical to the character sent out on the bus, then both the transmitter and the receiver are functioning properly.

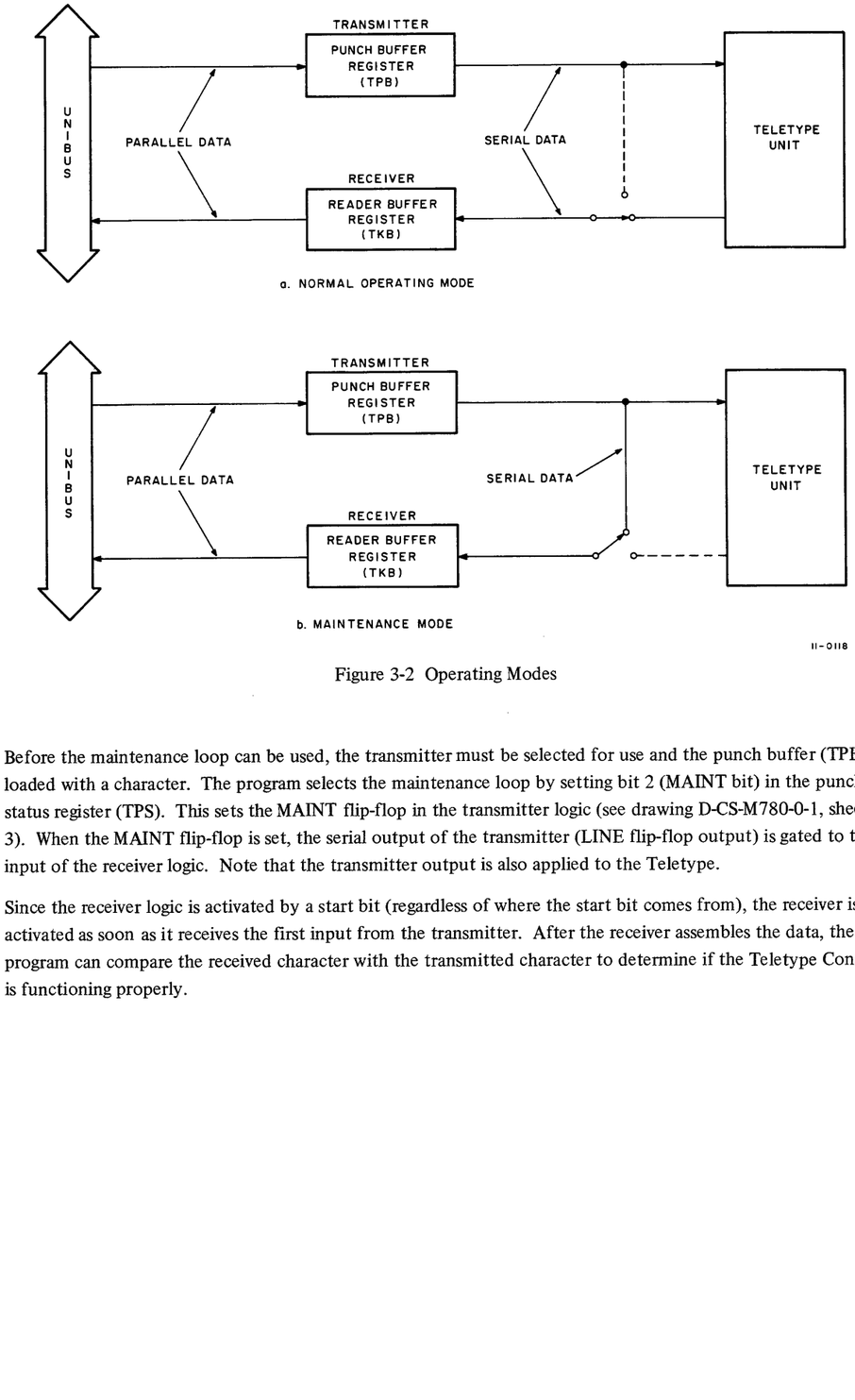


Figure 3-2 Operating Modes

Before the maintenance loop can be used, the transmitter must be selected for use and the punch buffer (TPB) loaded with a character. The program selects the maintenance loop by setting bit 2 (MAINT bit) in the punch status register (TPS). This sets the MAINT flip-flop in the transmitter logic (see drawing D-CS-M780-0-1, sheet 3). When the MAINT flip-flop is set, the serial output of the transmitter (LINE flip-flop output) is gated to the input of the receiver logic. Note that the transmitter output is also applied to the Teletype.

Since the receiver logic is activated by a start bit (regardless of where the start bit comes from), the receiver is activated as soon as it receives the first input from the transmitter. After the receiver assembles the data, the program can compare the received character with the transmitted character to determine if the Teletype Control is functioning properly.

CHAPTER 4
PROGRAMMING INFORMATION

4.1 SCOPE

This chapter presents general programming information for software control of the KL11 Teletype Control. Although a few typical program examples are included, it is beyond the scope of this manual to provide detailed programs. For more detailed information on programming, including Teletype operation, refer to the *Paper Tape Software Programming Handbook,* DEC-11-GGPA-D.

This chapter is divided into three major portions: device registers, timing considerations, and programming examples.

4.2 DEVICE REGISTERS

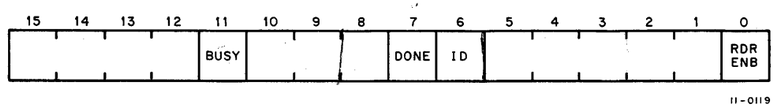
All software control of the KL11 Teletype Control is performed by means of four device registers. These registers have been assigned memory addresses, and can be read or loaded using any PDP-11 instruction that refers to their address. The four device registers and associated addresses are listed in Table 4-1.

Table 4-1
Standard Device Register Assignments

Register	Mnemonic	Address
Reader Status Register	TKS	777560
Reader Buffer Register	TKB	777562
Punch Status Register	TPS	777564
Punch Buffer Register	TPB	777566

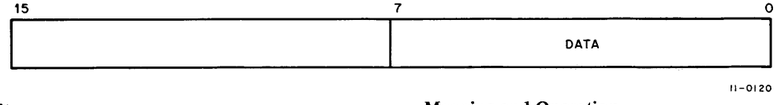
Figures 4-1 through 4-4 show the bit assignments within the four device registers. The "unused" and "load only" bits are always read as zeros. Loading "unused" or "read only" bits has no effect on the bit position. The mnemonic INIT refers to the initialization signal issued by the processor.

Note that in the figures, "reader" refers to the Teletype Keyboard/Reader and "punch" refers to the Teletype Printer/Punch.



Bit		Meaning and Operation
15 - 12	Unused	
11	BUSY	Indicates that the Teletype is receiving a start bit or information bits. Cleared by INIT; set by start bit; cleared when false start bit is detected; cleared after reception of first halt bit. Read only.
10 - 8	Unused	
7	DONE	Indicates that character is available in buffer. Cleared by INIT; cleared by referencing data buffer; causes interrupt when ID = 1. Read only. Cleared when RDR ENB is set.
6	ID	Interrupt enable on DONE. Cleared by INIT.
5 - 1	Unused	
0	RDR ENB	Enables paper-tape reader (not keyboard) to read one character. Cleared by INIT; cleared when legitimate start bit is detected. Load only.

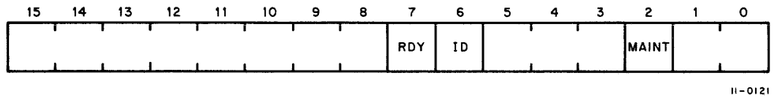
Figure 4-1 Reader Status Register Bit Assignments



Bit		Meaning and Operation
15 - 8	Unused	
7 - 0	Data Buffer	Holds character read. Cleared by legitimate start bit. Read only.

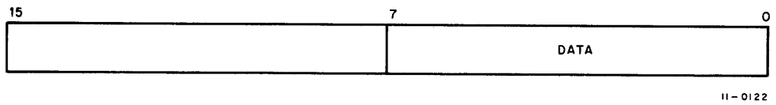
NOTE
Any reference to TKB (as word or byte) or TKB + 1 clears DONE.

Figure 4-2 Reader Buffer Register Bit Assignments



Bit		Meaning and Operation
15 - 8	Unused	
7	READY	Punch available. Set by INIT; cleared when buffer is loaded; set when punching complete. Causes interrupt if ID = 1. Read only.
6	ID	Enables READY to cause interrupt. Cleared by INIT.
5 - 3	Unused	
2	MAINT	Maintenance function. Disables serial line input from Teletype Unit and enables serial output of punch to feed into reader. Cleared by INIT.
1 - 0	Unused	

Figure 4-3 Punch Status Register Bit Assignments



Bit		Meaning and Operation
15 - 8	Unused	
7 - 0	Data Buffer	Holds character to be punched. Cleared by INIT. Load only.

NOTE

Any instruction that could modify TPB as a byte or word clears READY and initiates punching. Other reference to either byte or word has no effect on the punch.

Figure 4-4 Punch Buffer Register Bit Assignments

4.3 TIMING CONSIDERATIONS

The serial line input to the reader (see Figure 4-5) consists of 11 bits. Each bit is 9.09 ms in duration, for a total transmission time of 100 ms. The first bit is the start bit, followed by eight data bits (least significant bit first), followed by two halt bits. Thus, the maximum input rate is 10 characters per second. The DONE flag is set after the eighth data bit has been shifted into the buffer register. This occurs 77.3 ms (8-1/2 bit times) after receipt of the start bit. When characters are received from the keyboard at the maximum rate, the program has 27.3 ms after the DONE flag is set to read in the character with no information lost. (DONE flag at 77.3 ms, next incoming start bit at 100 ms, buffer loaded with octal 200 at 104.5 ms; therefore, 104.5 ms - 77.3 ms = 27.3 ms.)

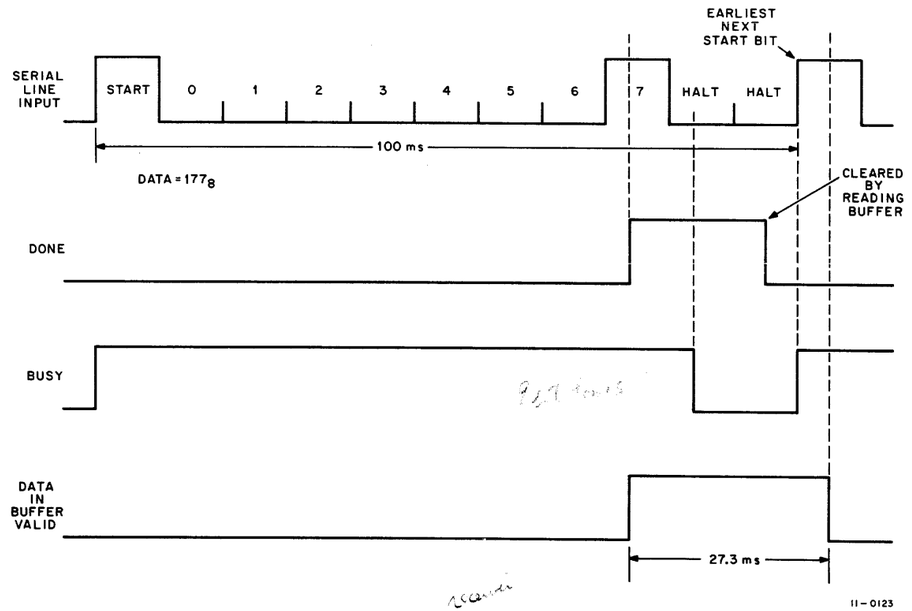


Figure 4-5 Reader Timing

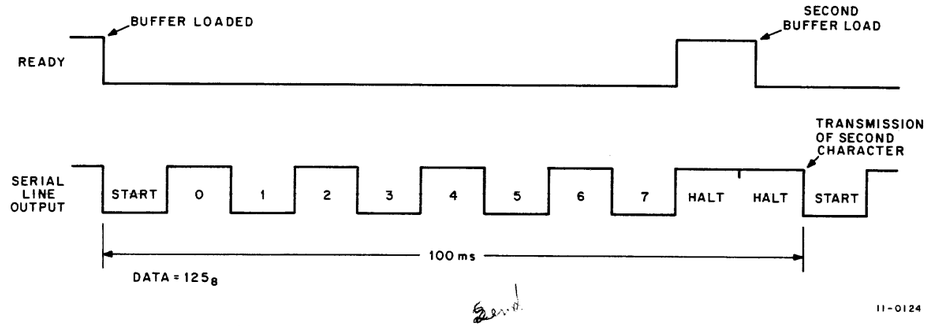


Figure 4-6 Punch Timing

When the punch buffer register is loaded, 11 bits (in the same format as the reader input) are shifted out on the serial line (see Figure 4-6). After the eighth data bit has been shifted out, the READY flag is set. This occurs 81.8 ms after the buffer is loaded. If the punching rate is to be maintained at the 10 character-per-second rate, the buffer must be reloaded within 18.2 ms (two bit times).

4.4 PROGRAMMING EXAMPLES

The following four examples represent typical programs for: reading a character, punching a character, echoing the keyboard, and reading 10 characters by means of an interrupt.

a. Reading a Character (from reader or keyboard)

```
READ:   INC TKS         ;Set RDR ENB
LOOP:   TSTB TKS        ;Look for DONE
        BPL LOOP        ;Wait if DONE = 0
        MOV TKB, R0     ;Read character
```

b. Punching a Character

```
PUNCH:  TSTB TPS        ;Test for READY
        BPL PUNCH       ;Wait if READY = 0
        MOV R0, TPB     ;Punch character
```

c. Echoing Keyboard

```
ECHO:   TSTB TKS        ;Character available?
        BPL ECHO        ;Wait if DONE = 0
LOOP:   TSTB TPS        ;Is punch ready?
        BPL LOOP        ;Wait if READY = 0
        MOV TKB, TPB    ;Punch character
        BR ECHO         ;Repeat for next character
```

d. Reading 10 Characters (by means of an interrupt)

```
START:  MOV #10, R0     ;Set up counter
        MOV #2000, R1   ;Set up buffer pointer
        MOV #101, TKS   ;Set ID and RDR ENB
TRAP:   BR TRAP         ;Hang up here until
                         block is read
                .
                .
                .
                .
                .
                .
60:     RDRINT          ;Start of reader service
                         routine
62:     000200          ;Raise processor to priority level 4
                .
                .
                .
                .
                .
                .
RDRINT: MOVB TKB, (R1)+ ;Put character into buffer
        DEC R0          ;Decrement counter
        BEQ END         ;If count = 0, get out
        INC TKS         ;Enable reader again
        RTI             ;Return from interrupt
END:    CMP (SP)+, (SP)+ ;Reset stack
        CLR TKS         ;Clear INT ENB
        JMP TRAP +2     ;Back to program
```

CHAPTER 5
ADJUSTMENTS

5.1 INTRODUCTION

This chapter provides procedures for adjusting the punch and reader clocks in the KL11 Teletype Control. In addition, an alternate method is provided when a calibrated scope is not available. In order to perform these adjustments properly, the following items are necessary: KL11 Teletype Tests (programs), KL11 Print Set, and an oscilloscope.

5.2 PUNCH CLOCK ADJUSTMENT

The punch clock (E17, DEC 9601) is adjusted by potentiometer R4. The physical location of this potentiometer is shown on drawing AR-KL11-0-5. The adjustment procedure is as follows:

Step	Procedure
1	Run program 11 of the KL11 Teletype Tests with the SWITCH REGISTER on the programmer's console set to 177.
2	Connect oscilloscope probe to pin CF1 (PUN CLOCK output) of the Teletype Control and observe that positive pulses (approximately 2-μs wide) are present.
3	Adjust potentiometer R4 until the time *between* pulses is 9.09 ms.

5.3 READER CLOCK ADJUSTMENT

The reader clock (E22, DEC 9601) is adjusted by potentiometer R12. The physical location of this potentiometer is shown on drawing AR-KL11-0-5. The adjustment procedure is as follows:

Step	Procedure
1	Run program 12 of the KL11 Teletype Tests with the SWITCH REGISTER on the programmer's console set to 177.
2	Connect oscilloscope probe to pin DR1 (RDR CLOCK output) of the Teletype Control and observe that positive pulses (approximately 2-μs wide) are present.
3	Adjust potentiometer R12 until the time *between* pulses is 4.55 ms.

5.4 USING UNCALIBRATED OSCILLOSCOPE

The adjustment procedure when using an uncalibrated oscilloscope is as follows:

Step	Procedure
1	Connect oscilloscope probes to leads 4 and 6 of the reader buffer register (E20, DEC 8271). Run program 1 of the KL11 Teletype Tests, externally triggering on pin DP1 (RDR START).
2	Observe that the negative transitions of the RDR CLOCK (lead 6) strobes the data present on lead 4 into the buffer register.
3	Adjust potentiometer R12 until the last *data* bit (bit 7) is strobed in the middle of the bit.
4	After R12 is correctly adjusted, connect the oscilloscope to pin DR1 (RDR CLOCK output) and observe that positive pulses are present.
5	Record the time interval between the positive pulses. Set the punch clock (refer to Paragraph 5.2) to twice this figure.

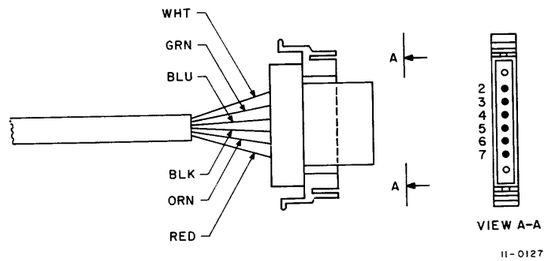
CHAPTER 6
MAINTENANCE AIDS

6.1 SCOPE

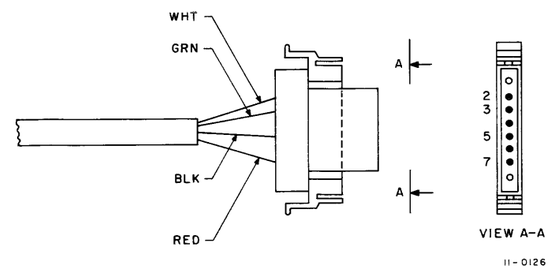
The basic maintenance philosophy of the Teletype Control is to present the user with the information necessary to understand normal operation of the unit. The user can then use this information when analyzing trouble symptoms to determine necessary corrective action. Although it is beyond the scope of this manual to present detailed troubleshooting information, some specific maintenance tips that are not obvious are included in subsequent paragraphs. General PDP-11 maintenance information is presented in the *PDP-11 Conventions Manual* (for the PDP-11/20 System) and in the *PDP-11/15 System Manual* (for the PDP-11/15 System).

6.2 GENERAL

The Teletype cable connects to the M780 module in the Teletype Control interface. The pin arrangement for connector J1, which connects to P1 on the M780 module, is shown in Figure 6-1.



a. ASR Teletype Cable



b. KSR Teletype Cable

Figure 6-1 Connector J1 Pin Arrangement

6.3 TRANSMITTER CIRCUIT

The following items should be noted whenever troubleshooting the Teletype Control transmitter circuit:

a. The function of diode D11 (in the +5V line associated with transistor Q1 in the punch output) is to keep positive spikes off the +5V line. If this component is shorted, the punch could run open intermittently. If the diode is open, the punch runs open continuously. When the punch runs open, the Teletype printing element stays in one position and "chatters".

b. To successfully run either the MainDEC System Exerciser Program (T17) or PRG5 of the Teletype MainDEC with an 33 ASR Teletype Unit, jumpers J1 and J2 must be set up for an 11-bit code (parallel with each other).

c. The output of the M780 transmitter circuit (P1, pins 2 and 5) is connected to the Teletype selector magnet through a Teletype Reader Control Board (DEC RS-B-4915). This board is mounted in the Teletype. A typical schematic of the 4915 board is shown in Figure 6-2.

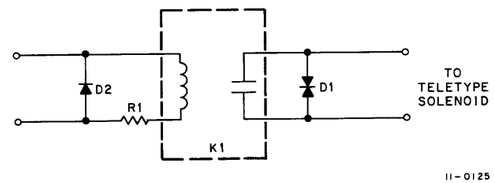


Figure 6-2 Reader Control Board – Typical Schematic

6.4 RECEIVER CIRCUIT

Capacitor C26 in the direct set line of the RDR START flip-flop, and capacitor C27 in the enabling input line to the RDR CLOCK flip-flop, prevent noise spikes. If either, or both, of these capacitors open, intermittent reader errors occur.

APPENDIX A
TELETYPE CONTROL VARIATIONS

Option	Module	Baud Rate		Halt Bits	Char/s	Bit Time (ms)		Transmitter					Receiver				
		XMIT	RECV			XMIT	RECV	C2 μF	C3 μF	R2 kΩ	R3 kΩ	R4 kΩ (Pot)	C9 μF	R14 kΩ	R13 kΩ	R12 kΩ (Pot)	C6 μF
KL11-A	M780	110	110	2	10	9.09	9.09	0.5	0.5	21.5	1.96	10	0.5	21.5	1.96	10	1.0
KL11-B	M780YB	150	150	1	15	6.67	6.67	0.5	0.5	14.7	1.0	10	0.5	14.7	1.0	10	0.01
KL11-C	M780YC	300	300	1	30	3.33	3.33	0.5	0.5	5.11	2.74	5	0.5	5.11	2.74	5	0.01
KL11-D	M780YD	600	600	1	60	1.67	1.67	0.5	0.5	2.74	1.47	2	0.5	2.74	1.47	2	0.01
KL11-E	M780YE	1200	110	1	120/10	0.833	9.09	0.22	0.22	1.96	1.47	5	0.5	21.5	1.96	10	0.01
KL11-F	M780YF	2400	2400	1	240	0.417	0.417	0.10	0.10	2.74	1.21	5	0.10	2.74	1.21	5	0.01

NOTES:

1. There is no M780YA variation.
2. Transmitter (punch) Clock (E17) runs at bit rate. Receiver (reader) Clock (E22) runs at twice bit rate.

READER'S COMMENTS

PDP-11 KL11 TELETYPE CONTROL
DEC-11-HR4C-D

Digital Equipment Corporation maintains a continuous effort to improve the quality and usefulness of its publications. To do this effectively we need user feedback – your critical evaluation of this manual.

Please comment on this manual's completeness, accuracy, organization, usability, and readability.

_____

_____

_____

_____

Did you find errors in this manual? _____

_____

_____

_____

_____

How can this manual be improved? _____

_____

_____

_____

_____

DEC also strives to keep its customers informed of current DEC software and publications. Thus, the following periodically distributed publications are available upon request. Please check the appropriate boxes for a current issue of the publication(s) desired.

☐ **Software Manual Update,** a quarterly collection of revisions to current software manuals.

☐ **User's Bookshelf,** a bibliography of current software manuals.

☐ **Program Library Price List,** a list of currently available software programs and manuals.

Please describe your position. _____

Name _____ Organization _____

Street _____ Department _____

City _____ State _____ Zip or Country _____

Fold Here

Do Not Tear - Fold Here and Staple

FIRST CLASS
PERMIT NO. 33
MAYNARD, MASS.

BUSINESS REPLY MAIL
NO POSTAGE STAMP NECESSARY IF MAILED IN THE UNITED STATES

Postage will be paid by:

digital

Digital Equipment Corporation
Technical Documentation Department
146 Main Street
Maynard, Massachusetts 01754